0.18 μm CMOS LNA AND MIXER FOR WIRELESS LAN APPLICATIONS

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Abstract -.Low Noise Amplifier (LNA) and mixer for 5.15-5.825 GHz wireless Local Area Network (LAN) applications were designed and fabricated in 0.18 μm CMOS technology. Newly proposed topologies are described. Simulation results for LNA are: Noise Figure (NF) 1.72 dB, power gain 18.6 dB, input 1-dB compression point (P_{-1dB}) –15.6 dBm. Simulation results for mixer are: power conversion gain 7.8 dB, input 3rd-order intercept point (IP3) 6.6 dBm, input P_{-1dB} –3.5 dBm, Single Side-Band NF 7.1 dB.

I. Introduction

Broadband wireless communication is the key technology to a new generation of products in the consumer market. Among other fields, broadband standards will be the basis for local area networks (LAN), and corresponding RF hardware is under active research and development. With the advent of 0.18 μm - minimum channel length process, CMOS technology becomes an attractive solution for 5 GHz-range applications. This article describes Low Noise Amplifier (LNA) and mixer for IEEE 802.11a-standard applications, designed in 0.18μm CMOS process.

II. Design Description

LNA design

The LNA has two-stage topology, first stage is Common Source amplifier, and the second stage is cascode amplifier. The key topological feature and original idea of this amplifier is inter-stage series resonance. Fig.1 shows LNA topology and equivalent circuit at the node X. Z_{sub} represents parasitic impedance to the ground through silicon substrate, Z_L is the load impedance of first stage, C_{in} is equivalent input capacitance of second stage, R_{in} represents real part of second stage input impedance, generated by inductive source degeneration L2. The L_g is tuned to series resonance with C_{in2}. This has the following effects: assuming that R_{in} is much smaller than magnitude of $Z_L \parallel Z_{sub}$, series-resonance network L_g-C_{in}-R_{in} provides low-impedance path from node X, eliminating the voltage gain from LNA input to the node X, but because of the series-resonance effect, there is a voltage gain from LNA input to the input of second stage, assuming the quality factor of resonance network is larger than 1. Therefore, Common Source (CS) stage provides the voltage gain but does not suffer from Miller effect, effectively acting as a CS transistor of a cascode amplifier. Also, low-impedance path from node X reduces current losses through substrate impedance Z_{sub}. By analyzing equivalent circuit shown in Fig1.b, it can be shown that if C_{in} is approximately equal to gate-source capacitance C_{gs2} of M2 (negligible Miller effect in 2nd stage) and R_{in} << magnitude of $Z_{sub} \parallel Z_L$, the current gain from 1st stage output to 2nd stage output i_{d2}/i_{d1} is approximated by

$$\frac{i_{d2}}{i_{d1}} \cong \frac{g_{m2}}{sC_{gs2}} \cong \frac{\omega_T}{\omega} \qquad (1)$$

where ω_T represents the cutoff frequency of M2 and ω the frequency of operation. Note that Eq.1 is valid regardless of the size of transistor M2.

At high frequencies, conventional cascode amplifier can experience significant current loss through substrate parasitics at its middle node, even with the low-impedance path into the source of Common Gate (CG) transistor. Besides reducing the gain, substrate parasitics reduce impedance seen from the source of CG transistor of cascode amplifier, seriously raising noise contribution of CG transistor and degrading overall noise performance [1]. Proposed LNA obviates these issues and therefore represents better solution for high-gain LNA comparing to two cascode-stage amplifier. Moreover, in designs with 3 or more volt of power supply, proposed AC topology can be realized with DC current reuse by stacking 1st and 2nd stages, thus sharing their DC current and reducing LNA current consumption by half.

Inter-stage series resonance benefits in the way described above at the expense of chip area occupied by inductor. Quality factor of on-chip inductors in typical integrated processes rarely exceeds 10, therefore, appearing in signal path, inductor L_g will lead to additional noise figure degradation. Also, voltage gain from LNA input to the input of 2nd stage depends on quality-factor of L_g-C_{in}-R_{in} network. Therefore, two versions of LNA layout were fabricated, one with L_g as integrated spiral inductor, and another with L_g implemented by bond-wires, which has higher quality factor.

Mixer design

The mixer depicted in Fig.2 consists of Gilbert-cell switching stage and newly proposed transconductance stage, which accommodates single-ended input signal and creates differential AC currents for switching stage, thus performing single-ended-to-differential conversion inherently. If double-balanced mixer topology is preferred in a receiver, such conversion must be performed somewhere in a signal path, since antenna is usually a single-ended device. This entails trade-offs about place of this conversion. Proposed transconductance stage allows benefiting from double-balanced mixer operation without additional signal-conversion blocks and power loss/current consumption associated with them.

The twin-well technological process allows separate N-Well (and therefore independent body-terminal connection) for every NMOS device. Consequently, biasing transistors M9 and M10 are free from body-effect, which allows symmetric DC biasing of M1-M2 and M3-M4 transconductance branches. This corresponds to significant improvement in gain and linearity performance of the mixer. Bond-wire inductors L1 and L2 were adjusted to make AC current in branches equal, which also was found to be beneficial for overall performance.

Since this mixer was designed as a part of superheterodyne receiver, the input and output matching is required for proper operation of image-rejection and IF filters. In this design, only bond-wire inductances are required for 50Ω input matching. According to simplified analysis [2], overall transconductance G_m of resonantly-matched (by inductive source degeneration) CS stage doesn't depend on transistor transconductance g_m, and depends only on device cut-off frequency ω_T, operating frequency ω and source resistance R_S:

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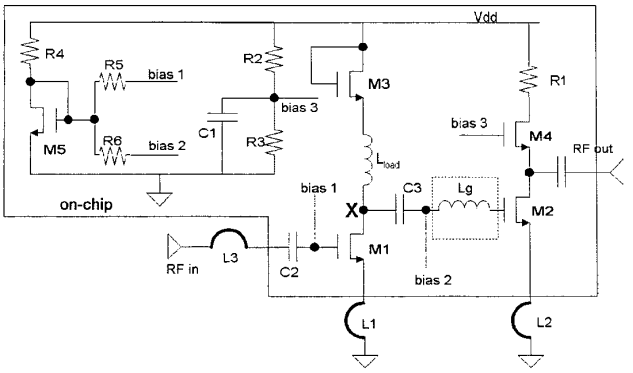

Figure 1a. LNA schematic.

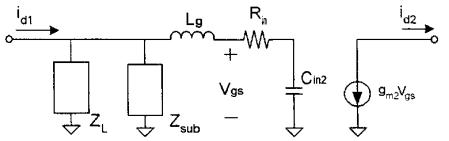

Figure 1b. Equivalent circuit at node X, looking out of M1's drain.

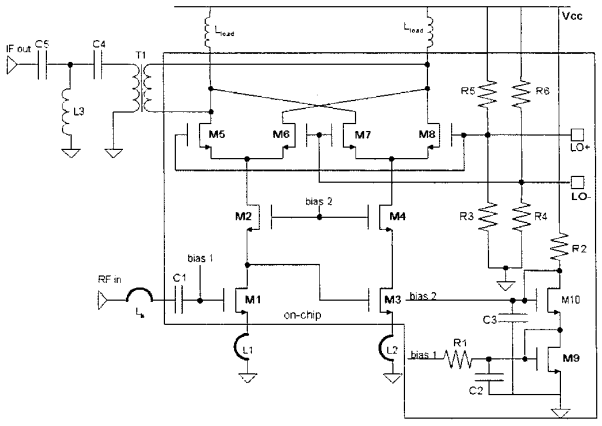

Figure 2. Mixer schematic.

$$G_m = \frac{\omega_T}{2\omega R_S} \qquad (2)$$

This fact was utilized by reducing the width of M1 and M3 in order to increase their DC current density and overdrive voltage V_{GS}-V_{TH}. This improves correspondingly ω_T of transistor and linearity of transconductance stage without decreasing of conversion gain.

During simulations, ideal transformer and external inductive load are assumed at the output of the mixer. Therefore, reported performance corresponds to the case of differential load or loss-less differential-to-single-ended conversion at the output.

III. Simulation Results

Table 1. Simulated LNA performance		
	L_g – bond-wire	L_g - integrated
Supply voltage	2.7 V	
Frequency range	5.15 – 5.825 GHz	
mag(S11)	-25.7 dB	-29.6 dB
mag(S22)	-15.2 dB	-15.6 dB
mag(S21)	18.6 dB	18.85 dB
Input P_{-1dB}	-15.6 dB	-15.7
NF	1.72 dB	1.89 dB
Power consumption	60.3 mW	60.5 mW

Table 2. Simulated mixer performance	
Supply voltage	2.7 V
Input RF frequency	5.15 – 5.825 GHz
Intermediate frequency (IF)	900 MHz
Power conversion gain	7.83 dB
Input P_{-1dB}	-3.5 dBm
Input IP3	6.6 dBm
Spot Single Side-Band (SSB) NF at 900 MHz	7.1 dB
mag(S11)	< -15.7 db
LO-IF feed-through	-18.6 dB
LO-RF feed-through	-101.2 dB
Power consumption	52.6 mW

IV. Conclusions

As a stage of wireless LAN transceiver design, LNA and mixer for 5.15-5.825 GHz applications were designed and manufactured in 0.18 μm CMOS process with square spiral inductors and Metal-Insulator-Metal capacitors. At this moment only simulation data of separated blocks is available, but simulated performance is good enough to allow successful receiver design. Also, some simulated parameters, like LNA Noise Figure and mixer IP3 are better than reported even in GaAs designs [3]. Predicted mixer's SSB NF as low as 7.1 dB is particularly interesting. Both devices introduce topological innovations, which can be utilized in a variety of applications. The chips are under experimental evaluation at this moment.

IV. References

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