A 2.4GHz Driver Amplifier for Bluetooth Application Based on 0.35μm CMOS

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Abstract – A driver amplifier for Bluetooth application is implemented in 0.35μm CMOS technology. This paper presents a driver amplifier with high linearity and gain, and demonstrates that linearity has a quality factor dependency of inductive load. The linearity difference of the driver amplifier between the external and on-chip inductive load is analyzed analytically and it is confirmed by a measurement. The measurement shows that the driver amplifier with an off-chip inductive load has a higher linearity of 3.6dB and a higher gain of 1.6dB than the driver amplifier with the on-chip inductive load has.

Index terms—Bluetooth, Driver Amplifier, PAN, Cascode

1. INTRODUCTION

Bluetooth is low cost, short-range radio technology, originally developed as a cable replacement to connect devices such as mobile phone handsets, headsets, and portable computers. However, by making wireless communications between any electrical devices possible, Bluetooth has created the notion of a Personal Area Network (PAN), a kind of close range wireless network that can change revolutionarily the way people interact with the information technology landscape around them [1].

To meet the tremendous demands for low-cost and high integration, a standard CMOS process technology is often preferred by circuit designers. Therefore, a lot of transmitter and receiver are designed for several systems.

For Bluetooth application a transmitter is generally characterized in three classes by the output power of the transmitter: 0 to 20dBm, -6 to 4dBm, and less than 0dBm [1].

For class 1 (0 to 20dBm) transmitter, in order to provide high output power for power amplifier (PA), a driver amplifier (DA) requires high enough gain. On the other hand, for class 2 (-6 to 4dBm) and 3 (less than 0dBm) transmitters, the DA requires high gain as well as high linearity. This paper presents techniques that increase linearity and gain in order to meet DA requirements of classes 1, 2 and 3 simultaneously.

2. DRIVER AMPLIFIER

Fig.1 shows the proposed DA schematic. As can be seen by Fig. 1, the driver amplifier was implemented as a single-ended configuration and two stages cascode topology for high gain. It is well known fact that the single-ended topology tends to get higher linearity at even much lower power dissipation while it is more sensitive to the supply and substrate noise than differential configuration.

From Fig. 1, it can be seen that each stage is composed of a cascode configuration. Cascode configuration improves reverse isolation and reduces the Miller effect [2].

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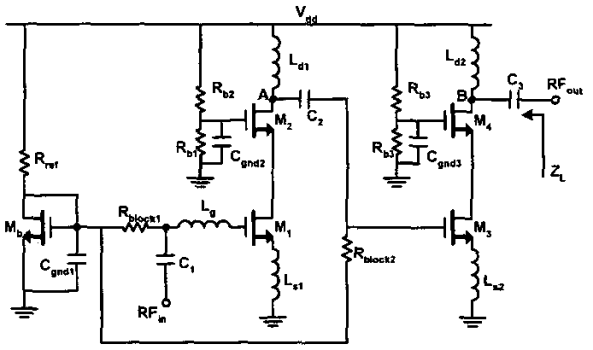

Fig.1 The proposed driver amplifier schematic

In Fig.1, resistors R_{block1} and R_{block2} de-couple the AC signal from DC bias circuit and also prevent the input signal from being affected by supply voltage fluctuation. The capacitors C_{gnd1}, C_{gnd2}, and C_{gnd3} provide AC ground at the gate node. In order to improve linearity and gain matching, as a degeneration component inductors L_{s1} and L_{s2} are implemented with bonding-wire. Proper selection of the inductors L_{s1}, L_g and size of M_1 at input stage can lead to achieve gain and noise matching simultaneously [3]. Although with transmitter the noise performance is not critical, a poor noise performance can degrade the sensitivity of receiver. Therefore, suitable noise performance is still required. Rests are bias circuit.

In the first-stage load inductor L_{d1} is an on-chip spiral inductor. In order to get maximum gain performance, inductance of L_{d1} is selected to resonate with parallel parasitic capacitance shown in the drain node of M_2 and the input capacitance of the second stage. Capacitor C_1 is a coupling capacitor, and capacitors C_2 and C_3 are used for matching and dc-blocking purposes, respectively. L_{d2} used for an inductive load of the second stage works for the same purpose as L_{d1}. But as will be discussed later, L_{d2} has a more important role to the gain and linearity of DA compare to L_{d1}.

The linearity of amplifier can be analyzed by two aspects. One is to consider the amplifier as an interconnection of two stages and the other is to look at it as an individual stage of schematic.

In the first case, when the DA is regarded as two stages amplifier, the overall linearity can be given by

$$\frac{1}{OIP_3} \approx \frac{1}{G_2 \cdot OIP_{3,1}} + \frac{1}{OIP_{3,2}} \qquad (1)$$

where OIP_3 is overall output 3rd-order intercept point, and $OIP_{3,1}$ and $OIP_{3,2}$ are the 3rd order intercept point of the first and second stages, respectively, and G_2 is gain in second stage. As can be seen from eq. (1), the linearity and gain of the second stage have stronger effect on overall linearity compare to those of the first stage. Therefore, the linearity $OIP_{3,2}$ and the gain G_2 of 2nd stage is key point improving overall linearity.

In the second case, linearity of circuit can be analyzed using taylor series concept.

The drain current i_{ds} can be given by [4]

$$i_{ds} = g_m v_i + \frac{g_m'}{2!} \cdot v_i^2 + \frac{g_m''}{3!} \cdot v_i^3 + \cdots \qquad (2)$$

where v_i is the input voltage, g_m the transconductance, and g_m' and g_m'' are the first and second derivative of g_m, respectively. As a result from eq. (2), the 3rd-order intercept point of the amplifier can be given by [5]

$$OIP_3 = 10\log\{2\frac{(g_m)^3}{|g_m''|}\mathrm{Re}[Z_L]\} + 30 \qquad (3)$$

where $Re[Z_L]$ is real value of output impedance Z_L looking

into the drain of M_4 assuming the output is reactively matched to the load. From eq. (3) it shows that linearity can be improved by increasing bias current of circuit because g_m can be increased by higher bias current. However, this approach can be in contrast with the requirements of a portable system because of high power dissipation though increasing the bias current might be beneficial for the gain and the linearity [4]. On the other hand, $Re[Z_L]$ can be increased by the proper selection of output matching circuit without worry about the high power dissipation. In this paper, the linearity of the 2nd stage amplifier is experimented as function of quality factor of the output matching circuit. In other words, linearity performance is compared with external and on-chip output inductors at the DA's second-stage load.

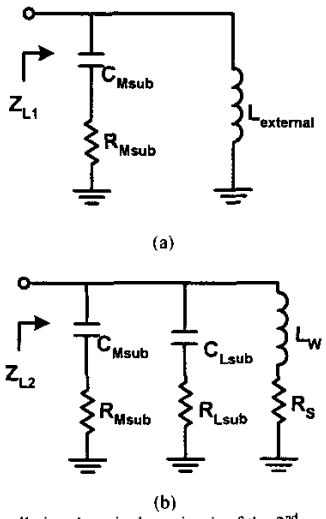

Fig.2 the small signal equivalent circuit of the 2nd stage of DA at node B, (a) the case of external load and (b) the case of on-chip load

Fig.2 shows small-signal equivalent circuits of Z_L with external and on-chip load at node B of Fig. 1. As shown in Fig. 2 the Z_{L1} is overall load impedance for external case and Z_{L2} for on-chip case, respectively. The capacitor C_{Msub} and the resister R_{Msub} represent output impedance looked into the drain of the transistor M_4 in Fig.1. In addition, the capacitor C_{Lsub}, the inductor L_W, and the resistors R_{Lsub} and R_s represent the model of on-chip spiral inductor. As can be seen from Fig. 2 (b), $Re[Z_L]$, $Re[Z_{L1}]$ is larger than $Re[Z_{L2}]$ because additional resistors R_{Lsub} and R_s decrease.

To improve linearity of amplifier, the loading inductor of the 2nd stage must have as high quality factor as possible. To maximize quality factor of load, the external inductor is recommended rather than the on-chip inductor. Inductor with high quality factor can be also helpful to increase gain of amplifier as well.

3. MEASUREMENT RESULT

Fig.3 shows measured difference of linearity between the DA with external and on-chip inductor as an output load. From Fig.3, the output P-1dB for the external load case is about 3.6dB higher than that of on-chip load case.

Measurements conformed considerations about quality factor of loading. The DA with external inductor load has 1.6dB higher gain and 0.4dB lower NF rather than that of on-chip spiral inductor under the equal power consumption of 45mW.

Fig.4 shows microphotograph of the proposed driver amplifier implemented in 0.35μm CMOS technology. As can be seen from Fig. 4, the fabricated chip shows the DA with and without output inductor as a load. Finally, Table.1 summarizes the measured performance of the proposed driver amplifier.

4. Conclusions

In the transmitter design, in order to meet the high output power specification of the transmitter, linearity and gain of a driver amplifier are tends to be key performance parameters. To achieve high linearity and gain at the same time, the proposed driver amplifier was designed as a single-ended two-stage cascade structure. This paper demonstrates that in the two stages amplifier increasing the linearity of the 2nd

stage is one solution to improve overall linearity of a system. In addition, linearity can be maximized by maximizing the quality factor of inductor used at output as a load. Therefore, measurement results have shown that attaching external inductor is useful method of improving the linearity as well as the gain of amplifier.

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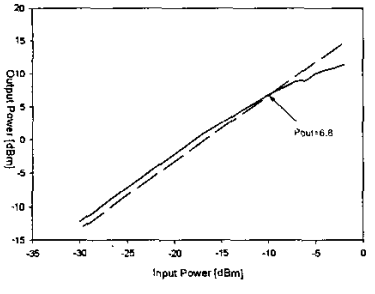
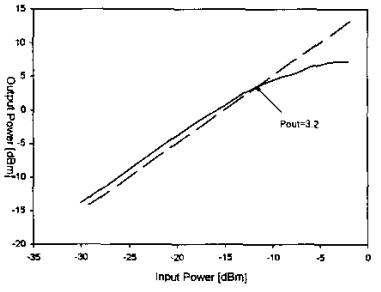


(a)

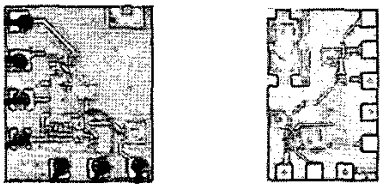


(b)

Fig.3 The input versus output response of the two DAs with (a) external inductor and (b) on-chip spiral inductor

Table.1 measurement result of the two DAs

	External	On-chip spiral
Supply voltage [V]	3	3
Gain @2.4GHz [dB]	17.8	16.2
Output P_{-1dB} [dBm]	6.8	3.2
NF @2.4GHz [dB]	5	5.4
Total current [mA]	15	15



(a) (b)

Fig.4 microphotograph of driver amplifier (a) without and (b) with on-chip spiral inductor.