A 5-GHz LNA for wireless LAN Application based on 0.5㎛ SiGe BiCMOS

Hye-Ryoung Kim, Sang-Gug Lee
School of Engineering, Information and Communication University,
P.O.Box 77, Yusong, Taejon 305-600, Korea.
Email: jamie@icu.ac.kr, sglee@icu.ac.kr

Abstract

This paper presents a 5-GHz band LNA using 0.5㎛ SiGe BiCMOS technology for wireless LAN application. To improve gain and linearity, the proposed LNA adopted a unique combination of inter-stage series resonance and linearity-enhancing bias circuit. The proposed LNA shows power gain of 18.3dB, a noise figure 1.65dB, and IIP3 – 3.95dBm while dissipating 11mA from a 3V power supply, based on simulation

Introduction

Recently, the interest in Wireless Local Area Network (WLAN) is increasing. Since the currently serviced wireless LAN systems, which operate in 2.4-GHz, have a disadvantage in terms of the data rate compare to the wired system, higher speed system is required. The representative high speed wireless LAN standards are the IEEE 802.11a and the High Performance Radio Local Area Network/2(HIPERLAN/2), which support the data rate up to 54Mbps and operate in the 5-GHz band [1]. Many researches about transceiver system on 5GHz band to meet these standards have been studied.

Among the transceiver system components, low noise amplifier (LNA) amplifies the small signal from the antenna, and dominates the overall system sensitivity. Thus, a number of 5-GHz band LNA have been developed for commercial applications based on compound semiconductor technologies. Considering the cost issue in the large volume wireless LAN market and the potential of the silicon technology to be able to handle the 5-GHz circuits, the silicon technology can be a better choice.

Table 1 summarizes performances of the previously reported LNAs based on silicon technology. All of them are implemented in CMOS technology. From Table 1, noise figure of these LNAs are poor compare to some of the commercially introduced products. For the commercial application, the SiGe technology has many advantages, yet, few papers have been reported for the 5-GHz band LNA implemented in SiGe technology. This paper presents a 5-GHz band LNA based on 0.5㎛ SiGe BiCMOS technology which features a cut-off frequency of 43-GHz and maximum oscillation frequency of 45-GHz. The proposed LNA is optimized for high gain, low noise figure, and high linearity through the combination of inter-stage series resonance technique and linearity-enhancing bias circuit. This work provides a reference for the LNA performance based on SiGe BiCMOS technology.

0-7803-7486-X/02/$17.00 © 2002 IEEE.

Table1. Performances of reported LNAs

	[1]	[2]	[3]
Technology CMOS	0.25um	0.24um	0.25um
VCC (V)	2.5	2	3
Frequency range (GHz)	5.15~5.35	5.15~5.35	5.15~5.35
Center frequency (GHz)	5.2	5.25	5.15
Gain (dB)	18	18 (voltage)	16
NF (dB)	6.4 (the overall receiver)	4.8 (LNA + filter)	2.5
Power dissipation (mW)	8.75	7.2	48

LNA Design

Fig. 1 shows the proposed LNA. The LNA consists of two stages; a common emitter and cascode amplifiers. In the first stage, L1 and L2 are assumed to be implemented with bond wire inductors and adopted for simultaneous gain and noise matching [4]. L3 is an on-chip inductor used as the load of the first stage. The diode connected transistor Q3 provides voltage drop and protects Q1 from the breakdown (V_{CE} < 2.9V), and also improves the overall stability by introducing a small resistance. C1 is a coupling capacitor. In Fig. 1, with the cascode topology, the base of transistor Q4 is connected to an ac ground through bond wire. At 5-GHz range, the cascode amplifier performance is very sensitive to the ac ground provided at the base of Q4. Therefore, it is very important to minimize the inductance from the base of Q4 to ground. In Fig. 1, L5 acts as a degeneration to improve linearity of the cascode amplifier. The series circuit of L4, the input capacitance of transistor Q2, and L5 is resonated by

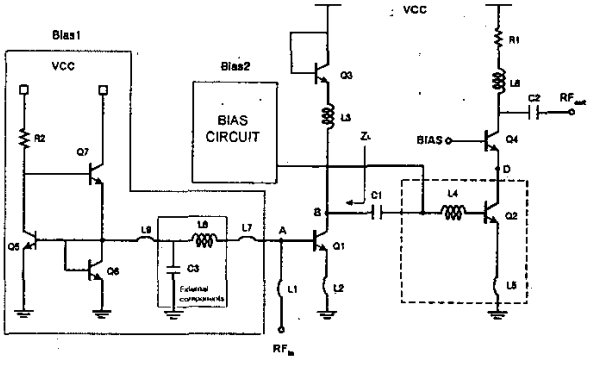

Figure 1. LNA topology

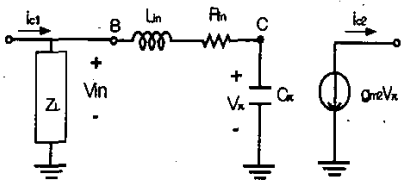

Figure 2. The equivalent circuit of A in the fig. 1

controlling the value of L4 [5]. Fig. 2 shows the small signal equivalent circuit of the part of circuit inside dashed box of Fig. 1. In fig. 2, Z_L represents the load impedance of the first stage, i_{c1} the collector current of Q1, and i_{c2} the collector current of Q2. In Fig. 2, L_{in} is the input inductance of cascode amplifier composed of L4 and L5. C_π is the base-emitter capacitance of Q2 where the Miller capacitance is neglected. R_{in} represents the real part of the input impedance of cascode amplifier. In Fig. 2, as described above, the inductance L_{in} and capacitance C_π can be set to resonate. This resonance provides low impedance at node B. Therefore, most of collector current of transistor Q1 flows into the base of transistor Q2, which is amplified by the current gain of Q2 at the frequency of operation. Under this condition, the current amplification ratio can be expressed as

$$\beta_{Q2}(\omega) = \frac{i_{c2}}{i_{c1}} = \frac{\omega_T}{\omega}$$

where β_{Q2} represents the current gain of Q2 at frequency ω and ω_T the cutoff frequency of Q2. Considering the fact that the BiCMOS technology used in this design has f_T of 43-GHz and the operating frequency is about 5-GHz, the current gain is approximately nine. The low impedance at node B also reduces gain of the first stage, thereby reducing Miller capacitance of Q1. Thus, the inter-stage series resonance leads to high overall gain.

It was reported in [6] that for a common emitter or cascode amplifier shown in Fig. 1, the linearity of each amplifier can be improved significantly when the impedance seen by the base-emitter junction of each common emitter transistor is low at dc. The bias circuits shown in Fig. 1 are designed to present low impedance at dc. In the bias circuit, the combination of external L8 and C3 are added to protect the amplifiers from the bias circuit noise at the frequency of interest. In [5], the inter-stage resonated LNA adopted the current reused topology sharing the same current in the first and second stages. However, in that topology, the impedance seen by the base-emitter junction of the common base transistor of the cascode amplifier is very high leading to poor overall linearity. Considering the linearity issue, in this work the dc currents of the first and the second stage are separated. In Fig. 1, the Bias2 is the same as Bias1 except the component values. In the bias circuit shown in Fig. 1, since the inductor induce no dc voltage drop, the proposed bias circuit encourages the class AB operation with increasing input signal. This class AB operation of the LNA leads to high –1dB compression point [7]. In Fig. 1, L8 and C3 are implemented as an external chip inductor because the value of L8 is too large for on-chip implementation. In Fig. 1, L6, C2 and R1 constitute output matching network and R1 is also used for LNA stabilization. The simulation results of the proposed LNA are shown in Table 2. As can be seen from Table 1 and Table 2, the proposed LNA has a higher gain, lower noise figure and better linearity compare to the previously reported works. Fig.3 shows the layout of the proposed LNA.

Conclusion

This paper presents a 5-GHz band LNA for the wireless LAN application based on 0.5㎛ SiGe BiCMOS

	Performance
Gain	18.3dB
NF(dB)	1.65dB
IIP3	-3.95dBm
S11	-25dB
S22	-27.3dB
Input P1dB	-12.25dB
Power consumption	31mW

Table 2. Simulation data of the proposed LNA at 5.7GHz

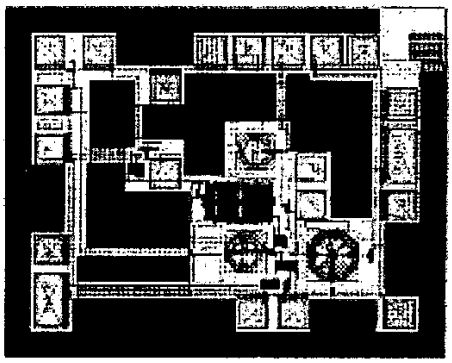

Figure 3. The layout of proposed LNA

operation of frequency of the first stage and provides high current gain to the second stage. Together with the use of the low impedance bias scheme at dc, the linearity is also improved. The simulated performance of the LNA is power gain of 18.3dB, a noise figure 1.65dB, and IIP3 – 3.95dBm while dissipating 11mA from a 3V power supply.

Reference

[1] Behzad Razavi, "A 5.2-GHz CMOS Receiver with 62-dB Image Rejection," *IEEE J. Solid- state Circuits.*, vol. 36, pp.810–815, May 2001.

[2] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE J. Solid-State Circuits*, pp.765–772, May 2000.

[3] Ting-Ping Liu and Eric Westerwick, "5-GHz CMOS Radio Transceiver Front-End Chipset," *IEEE J. Solid-State Circuits*, pp.1927–1933, Dec. 2000.

[4] Sorin P. Vinigescu and Michael C. Maliepaard, "A Scalable High-Frequency Noise Model for Bipolar Transistors with application to optimal transistor sizing for Low-Noise Amplifier design," *IEEE J. Solid-State Circuits*, vol. 32, NO 9.pp.1430–1438, Sep. 1997.

[5] Choong-Yul Cha and Sang-Gug Lee, "A Low Power, High Gain LNA Topology," *International Conference on Microwave and Millimeter Wave Technology*, Beijing, China Sep. 2000.

[6] Jin-su Ko, Hyun-Seok Kim, Beom-Kyu Ko, "Effect of bias scheme on intermodulation distortion and its use for the design of PCS Tx driver," *IEEE Radio Frequency Integrated Circuits Symposium*, 2000.

[7] Keng Leong Fong, "High-Frequency Nonlinearity Analysis of Common-Emitter and Differential-pair Transconductance Stages," *IEEE J. Solid- state Circuits.*, vol. 33, pp.548–555, April 1998.