A 5.2 GHz, 1.7 dB NF Low Noise Amplifier for Wireless LAN Based on 0.18 um CMOS Technology

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Abstract— A high gain, low noise LNA is implemented using inter-stage series resonance technique. This paper reports the implication of the quality factor of the resonating inductor on the LNA performances such as voltage and current gain, noise figure, and power gain. Two versions LNAs with low and high Q resonating inductors are designed for 5.2 GHz applications based on 0.18 μm CMOS technology. Simulation results show power gain of 18.9 dB, NF of 1.7 dB, and OIP3 of 12.9 dBm from the high Q inductor version.

Index terms— LNA, RF frequency, resonance, quality factor, CMOS, Wireless LAN, Integrated.

I. INTRODUCTION

With the recent proliferation of wireless communication applications, there is an extensive effort to develop low cost, highly integrated RF circuits. In typical receiver architectures, a low noise amplifier is the one of the most critical blocks to determine the sensitivity of communication systems. Generally, at high frequencies, GaAs and SiGe Bipolar technologies are used to achieve high performances such as high gain, high linearity, and low noise. However, with the commercial products, one of the most important factors that need to be considered is the cost, where the CMOS technology has competitive advantage. In order to be competitive, the performances of CMOS based RF circuits need to be comparable.

Many high gain and high linearity amplifier topologies have been proposed to satisfy the performance requirements such as low power, low noise, and high linearity. Typically, cascode is the choice because it is easy to satisfy both noise and power gain requirements [1]. However, at high frequencies, the substrate parasitic reduces impedance seen by the source of common gate (CG) transistor of cascode topology such that the noise contribution of CG transistor is increased, which degrades the overall circuit noise performance [2]. Besides that, cascode amplifier can experience significant current loss through the substrate parasitic at the drain node of common-source transistor leading to overall gain reduction. As an alternative, an LNA topology with inter-stage series resonance network is proposed in [3], [5]. However, in the reported [3], [5], the authors did not clearly explain the implication of the quality factor of the inductor used for the series resonance. This paper analyzes the effect of inter-stage inductor quality factor on the performances of LNA. The LNAs are optimized based on this insight and applied for 5.2 GHz band for the optimum NF, gain, and linearity.

II. LNA DESIGN

Fig. 1 shows the proposed LNA schematic, which consists of two stages. The first stage is common source (CS) amplifier, which includes M_1, L_g, L_s, M_4, and L_1, which is used as a choke. The diode connected M_4 is used for the voltage drop because of the supply voltage limitation on M_1. Moreover, M_4 also contributes to improve the stability of the first stage by reducing the quality factor of inductor L_1. In the first stage, L_s and L_g are used for simultaneous matching of gain and NF [1], [2].

The second stage has cascode configuration, which consists of transistors M_2, M_3, and the degeneration inductor L_3 which is used to improve linearity. The capacitor C_c is for the ac coupling; L_2 and C_o are for the output matching. In Fig.1, an inter-stages inductor L_c is included to resonate with input capacitance of second stage (C_{in2}), which can improve the gain and NF of the amplifier.

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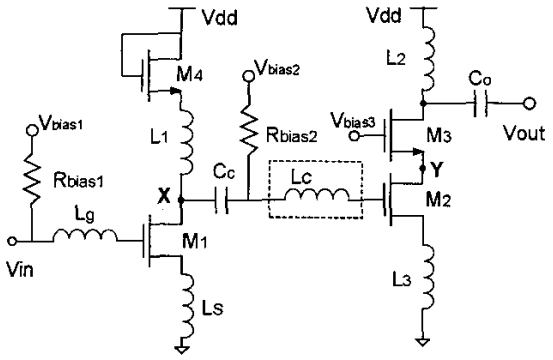

Fig. 1. The proposed LNA schematic

The small signal equivalent circuit of the proposed LNA from the drain node of M_1 to that of M_2 is shown in Fig. 2. In Fig.2, Z_{sub} and Z_{L1} represent parasitic impedance to the ground through silicon substrate and the load impedance of the first stage; R_{in} and C_{in2} are the real part of the input impedance and equivalent input capacitance of the second stage seen from node X, respectively. In Fig. 2, if R_{in} is much smaller than $|Z_{L1} // Z_{sub}|$, the series resonance network L_c-C_{in2} will provide low impedance at node X. Under the series resonance, and assuming $C_{in2} \cong C_{gs2}$, the current gain from the drain of M_1 to that of M_2 can be given by.

$$\frac{i_{d2}}{i_{d1}} \cong \frac{g_{m2}}{sC_{gs2}} \cong \frac{\omega_T}{\omega_0} \qquad (1)$$

where i_{d1}, i_{d2} are the currents of M_1, M_2; C_{gs2} and g_{m2} are the gate-source capacitance and transconduc-tance of the M_2, respectively. ω_T represents the cutoff frequency of M_2 and ω_0 is the operating frequency.

Note that equation (1) is valid regardless of the size of transistor M_2 and the value of R_{in} as long as $R_{in} << |Z_{L1} // Z_{sub}|$. In equation (1), with given 0.18 μm CMOS technology, the proposed series resonance can provide current gain more than 7. In addition, due to the small impedance presented at node X, the proposed topology can avoid the signal loss through substrate. Besides, the low impedance at node X also reduces voltage gain of the first stage so that the Miller effect on M_1 is reduced.

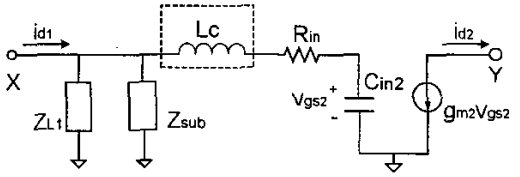

Fig. 2. Equivalent circuit of proposed LNA

In Fig. 1, the effect of quality factor of the inter-stage series resonance network on the performances of LNA is one of the importance factors that need to be considered. From Fig. 2, the quality factor (Q) of the resonance network can be calculated by [11]

$$Q = \frac{\sqrt{L_c C_{in2}}}{R_{in}} \qquad (2)$$

and

$$R_{in} = \frac{g_{m2} C_{gs2}}{L_3} + R_{Lc} \qquad (3)$$

where R_{Lc} is parasitic series resistance of L_c. As can be seen in (2) and (3) the Q of resonance network can depend significantly on R_{Lc}. The effect of R_{Lc} on the performances of LNA can be summarized as follows: First, if $R_{in} << |Z_{L1} // Z_{sub}|$, the series resonance condition will provide low impedance at node X such that the current gain from node X to node Y does not depend on R_{Lc}. Second, the voltage gain, A_v, from the gate of M_1 to that of M_2 can be calculated base on the equivalent circuit shown in Fig. 3

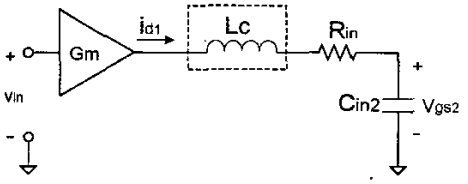

Fig. 3. Equivalent circuit to calculate voltage from input to the input of the second stage

From Fig. 3, the output current of the first stage can be given by

$$i_{d1} = G_m . v_{in} \qquad (4)$$

The voltage at the input of the second stage is

$$v_{gs2} = i_{d1} \cdot \frac{1}{sC_{in2}} = \frac{1}{sC_{in2}} . G_m . v_{in} \qquad (5)$$

Therefore, the voltage gain A_v can be expressed as

$$A_v = \frac{v_{gs2}}{v_{in}} = G_m \cdot \frac{1}{sC_{in2}} \quad (6)$$

As can be seen in (6), the voltage gain A_v is independent from R_{in}, such that R_{Lc} does not affect the voltage gain of the amplifier.

However, since the voltage gain of the M_1 is small, the thermal noise generated by R_{Lc} will directly show up at the input of LNA such that the noise performance of LNA can be degraded. In addition, the power gain of the overall LNA can be reduced due to power loss through R_{Lc}.

The noise generated by diode connected M_4 and the parasitic resistance of L_1 are insignificant at node X due to the large impedance provided by L_1.

III. SIMULATION RESULTS

Considering the effect of R_{Lc} on the performances of LNA, two versions of LNAs are designed. In the first version, L_c is implemented by an on-chip spiral inductor, which is the case of low quality factor. With the other one with L_c is realized by bonding wire, which can provide high quality factor. Simulation results of NF and power gain of two versions are shown in Fig. 4.

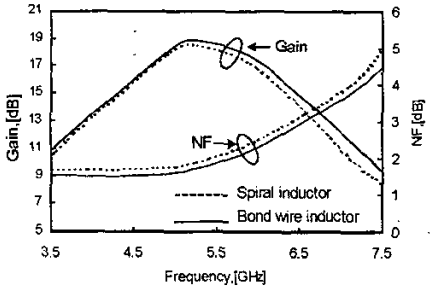

Fig.4. Comparison NF and Gain of LNAs by using spiral and bond wire inductors.

As can be seen from Fig. 4, the on-chip inductor version has significantly higher noise figure compare to the bonding wire one, while the power gain reduction is less significant as expected.

The results of two versions LNA are summarized in Table 1, which are simulated based on 0.18 μm CMOS technology. Table 2 shows the comparison between this work and some other reported works. As can be seen in Table 2, the proposed LNA shows the lowest NF and highest power gain compare to previous works. Fig. 5 shows layout of the two proposed LNA versions

Table 1. Performances of two LNA versions

Parameters	Bond-wire	Spiral inductor
S11/S22 [dB]	-25.7 /-15.2	-29.6 /-15.6
S21 [dB]	18.9	18.5
NF [dB]	1.7	1.9
Input P1dB[dBm]	-15.7	-15.6
OIP3 [dBm]	12.9	12.9
Power [mW]	22.3	22.5

Table 2. Performances comparisons

Parameters	[7]	[8]	[9]	**This work**
Freq. [GHz]	5.25	5.8	5.2	5.2
Tech. [μm]	0.25	0.25	0.25	0.18
Supply [V]	3.0	2.0	1.5	2.7
Gain [dB]	14.4	10	17	18.9
NF [dB]	2.5	3.0	2.1	1.7
OIP3 [dB]	12.9	12	-	12.9
Power [mW]	24	20	9	22.3

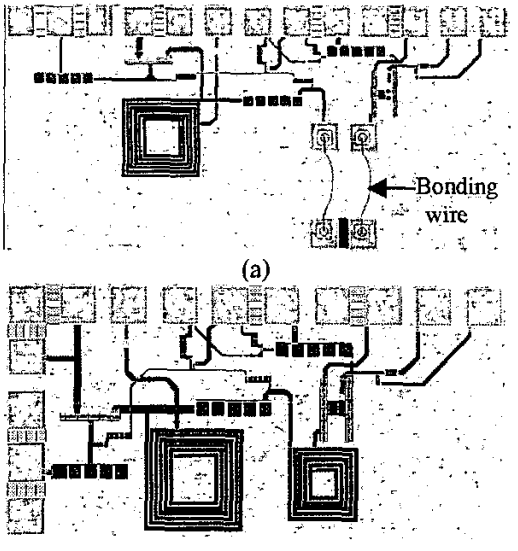

Fig. 5 Layout of proposed LNA.
(a) Using bonding wire as inter-stage inductor
(b) Using spiral on-chip inductor

IV. SUMMARY

This paper proposes a high gain, and low noise LNA. The LNA consists of two stages. The first stage is the common source amplifier and the second has cascode configuration. High gain and low noise are achieved by the use of inter-stage series resonance technique. Inter-stage series resonance network provides the current gain from the drain of the first transistor to that of the second transistor. It also provides low impedance at the output of the first stage, therefore the signal loss through silicon substrate is avoided and the Miller effect of the first stage is reduced. The effect of the quality factor of inter-stage series resonance network on the LNA performance is analyzed. The current gain and voltage gain are not affected by quality factor of resonance network. However, the parasitic resistance of inter-stage inductor will affect the noise figure and the power gain of the proposed LNA. To demonstrate the effect of quality factor of inter-stage inductor, two version of LNAs are designed, one with low quality factor, which is the case of on-chip inductor and the other one with higher quality factor, which is the case of using bonding wire. Simulation results show that the on-chip inductor version gives slightly lower power gain but a little more significant noise figure degradation.

Two versions of proposed LNA are fabricated based on 0.18 μm CMOS technology, which under evaluation and the results will be presented at conference.

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