A Complementary Colpitts Oscillator based on 0.35 μm CMOS Technology

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Abstract

A new complementary Colpitts CMOS oscillator topology is proposed and analyzed based on one port model. Analysis indicates that the proposed complementary Colpitts oscillator topology has advantage over other topologies for low phase noise and high frequency operation while dissipating small power. The analysis also provides the design guidelines for optimizing the phase noise of the proposed topology. The performance advantage of proposed oscillator topology originates from the simplicity, composed of effectively only two components (complementary transistor and one inductor), and the higher negative conductance of oscillator core. The proposed VCOs are fabricated using 0.35 μm CMOS technology for 2, 5, 6, and 10GHz band. Measurement shows excellent performance considering the technology and power dissipation in 5 and 6 GHz band VCOs.

1. Introduction

Integrated CMOS VCO is one of the key technologies to realize the single chip RF ICs. With increase in the frequency of operation, e.g., above 5 GHz, the implementation of integrated CMOS VCO becomes ever challenging. Due to the parasitics in active and passive components, optimizing the circuit and device topology is the key strategy for the performance enhancement as a way to improve the quality factor of the tank circuit. In CMOS technology, the substrate parasitic impedance of the MOSFET, the series resistance of spiral inductor, and the series and parallel parasitic resistance of the capacitors are the factors that contribute the degradation of the quality-factor of the tank circuit. Another factor that determines the oscillator performance is the negative conductance. The larger amplitude of negative conductance can provide potential to achieve lower phase noise with lower power dissipation. Therefore, the smaller number of components and the larger (negative) conductance in oscillator core are the directions for the integrated low phase noise and high frequency oscillator design with lower power consumption.

Most of the previously reported VCOs tend to rely on the negative-G_m topology, and focuses on the layout optimization techniques such as the transistor structure, the quality-factor of the passive components, symmetry, etc [1-3]. In negative-G_m based sub-micron CMOS VCOs, the NMOS-only topologies tend to show poor phase noise than that of the complementary topology. The blames for the performance degradation in the NMOS-only topologies are the hot carrier effect, poor symmetry, and lower g_m [3]. Traditionally, the Colpitts oscillator has been the most favored topology for low phase noise [4]. Even though, small-signal wise, the NMOS-only based Colpitts is simple (for example, compare to negative-G_m oscillator), the overall circuit schematic can be quite complicated considering the additional bias circuit and the buffer interface.

This work reports a complementary Colpitts oscillator that is composed of effectively two components, a complementary N- & PMOS transistor pair and an inductor. The proposed oscillator requires no additional circuit for biasing and buffer interface, which is desirable for low phase noise and high frequency operation with low power dissipation. In section II, the operational principle and the phase noise optimization method of the proposed complementary Colpitts oscillator are described. Section III describes the experimental results of the fabricated VCOs and the comparison with the previous works, and section IV concludes.

2. Complementary Colpitts oscillator topology and the one-port analysis

2.1 One-Port Analysis

Fig. 1(a) and 1(b) show the proposed complementary Colpitts oscillator and the equivalent small-signal circuit, respectively. In Fig. 1(b), G_{m0}, C_{gs}, C_{sub}, and R_{sub} represent the overall transconductance ($g_{mn}+g_{mp}$), the overall gate-source capacitance, the drain to substrate parasitic capacitance and the resistance of the transistors M_1 and M_2 in Fig. 1(a), respectively. In Fig. 1(b), R_f represents the series resistance of inductor L_f. From Fig. 1(a) and 1(b), the transistors M_1 and M_2, the inductor L_f, and the gate-source capacitors C_{gs}, and the substrate parasitc capacitance C_{sub} constitutes a Colpitts oscillator. As described before, the simplicity and the complementary structure of the proposed Colpitts oscillator increases the potential for the lower phase noise, higher frequency of oscillation, and the lower power dissipation.

For the better understanding and the design optimization, the one-port analysis for the small-signal equivalent circuit shown in Fig. 1(b) is described in the following, which can be compared the analysis on reference [5]. From Fig. 1(b), the branch currents, $i_d(s)$ can be given by

$$i_d(s) = \frac{G_{m0}}{s^2 L_f C_{gs} + sC_{gs}R_s + 1} v_d(s) = G_m(s) v_d(s) \quad (1)$$

where v_d represents the small-signal drain node voltage of the N- and PMOS transistors. Based on Eq. (1), the small-signal circuit shown in Fig. 1(b) can be modified

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as shown Fig. 2(a). In Fig. 2(a), the equivalent conductance, $G_m(s)$, can be expressed as follows

$$G_m(s) = G_{m0}\frac{1-\left(\frac{\omega}{\omega_{sr}}\right)^2}{\left[1-\left(\frac{\omega}{\omega_{sr}}\right)^2\right]^2+\left[\left(\frac{\omega}{\omega_{sr}}\right)/Q_{sr}\right]^2} + \frac{1}{j}\frac{G_{m0}\left[\left(\frac{\omega}{\omega_{sr}}\right)/Q_{sr}\right]}{\left[1-\left(\frac{\omega}{\omega_{sr}}\right)^2\right]^2+\left[\left(\frac{\omega}{\omega_{sr}}\right)/Q_{sr}\right]^2} \quad (2)$$
$$= G_r + \frac{1}{j\omega L_i}$$

where $Q_{sr} = \sqrt{L_f / C_{gs}}/R_f$, $\omega_{sr}^2 = 1/(L_f C_{gs})$. In Eq. (2), Q_{sr} and ω_{sr} represent the quality-factor and resonance frequency of the series R_f-L_f-C_{gs} circuit, respectively. From Eq. (2), it can be seen that the real value of the conductance, G_r, becomes negative when $\omega > \omega_{sr}$, meaning that the proposed oscillator can oscillate at frequencies above ω_{sr}. The negative conductance generation behavior can be explained as follows; at frequencies above ω_{sr}, due to the series connection of L_f and C_{gs}, the phase delay at the gate-node of the transistor w.r.t. the drain-node becomes larger than 90°, and this leads to the drain current inversion. As shown in Eq. (2), the imaginary part of $G_m(s)$ can be represented by an equivalent inductor at all frequencies, and by the similar mechanism, the inductance increases rapidly for $\omega > \omega_{sr}$. At a very high frequency oscillation, the channel transition delay of mobile carrier in MOSFET may also contribute phase delay.

$$G_r = G_{m0}\frac{1-\left(\frac{\omega}{\omega_{sr}}\right)^2}{\left[1-\left(\frac{\omega}{\omega_{sr}}\right)^2\right]^2+\left[\left(\frac{\omega}{\omega_{sr}}\right)/Q_{sr}\right]^2} \quad (3)$$

$$L_i = \frac{1}{G_{m0}\omega_{sr}}\frac{Q_{sr}\left\{\left[1-\left(\frac{\omega}{\omega_{sr}}\right)^2\right]^2+\left[\left(\frac{\omega}{\omega_{sr}}\right)/Q_{sr}\right]^2\right\}}{\left(\frac{\omega}{\omega_{sr}}\right)^2} \quad (4)$$

Based on above discussions, the equivalent circuit shown in Fig. 2(a) can be modified like the way shown in Fig. 2(b). In Fig. 2(b), the conductance $G_m(s)$ is represented by two separate components; the equivalent real conductance G_r and the inductance L_i. Now, for frequencies $\omega > \omega_{sr}$, where G_r becomes negative, the circuit shown in Fig. 2(b) becomes the familiar one-port oscillator model. From Eq. (2), G_r and L_i are re-expressed as follows

Fig. 3 shows the variation of the normalized negative conductance, G_r/G_{m0}, as a function of the resonance frequency of the series R_f-L_f-C_{gs} network, ω/ω_{sr}, for various values of Q_{sr}. As can be seen in Fig. 3, the proposed oscillator topology provides large negative conductance over wide frequency band of operation, especially at frequency range of $1.1\omega_{sr} < \omega < 1.3\omega_{sr}$ and for high value Q_{sr}.

Note that the reference conductance value $G_{m0} = g_{mn} + g_{mp}$. Fig. 3 indicates that the proposed topology is suitable for very low power oscillation, especially when high quality factor inductors are adopted.

In Fig. 3, $G_r = 0$, when $\omega = \omega_{sr}$. As mentioned before, at this frequency, the phase difference between the drain and gate nodes of the transistors in Fig. 1(a) becomes 90°. Therefore, no real component is created in $G_m(s)$. Now, at frequencies slightly higher than ω_{sr}, the phase of gate node rapidly approaches 180° leading to negative real conductance. In this frequency region, the voltage drop across the gate-source capacitor is amplified by the amount of the quality factor of the series R_s-L_f-C_{gs} circuit, which explains the sharp increase in G_r in Fig. 3. As frequency increases further, the phase of the gate node approaches 180°, where the amplification factor diminishes, and the voltage division mechanism dominates the voltage drop across the gate-source capacitor. Therefore, the negative conductance decreases with increase in frequency.

Fig. 4 shows the variation of the value $L_i/(1/G_{m0}\omega_{sr})$ as a function of relative frequency ω/ω_{sr}. Considering the fact that the typical values for G_{m0} (1 ~ 30 mS) and ω_{sr} (1 ~ 5 GHz), from Fig. 4, it can be seen that the values for L_i ranges from a few to a few hundred nano-Henry, depending on the frequency of operation and the quality factor Q_{sr}. Therefore, at frequencies near ω_{sr}, L_i can play major role in determining the frequency of resonance. However, with low G_{m0} and ω_{sr} system, L_i contributes little on the oscillation frequency.

II.2 Phase Noise Optimization

Based on Fig. 2(c), the oscillation frequency of the proposed complementary Colpitts oscillator would be determined by the combined parallel resonant frequency of L_f, C_{gs}, C_{sub}, C_L and L_i. The capacitor C_L is the loading capacitor at the drain node of M_1 and M_2 shown in Fig. 1(a). According to Leeson's phase noise model [9] and Hajimiri's phase noise model [10], there are two portions in phase noise contribution, amplitude fluctuation and phase perturbation. In the low frequency offset, the phase perturbation term is the dominant factor, which is inversely proportional to the square of the maximum charge swing, q_{max}, where $q_{max} = C_{tank} \times V_{max}$, C_{tank} and V_{max} is the according capacitance and maximum voltage swing of parallel tank, respectively [10]. In generally, the increase of C_{tank} is not efficient way in the constant negative-G_m oscillator, ex, differential oscillator, which decreases the loaded Q of tank and also V_{max}. Distinctively, the proposed complementary oscillator provides large negative conductance over wide frequency band of operation and has the peak near the frequency ω_{sr} shown in Fig. 3. By adjusting the capacitance of C_L in Fig. 2(C), the oscillation frequency of the proposed oscillator can be controlled without affecting the frequency behavior of G_r and the combined quality factor of R_s-L_f-C_{gs} and C_{sub}-R_{sub} branch. The

increase of C_L makes the oscillation frequency approach to the w_{sr}, decrease the quality factor of the series R_s-L_f-C_{gs} branch, but, increase the quality factor of the C_{sub}-R_{sub} branch and also rapidly increase the negative conductance. The increase of negative conductance make slow the decrease of V_{max} for large loading of C_L. This means that the increase of q_{max} is possible at the same with the increase of C_L. In addition, for large CL, the cyclo-stationary phase noise contribution of MOSFET can be suppressed since the phase difference between gate and drain node in Fig. 1(a) approached to 90°.

Simulation shows that the phase noise improvement has 20dBc/dec dependency over the increase of capacitance, C_L. For example, the 10pF loading of C_L has 20dBc improvements in phase noise performance over 1pF loading of C_L. From the simulation, the optimal oscillation frequency for minimum phase noise of the proposed oscillator is located at frequencies 1.1 ~ 1.3 times higher than ω_{sr}, depends on the quality factor of the inductor L_f.

3. Experimental Results

Fig. 5 shows the complete schematic of the proposed complementary Colpitts oscillator applied for VCO, which includes a directly coupled inverter as a buffer. In Fig. 5, C_{var} represents an accumulation-mode MOS varactor, R_b the ac blocking resistor, C_{by} the bypass capacitor to ac ground. In Fig. 5, the varactor is connected on the gate-side of the oscillator core in order to obtain wider tuning range. The capacitve loading on the drain-side of oscillator core is larger than that of the gate-side due to the drain junction capacitances of core transistors and the input capacitances of the inverter buffer. The L_o and C_o are added for impedance matching and dc blocking.

Several VCOs of the topology shown in Fig. 5 with different frequency of oscillation, 2GHz, 5GHz, 6GHz, and 10GHz bands, has been fabricated based on 0.35 μm CMOS technology. With 2 and 10GHz band VCOs, the inductors are implemented as an external PCB spiral and on-chip bond-wire, respectively, while on-chip spiral inductors are used for the 5 and 6GHz band VCOs.

The performances of the VCOs are evaluated for various power dissipations by changing the supply voltage. Table I summarizes the measurement results in comparison with other reported 5GHz band VCOs. The fabricated VCOs have not been optimized for minimum phase noise following design guidelines as described in the previous section. However, overall the proposed VCO shows respectable performance considering the inferior technology, especially, the 5GHz band VCO shown in Table I presents better performance than that of the corresponding previous work, which is implemented using 0.25μm CMOS technology. In Table 1, for the 2GHz band VCO with external PCB spiral, the phase noise performance can be improved more than 15dBc by increasing the loading capacitance. Fig. 6 shows the phase noise measurement result at 6GHz. In Fig. 6, the phase noise at 1MHz offset is −119.3dBc while dissipating 4.6mA of current from 2.0V supply. Fig. 7 shows the micrograph of the fabricated VCOs; 6, 10, 5, and 2GHz bands, respectively.

4. Conclusions

A complementary Colpitts CMOS oscillator topology is newly proposed and analyzed based on one-port oscillator model. Proposed Colpitts oscillator core composed of only two components; a complementary transistor and one inductor. The one-port analysis indicates that the proposed oscillator is adequate for high frequency, low noise, and low power application, due to the simplicity and high negative conductance of the oscillator core. The phase noise performance of the proposed oscillator can be improved by placing large loading capacitor at the drain node of oscillator. One-port analysis and simulation shows that the optimum oscillation frequency of proposed oscillator is located at frequencies 1.1 ~ 1.3 times higher than ω_{sr}, depends on the quality factor of the inductor L_f. Several VCOs of 2, 5, 6, and 10GHz bands are fabricated using 0.35 μm CMOS technology. The measurement results prove the topological advantages of the proposed oscillator over other VCO topologies. The phase noise of 6GHz VCOs at 1MHz offset is −119.3dBc while dissipating 4.6mA of current from 2.0V supply.

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Table I. Measurement results of proposed VCO and other publications

Freq. [GHz]	Supp. Volt.	DC Current	PN@1MHz/ Meas. Freq.	Output Power [dBm]	Tech. CMOS [μm]
9.92~ 10.59	3.3 V	15mA	-114dBc/10.5G	+ 0.5	0.35
6.50 ~ 6.92	3.3 V	15mA	-121.7dBc/6.9G	+ 5.1	0.35
5.65 ~ 5.98	2.5 V	8.93mA	-118.9dBc/5.9G	+ 1.8	0.35

5.69 ~ 6.02	2.0 V	4.63mA	-119.3dBc/6.0G	- 2.5	0.35
2.43 ~ 2.55	2.0 V	4.66mA	- 123.22dBc/2.53G	+ 1.8	0.35
2.49 ~ 2.62	1.5 V	2.42mA	- 116.58dBc/2.55G	- 3.4	0.35
[3]	1.5V	4.7mA*	-117dBc/5.35G	-	0.25
[6]	2.5V	2mA*	-112dBc/5.8G	+ 0.9	0.25
[7]	2.5V	5.5mA*	-114dBc/5.0G	-	0.25
[8]	2.7V	4.0mA*	-110dBc/4.7G	-	0.35

* VCO core current only

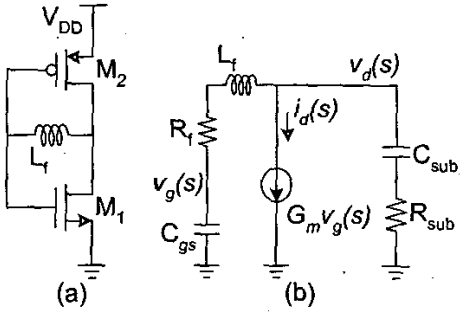

Fig. 1. The proposed complementary Colpitts oscillator: (a) original schematic (b) small-signal equivalent circuit with parasitic.

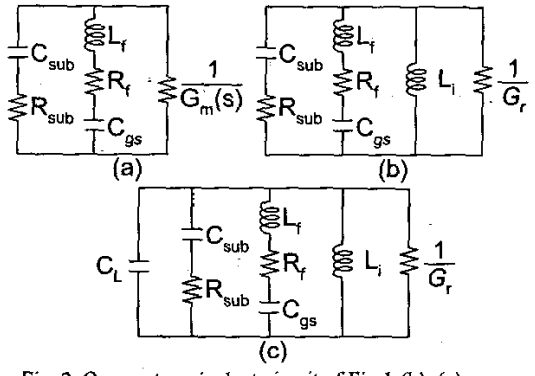

Fig. 2. One port equivalent circuit of Fig.1-(b): (a) one-port equivalent circuit, (b) modified one-port equivalent circuit, and (c) one-port equivalent circuit with loading capacitor.

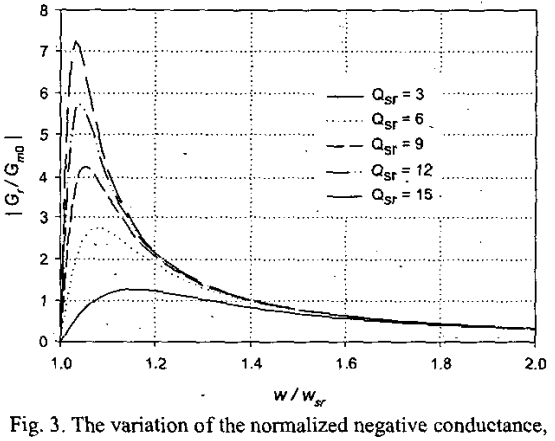

Fig. 3. The variation of the normalized negative conductance, G_r/G_{m0}, as a function of ω/ω_{sr}, for various values of Q_{sr}.

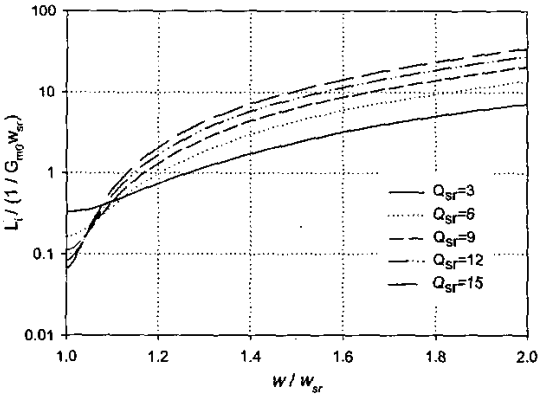

Fig. 4. The variation of the value $L_f/(1/G_{m0}\omega_{sr})$ as a function of relative frequency ω/ω_{sr}.

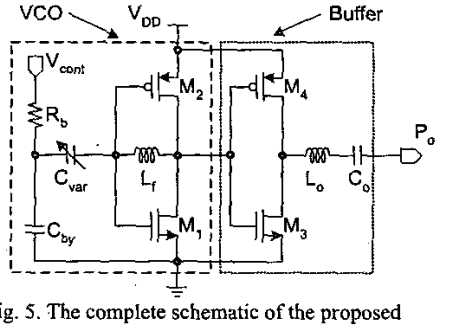

Fig. 5. The complete schematic of the proposed complementary Colpitts oscillator applied for VCO.

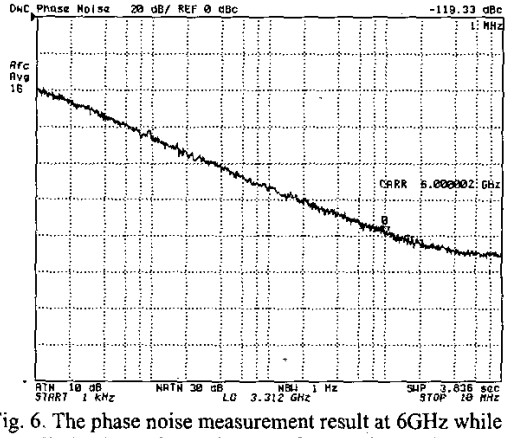

Fig. 6. The phase noise measurement result at 6GHz while dissipating 4.6mA of current from 2.0V supply.

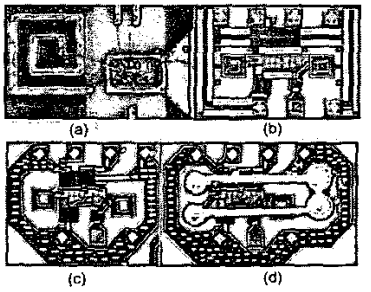

Fig. 7. Fabricated oscillator micrograph for (a) 2 GHz, (b) 5 GHz, (c) 6 GHz, and (d) 10 GHz band application.