Low Power Quadrature VCO with the Back-Gate Coupling

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Abstract

A new quadrature VCO (QVCO) is proposed with the NMOS back-gate as a coupling transistors. The advantage of proposed QVCO is analyzed in terms of power consumption and phase noise. Additional design techniques are applied to improve the symmetry of the complimentary VCO and to suppress the tail current noise contribution. The very low power QVCO has been fabricated in 0.18um CMOS technology for 1GHz band operation and obtained phase noise of -120 dBc/Hz at 1MHz offset while dissipating only 3mA for the whole QVCO from 1.8V supply.

I. Introduction

The demand for low cost, low power, and small size has been increasing with the extensive researches on transceiver architecture and RF circuit design. In implementing the RF transceivers, the low power consumption is one of the challenging requirements due to the battery lifetime.

In the last few years, the popularity of direct conversion architecture has been dramatically increased because of the possibility for the low power, low cost, and single-chip transceiver [1], [2]. The quadrature VCO is one of the key elements that are required to implement direct conversion transceiver. The low power QVCO design has been one of the most challenging hurdles in implementing the low power transceivers since the QVCO tends to dissipate too much current.

The reported quadrature generation techniques are the combination of VCO and poly-phase filter, frequency-division using flip-flop, ring oscillator, and LC oscillator with coupling transistors (QVCO). Among the reported quadrature generation techniques, the QVCO shows the better phase noise [3], [4], [5].

Figure 1 shows the conventional QVCO schematic. In Figure 1, each oscillator consists of a cross-coupled pair of transistors (M_1, M_2, and M_3, M_4) with LC tuning circuit L_L and C_V. The additional transistors (M_5, M_6, and M_7, M_8) are used for quadrature coupling between two separate differential VCOs [3].

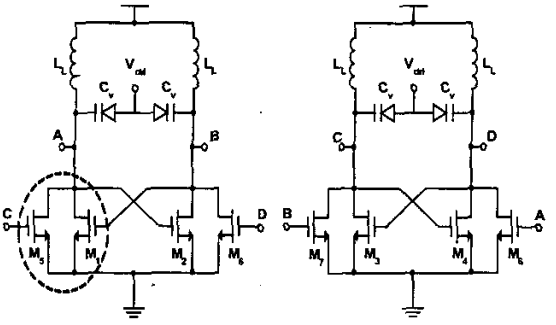

Figure 1. The Conventional QVCO schematic

Based on the conventional topology shown in Figure 1, many works have been reported to achieve the better phase noise and lower power dissipation. Compared to the other QVCO, the complementary QVCO in [4] shows good phase noise with improving passive components and achieves lower current consumption by operating the VCO in the current limited region. Even though the complementary QVCO can provide good phase noise with the reduced power consumption, power dissipation is still on the high side for low power application. For the four coupling transistors consume more than 25% of total current. In addition, the four coupling transistors contribute additional noise to the LC tank and the variation of the transconductance of coupling transistors by 1/f noise degrades the phase noise [5].

II. New Quadrature Coupling Topology

As a way to reduce the power consumption in the QVCO, this paper proposes a new coupling topology which does not require additional coupling transistors. Figure 2 shows the proposed QVCO circuit. In Figure 2, each transistor is assumed to be in separate wells. In this topology, then, we could use the NMOS back-gates to couple the signals between the two differential VCO, instead of the transistors.

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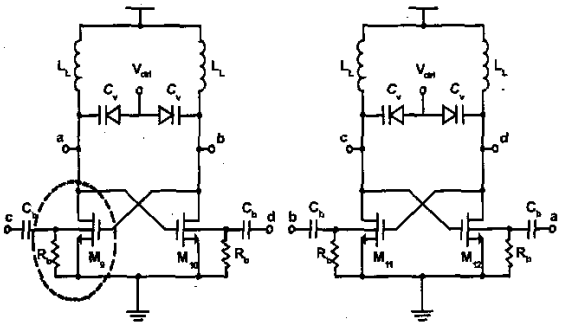

Figure 2. The proposed back-gate coupled QVCO schematic

As can be seen from Figure 2, compared to the conventional topology shown in Figure 1, the coupling transistors are removed in the proposed QVCO, and the coupling signal is applied to the back-gates of the core NMOS transistors. In Figure 2, the resistor R_b is added for the DC biasing of the body terminals and the capacitor C_b represents the coupling capacitor.

In Figure 1, the main signal coming from node *B* and the coupling signal coming from node *C* set the signal values at node *A*. Like wise, in Figure 2, signals from node *b* and node *c* set the value for node *a*. Figure 3 (a) and (b) show the small signal equivalent representation for the part of the circuit circled with the dashed lines in Figure 1 and 2, respectively. In Figure 3 (b), the v_{gs9} and v_{bs9} are the corresponding signals of v_{gs1} and v_{gs5} in Figure 3 (a), respectively. Like wise, g_{m9} and g_{mb9} are the matching components to g_{m1} and g_{m5}, respectively. Therefore, the small-signal circuits shown in Figure 3 are effectively the same. Thus, the back-gate in Figure 3 (b) replace the coupling transistor M_5 of the conventional QVCO.

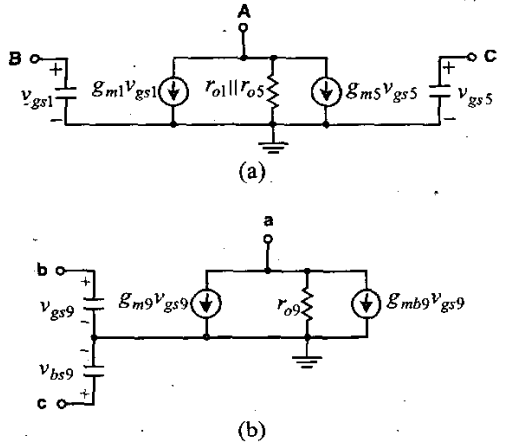

Figure 3. The small-signal equivalent circuits of Figure 1 and Figure 2

Note that, in Figure 1, the coupling transistors require additional power dissipation and contribute noise signals to the LC tank. In addition, according to [5], the phase noise in the conventional QVCO is greatly degraded by the variation of G_{Mc}, the transconductance of coupling transistors. The 1/f noise currents from the coupling transistors produce a slowly varying current offset which affects the current level flowing into the tank. This in turn changes G_{Mc} and coupling of both oscillators, so it modulates the output frequency, and eventually degrades the phase noise. Therefore, the back-gate coupling topology of this work has a clear advantage in power dissipation as well as the phase noise characteristics.

III. QVCO Design and Experimental Results

Figure 4 shows the implemented quadrature VCO schematic. As shown in Figure 4, the QVCO consists of two identical complementary differential oscillators, and the two oscillators are coupled directly by the NMOS back-gates for the quadrature outputs. In Figure 4, the resistors R_1 and R_2 are used as current sources in order to improve the symmetry of the complimentary differential oscillators, which helps to reduce the phase noise. The value of R_1 and R_2 is chosen for maximum current limited operation. The capacitor C_g in Figure 4 is added to suppress the injection of the high-frequency noise from the current source into the oscillator core by the large amplitude harmonics of the output. In Figure 4, due to the differential voltage swing of the harmonics of each differential oscillator core at node X and Y, one on-chip coupling capacitor cancels out these harmonics. Compare to the previous work [6], where the current source is shunted by a capacitor terminated to the off-chip ground, the on-chip capacitor can provide low impedance up to very high frequency due to its high resonance frequency. [6]

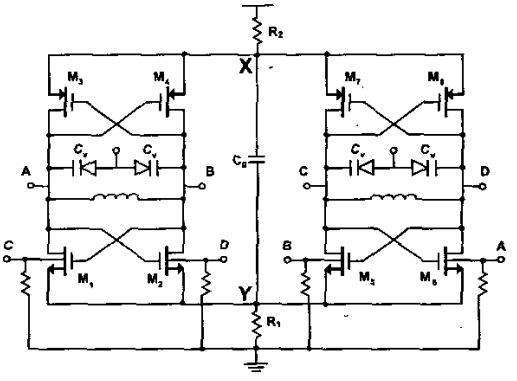

Figure 4. The implemented QVCO schematic

The proposed QVCO shown in Figure 4 is implemented with a standard 0.18um CMOS technology for 1GHz band operation. Figure 5 shows the die photograph of the implemented QVCO. As can be seen in Figure 5, the on-chip spiral inductors and accummlation mode MOS varactors are used as tuning elements. Figure 6 shows a plot of measured phase noise versus offset frequency at 1.1GHz oscillation. The phase noise at 1MHz offset is –120dBc/Hz while dissipating total of only 3mA for the whole QVCO from 1.8V supply. Figure 7 shows the output power spectrum of the QVCO with output power of 2.8dBm. The tuning range of 28.3% is achieved as shown in Figure 8. Table 1 gives a summary of the measurement results of the QVCO.

Table 2 shows the recently published QVCOs' performance, along with this work. As can be seen from Table 2, the QVCO implemented in this work dissipates the least amount power.

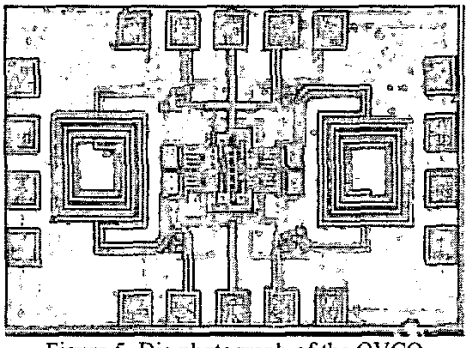

Figure 5. Die photograph of the QVCO

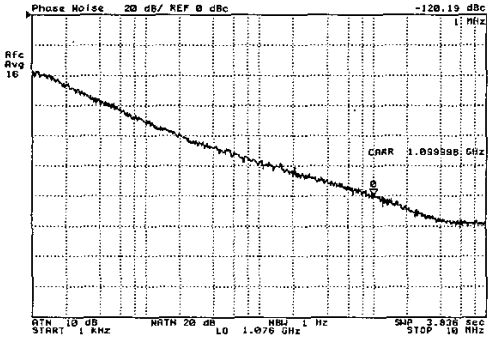

Figure 6. Measured phase noise at 1.1GHz

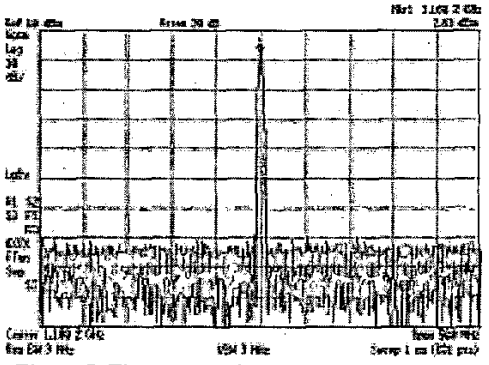

Figure 7. The measured output power spectrum of the QVCO

Supply voltage	1.8 V
Current of oscillator core	3 mA
Output power	> 2.5 dBm
Center frequency	1.21 GHz
Tuning range	1.047 ~ 1.39 GHz
Phase noise @ 1 MHz	- 120 dBc/Hz
Process	0.18μm CMOS technology

Table 1. Summary of the QVCO performance

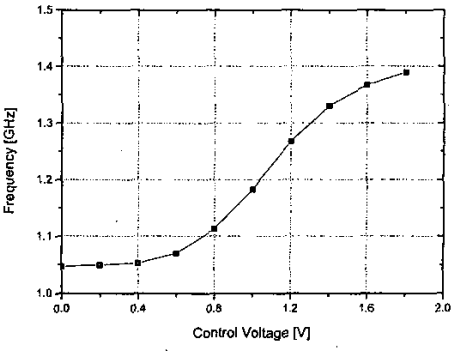

Figure 8. Measured frequency versus control voltage of the QVCO

VCO	Tech [um]	Freq. [GHz]	Power [mW]	Phasenoise [dBc/Hz]
[4]	0.25	1.8	20	-143
[5]	0.35	1.8	50	-140
This	0.18	1.1	5.4	-137

Table 2. The Measurement results with previous QVCOs (Phase noise is recalculated at 3MHz offset)

V. Conclusions

The very low power CMOS quadrature VCO is realized with the NMOS back-gate coupling topology. The advantage of proposed QVCO is analyzed in terms of power consumption and phase noise. Additional design techniques are applied to improve the symmetry of the complimentary VCO and to suppress the tail current noise contribution. The proposed QVCO fabricated in 0.18um CMOS technology is designed for 1GHz band operation obtaining phase noise of –120dBc/Hz at 1MHz offset while dissipating only 3mA for the whole QVCO from 1.8V supply.

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