Ultra Low-Voltage and Low-Power dB-Linear V-I Converter Using Composite NMOS Transistors

Quoc-Hoang Duong, Trung-Kien Nguyen, Hoang-Nam Duong and Sang-Gug Lee

Abstract - **In this paper, an ultra low-voltage and low-power exponential V-I converter is developed, using Taylor series expansion for realizing the exponential characteristics. The new CMOS exponential V-I converter is based on the composite NMOS transistors. The newly proposed approximation function based on Taylor's concept is used to extend the dB-linear output current range. In a 0.25 μm CMOS process, the simulations show more than 20 dB output current range and 18 dB-linear range with the linearity error less than ± 0.5 dB. The average power dissipation is less than 50 μW at ± 1 V supply voltage. The proposed EVIC can be used for the design of an extremely low-voltage and low-power variable gain amplifier (VGA) and automatic gain control (AGC).**

I. INTRODUCTION

In the past decade, CMOS technology has played a major role in the rapid advancement and the increased integration of very large scale integration (VLSI) systems. Low-voltage and low-power VLSI circuits are of particular interest in the field of microelectronics. The advances in the CMOS VLSI technology and the market demand for portable and mobile electronic equipment lead to increasing reductions on the power consumption. CMOS devices feature high-input impedance, extremely low-offset switches, high packing density, low-switching power consumption, and most importantly, they are easily scaled. Scaling down the transistor sizes can then integrate more circuit components in a single chip so that the circuit area, and thus its cost, will be reduced [1]. When a MOS transistor size is decreased, not only are its channel length and width reduced, but also the thickness of the gate oxide. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced. With advances in CMOS digital signal processing technique, CMOS became a main fabrication process for analog and mixed signal processing circuitry.

The dB-linear V-I converter is the key component for the design of VGAs and AGCs, which are widely used in analog signal processing; such as in hearing aids, disk drive, and telecommunication applications [2-4]. This converter is not available in CMOS technology since CMOS transistors follow a square-law characteristic in strong inversion. However, it is easily obtained in bipolar technology. Unfortunately, the bipolar techniques for VGAs and AGCs are not compatible for monolithic low voltage CMOS-based analog and mixed-signal circuits. Moreover, good performance bipolar transistors are not readily available in the conventional technology, while BiCMOS solution may not be cost-effective. Although CMOS transistors exhibit exponential characteristics in weak inversion, except the very low-speed applications, the circuit could be too slow.

Since there is no intrinsic logarithmic MOS device operating in the saturation region for CMOS technologies, the exponential characteristics can be implemented by using a "pseudo-exponential" generator [2-5], or Taylor series expansion for realizing the exponential characteristics [6-9]. Based on Taylor concept, the dB-linear V-I converter (EVIC) can be implemented by using building blocks [5,6], or by using composite NMOS transistors [8,9]. However, these previously reported EVICs tend to show very small dB-linear variation of the output current (less than 15 dB with a linearity error less than ± 0.5 dB) [7,8]. Moreover, EVICs in [7,8] are not power efficient (≅ 0.9 mW). Although the circuit in [9] is simple with high dB-linear range, the power consumption is still high (0.3 mW) and the input voltage dynamic range are restricted.

To overcome these difficulties, this paper presents a new and very simple EVIC using the composite NMOS transistors and the newly proposed approximation function to increase the dB-linear output current range as well as the differential input swing with ultra low-voltage supply (less than ± 1V) and ultra low-power consumption (less than 50 μW). The Simulation results will be given to verify the validity of this approach.

II. APPROXIMATION METHOD

A. Basic Concepts

According to the Taylor's series expansion, a general exponential function can be expressed as

Quoc-Hoang Duong is now a master student at RFME lab, Information and Communication University, 58-4 Hwaam-Dong, Yuseong-gu, Daejeon, South Korea.
Email: Hoang@icu.ac.kr Tel. (82-42) 866 6203

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$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \ldots + \frac{a^n}{n!}x^n + \ldots \quad (1)$$

where a and x are the coefficient and the independent variable, respectively. Obviously, for $|ax| \geq 1$ the exponential function cannot be implemented by a low-order polynomial. The exponential function can be approximated with small deviation from the ideal exponential function by eliminating the higher order terms for $|ax| << 1$. By neglecting the terms higher than second-order in Eq. (1), the approximation equation can be given as.

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (2)$$

The comparison between the "Pseudo-exponential" approximation, Taylor's approximation and the ideal exponential given in Fig. 1. As can be shown in Fig. 1 by the 'o'symbol line, for $|ax| \leq 1$, Eq. (2) provides 14 dB variation and 12 dB-linear variation with the error less than ± 0.5 dB.

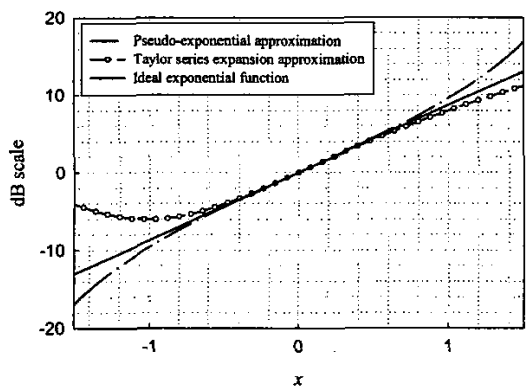

Fig.1 Comparison between the Ideal exponential function and the approximation function based on "pseudo-exponential" function and Eq. (2).

B. Approximation method

The proposed approximation function is adopted from [9]. Typically, the "pseudo-exponential" generator is of particular interest since it provides larger dB-linear range (about 15 dB with the error < ± 0.5 dB as shown in Fig. 2 by the diamond's symbol line) compared to that of the other one. Unfortunately, the "pseudo-exponential" method in which the exponential function is expressed as: $\exp(2x) \cong (1+x)/(1-x)$ is difficultly implemented due to the requirement of division function. Differently, the approximation function based on Taylor series expansion follows a squaring function and comprises only additive functions as shown in Eq. (2). Moreover, as mentioned previously, the CMOS transistors have square-law characteristics in strong inversion. Consequently, the approximation based on Taylor series expansion can be easily implemented in CMOS technology. Although this method results in small dB-linear output current range, its simplicity still attracts designers to design the dB-linear V-I converter simply by using building blocks [6,7], or by using composite NMOS transistors [8,9]. This paper uses a new approximation as follows [9]

$$e^{ax} \cong k + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (3)$$

For k = 1, Eq. (3) actually becomes Eq. (2) which provides 14 dB amplitude variation, and 12 dB range with linearity error less than ± 0.5 dB for $|x| \leq 1/a$ as shown in Fig. 1 by the dashed line.

Using Matlab simulation tool for simulating Eq. (3), the results show that for k slightly less than 1, the approximation in Eq. (3) shows higher dB-linear range than that of Eq. (2). As shown in Fig. 2 by the o'symbol line for k = 0.95, the dB-linear range is extended to about 15 dB with linearity error less than ± 0.5 dB which is almost the same as the performance of the "Pseudo-exponential" approximation. While k decreases, the dB-linear ranges can be extended to even much higher values as depicted in Fig. 2 for k = 0.9 and 0.8. The proposed idea in this paper opens up a new possibility for designers to take full advantages of the approximation method based on Taylor series expansion without any sacrifices.

III. CIRCUIT DESCRIPTIONS

The circuit design is based on the composite NMOS transistor [10] as shown in Fig. 3 with the assumption that transistors M1 and M2 are identical and operating in saturation region without body effects. The drain currents of M1 and M2 follows the below equation:

$$I_{d1} = \frac{K_n}{2}(V_{in} - V_Y - V_{tn})^2 \quad (4)$$

$$I_{d2} = \frac{K_n}{2}(V_Y - V_1 - V_{tn})^2 \quad (5)$$

where $K_n = \mu C_{ox} W/L$ is the process parameter and V_{tn} is the threshold voltage, V_{in} is the input voltage. The subtraction between the above two currents leads to the following equation

$$I_{d1} - I_{d2} = \frac{K_n}{2}(V_{in} - V_Y - V_{tn})^2 - \frac{K_n}{2}(V_Y - V_1 - V_{tn})^2 \quad (6)$$

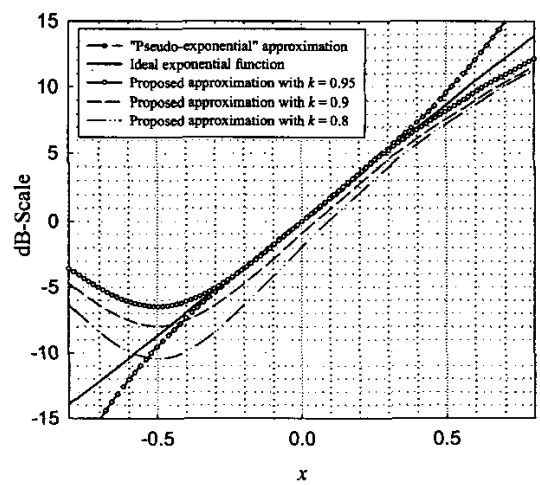

Fig.2 Plot of various functions on a decibel scale

In order to apply Eq. (3), a tunable bias current, $I_0 = K_n V_0^2/2$, is added to the Eq. (6). The voltage V_1 is equal to the negative supply voltage, V_{ss}, from Eq. (6) the following equation applies:

$$I_{out} = I_{d1} - I_{d2} + I_0 \quad (7)$$

$$= \frac{K_n}{2}\left[V_0^2 + (2V_{in} - V_{ss})(2V_Y + V_{ss}) - 2(V_Y + V_{in})V_{in} + V_{in}^2\right]$$

$$= \frac{K_n}{2}\left[V_0^2 + (2V_{in} - V_{ss})(2V_Y + V_{ss})\right] \times$$

$$\times\left[1 - \frac{2(V_Y + V_{in})}{\left[V_0^2 + (2V_{in} - V_{ss})(2V_Y + V_{ss})\right]}V_{in} + \frac{V_{in}^2}{\left[V_0^2 + (2V_{in} - V_{ss})(2V_Y + V_{ss})\right]}\right]$$

Obviously, the output current, I_{out}, is a squaring function of V_{in}. The I_{out} as an exponential approximation function of V_{in} as in Eq. (3) can be obtained by adjusting I_0 as well as V_0^2. From Eq. (7), the approximation as in Eq. (2) is achieved for I_0 satisfying the following equation

$$I_0 = \frac{K_n}{2}V_0^2$$

$$= \frac{K_n}{2}\left[2(V_Y + V_m)^2 - (2V_{tn} - V_{ss})(2V_Y + V_{ss})\right] \quad (8)$$

The proposed dB-linear V-I converter for realizing Eq. (7) is shown in Fig. 4. In Fig.4, the transistors M1 and M2 form the composite NMOS transistors, the transistor M4 copies the drain current of M1. This current is added to the bias current, I_0, and is subtracted to the drain current of M2 to form the output current as in Eq. (7). Theoretically, the input range of this circuit should be

$$V_Y + V_{tn1} \le V_{in} \le V_{dd} - |V_{tp3}| + V_{tn1} \quad (9)$$

where V_{tn1} and V_{tp3} are the threshold voltage of transistors M1 and M3. As shown in Eq. (9), the smaller the V_Y the lager the input voltage swing is. As in [8], the V_Y is rather high (-0.75 V) such that the dynamic input range is limited. Though [9] reduces the V_Y closely to V_{ss} + V_{tn1}, it can only improve the input dynamic range in a small value. In this paper, the reuse of the drain current, I_{d1}, flowing through the transistor, M5, will generate the V_Y as the bias voltage of M2. For extremely low drain current of M1, the V_Y is relatively closed to Vss such that the dynamic input range is improved drastically. In this case, the transistor M2 is in triode region and cut-off , however, as in Eq. (7) the exponential approximation is still maintained. As the I_{d1} increases to drive the M2 to saturation region, the composite NMOS transistor will be in use.

As in [8,9], the two current mirrors are needed to stabilize the V_Y such that the power consumption is rather high (0.3 mW and 0.8 mW). The idea of reusing the I_{d1} in this paper results in a very compact circuit with wide input range as shown in Fig. 4 and 5. Moreover, reusing I_{d1} not only improves the dynamic range, but also reduces the power consumption critically (50 μW) compared to [8,9].

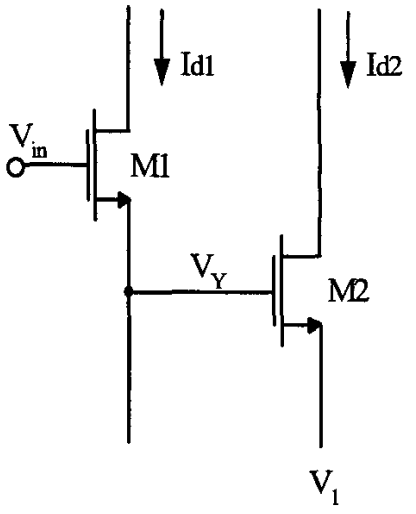

Fig.3 Composite NMOS transistors

IV. SIMULATION RESULTS

The aspect ratios of all transistors in Fig. 4 are listed in Table 1. The simulation results are shown in Fig. 5. In Fig. 5, as V_{in} varies from –0.3 V to 1 V, and I_0 = 5 μA, the approximation as in Eq. (2) is achieved with 12 dB range and the linearity error is less than ± 0.5 dB as shown in Fig.5 by the dashed line. By reducing I_0, the dB linear ranges are increased as depicted in Fig. 5 by the dash-dotted, dash-dot-dotted, and o'symbol lines. The 'o'symbol line, which is corresponding to I_0= 2 μA, shows more than 20 dB range and 18 dB linear range with linearity error less than ± 0.5 dB over a large input voltage range from –0.3 V to 0.9 V.

Based on 0.25 μm CMOS process, the V_{tn1} and $|V_{tp3}|$ are respectively 0.48 V and 0.6 V. Theoretically, the input voltage swing is from –0.52 V to 0.88 V. Therefore, when V_{in} > 0.88 V, the simulation result deviates from the ideal line.

V. CONCLUSION

A new dB-linear V-I converter based on the proposed modified Taylor series expansion is presented with the use of composite NMOS transistor. The proposed EVIC achieves 18 dB-linear range with the linearity error less than ± 0.5 dB over large input voltage swing (from –0.3V to 0.9V) with ultra low power consumption (less than 50 μW). The proposed circuit can operate at rather low supply voltage (less than ± 1 V). However, the input voltage swing is proportional to the supply voltage. The circuit is compact and power-efficient. It could be used in the design of extremely low-voltage low-power VGA and AGC.

TABLE 1
ASPECT RATIOS OF TRANSISTORS IN FIG. 4.

Transistors	Aspect ratios μm/μm
M1, M2	1/4
M3, M4	40/1
M5	200/1

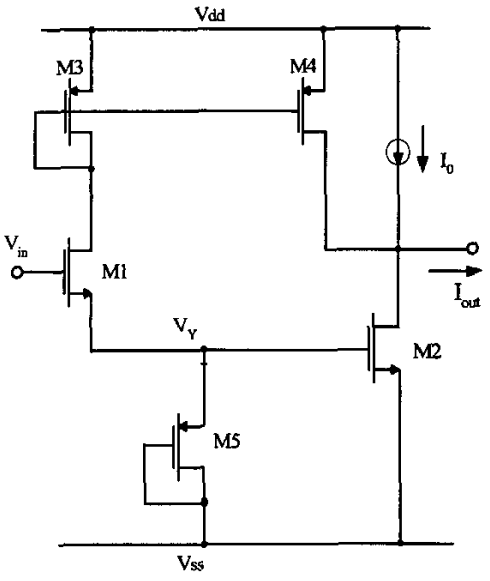

Fig.4 The complete proposed exponential V-I converter.

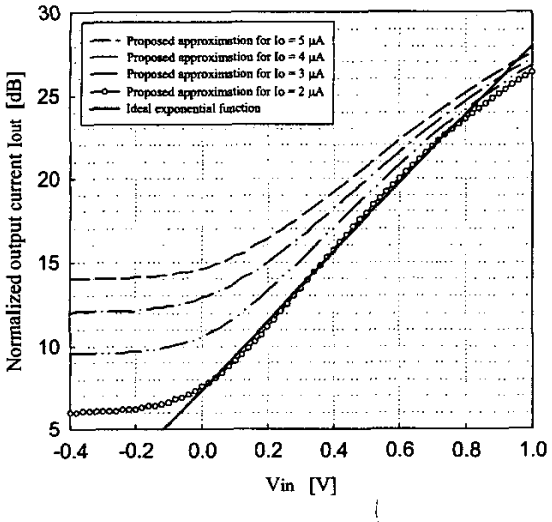

Fig.5 The I-V performance of the proposed EVIC shown in Figure 4 for various I_0.

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