Noise and Gain Optimization Technique for RF-Integrated CMOS Low Noise Amplifier

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Abstract

In this paper, very simple and insightful sets of noise parameters expressions for power-constrained simultaneous noise and input matching CMOS LNA design technique are newly introduced. Based on the noise parameters expression, the design principle, advantages, and limitations are clearly explained. Additionally, this paper proposes a gain enhancement technique that is implemented by using simple positive feedback. The proposed LNA is optimized for 5 GHz WLAN applications based on 0.18 μm CMOS technology. Measurement results show power gain of 18 dB, NF of 1.5 dB, and IIP3 of -5 dBm while dissipates the DC current of 4 mA at supply voltage of 2.5 V.

1. INTRODUCTION

In typical receiver architectures, a low noise amplifier (LNA) is one of the key components that determine the sensitivity of the receiver [1], [2]. Generally, the goal of LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation. A number of LNA design techniques have been reported to satisfy these goals [3]-[6]. The LNA design optimization technique proposed in [6] can be applied for power-constrained simultaneous noise and input matching. However, as discussed in [6], the fully potential of this technique is not provided clearly. This paper attempts to analyze and try to provide consistent and perspective understanding of this technique based on the noise parameter expressions. In addition, by using the noise parameter expressions, the design principle, advantages and practical limitation for the power-constrained simultaneous noise and input matching technique are explained. Besides, in this paper, the power gain of the LNA is improved by using simple positive feedback technique. The proposed LNAs are fabricated based on 0.18 μm CMOS technology for 5 GHz WLAN applications. Measurement results show power gain of 18 dB, NF of 1.5 dB, IIP3 of -5 dBm while dissipates current of 4 mA from supply voltage of 2.5 V.

2. LNA DESIGN

2.1 Power-Constrained Simultaneous Noise and Input Matching Technique

A simple cascode inductive degeneration LNA as shown in Fig. 1a is one of the most popular topology due to its wide bandwidth, high gain, and high reverse isolation. In the given example, the selection of the cascode topology simplifies the analysis as well, as the gate-drain capacitance can be neglected [4]. Fig. 1-(b) shows the simplified small-signal equivalent circuit of the cascode amplifier for the noise analysis including the intrinsic transistor noise model. Assume that in Fig. 1-(b), the parasitic resistances of gate, body, source, and drain of transistor are neglected as well.

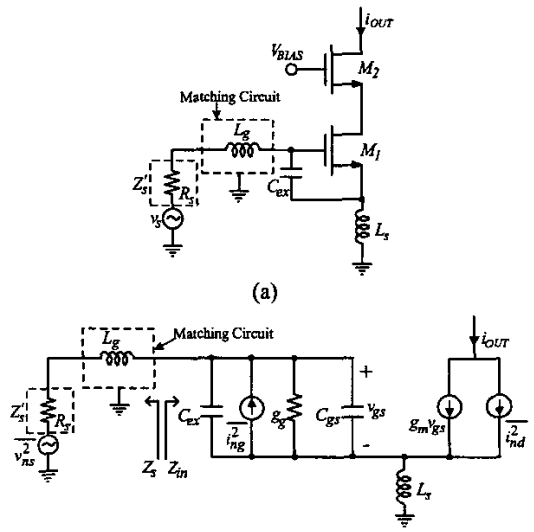

Fig. 1. (a) Small-signal equivalent circuit of the simple cascode (a), proposed LNA (b)

In Fig. 1-(a), the mean-squared channel noise current is given by [7]

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f \tag{1}$$

Here g_{do} is the drain-source conductance at zero drain-source voltage V_{DS}, k a Boltzmann constant, T absolute temperature and Δf bandwidth. The parameter γ has a value of unity at zero V_{DS} in long-channel devices, 2/3 in saturation and increases more than two in short-channel devices and/or at high V_{GS} and V_{DS}. The fluctuating channel potential due to channel noise current in (1) couples capacitive into the gate terminal, leading to a noisy gate current. As in [7], the mean-squared gate-induced noise current is

$$\overline{i_{ng}^2} = 4kT\delta_{eff} g_g \Delta f \tag{2}$$

where $g_g = \dfrac{\omega^2 C_{gs}^2}{5g_{d0}}$, $\delta_{eff} = \delta.\left(\dfrac{C_{gs}^2}{C_t^2}\right)$ and $C_t = C_{gs} + C_{ex}$

Here δ has a value of 4/3 in long-channel devices, whose

value is twice of γ. The value δ also increases in short-channel devices and at high V_{GS} and V_{DS}.

As shown in Fig. 1, the mean-squared output noise current by the source matching circuit is

$$\overline{i_{o,ns}^2} = \left|\frac{R_s}{D}\cdot g_m\right|^2 \cdot \overline{i_{ns}^2} \tag{3}$$

When the source admittance is

$Y_s = G_s + jB_s = \left(R_s + sL_g\right)^{-1}$, the mean squared noise current by source is $\overline{i_{ns}^2} = 4kTG_s\Delta f$

The mean-squared output noise current by the gate induced noise source are given by

$$\overline{i_{o,ng}^2} = \left|\frac{R_s + sL_g + sL_s)}{D}\cdot g_m\right|^2 \cdot \overline{i_{ng}^2} \tag{4}$$

Since the mean-squared output noise current by the channel noise source is changed by the feedback source inductance L_s, so that the expression is

$$\overline{i_{o,nd}^2} = \left|\frac{1+sC_{gs}(sL_g+sL_s)+sC_{gs}R_s}{D}\right|^2 \cdot \overline{i_{nd}^2} \tag{5}$$

where $D = 1+sC_t(sL_g+sL_s)+sC_tR_s+g_m sL_s)$ (6)

To consider the correlation between gate-induced and channel noise sources, the gate induced noise current is expressed as sum of uncorrelated and correlated portion. The mean-squared expression is

$$\overline{i_{ng}^2} = \overline{i_{ngu}^2} + \overline{i_{ngc}^2} = 4kT\delta g_g(1-|c|^2) + 4kT\delta g_g|c|^2 \tag{7}$$

The coefficient of cross-correlation between gate-induced and channel noise sources is c = 0.395j

Considering correlation, the total output noise current consists of the output current from source termination, gate-induced and channel noise sources. It is expressed as

$$\begin{aligned}\left|i_{o,total^2}\right|^2 &= \left|i_{o,ns}+i_{o,ng}+i_{o,nd}\right|^2 \\ &= \left|i_{o,ns}\right|^2 + \left|i_{o,ngc}+i_{o,nd}\right|^2 + \left|i_{o,ngu}\right|^2\end{aligned} \tag{8}$$

Noise factor can also be calculated as follows [2]

$$F = F_{min} + \frac{R_n\left|Y_s - Y_{opt}\right|^2}{G_s} \tag{9}$$

Here Y_s and Y_{opt} are source admittance and optimum source admittance, respectively.

Since the noise factor is defined as the ratio between total mean-squared output noise current and mean-squared output noise current due to input source only, therefore using (1)-(8), the noise factor is given expressed as

$$F = 1+\frac{1}{g_m^2R_s}\cdot\left\{\begin{array}{l}\gamma g_{d0}\cdot\left\{\begin{array}{l}\left[1+s^2C_t\left(L_g+L_s\right)\left(1+|c|\alpha\sqrt{\frac{\delta_{eff}}{5\gamma}}\right)\right]^2 \\ -\left(sC_tR_s\right)^2\left(1+|c|\alpha\sqrt{\frac{\delta_{eff}}{5\gamma}}\right)^2\end{array}\right\} \\ -\frac{\alpha\delta_{eff}}{5}\left(1-|c|^2\right)g_m\left(sC_t\right)^2\left(R_s^2-sL_g^2\right)\end{array}\right\} \tag{10}$$

The noise parameters are obtained by comparing (9) and solving the zero solutions after differentiating (10) with respect to R_s and L_g respectively. The noise parameters are given by (11) – (13)

$$F_{min} = 1+\frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{11}$$

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}}+j\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)}+\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \tag{12}$$

$$R_n = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m} \tag{13}$$

Note that, interestingly, as can be seen from (11) and (13), the minimum noise figure F_{min} and the noise resistance R_n are not affected by the addition of C_{ex}.

From Fig. 1-(b), the input impedance of the LNA is given by

$$Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_mL_s}{C_t} \tag{14}$$

As can be seen in (14), the source degeneration generates real part at the input impedance. This is important because there is no real part in the input impedance without degeneration while there is in the optimum noise impedance. Therefore, if not excessive, L_s helps to reduce the discrepancy between the real parts of the optimum noise impedance and the LNA input impedance. Furthermore, from (13), the imaginary part of Z_{in} is changed by sL_s, and this is followed by nearly the same change in Z_{opt} in (12), especially with advanced technology considering the value of c is higher than 0.4 (e.g., $c \approx 0.5$ with 0.25 μm technology), and α becomes lower than 1 [8].

Now, for the circuit shown in Fig. 1-(a), the condition that allows the simultaneous noise and input matching is

$$Z_{opt} = Z_{in}^* \tag{15}$$

From (11)-(14), (15) can be satisfied when the following conditions are met:

$$\mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_s] \quad (16) \qquad \mathrm{Im}[Z_{opt}] = \mathrm{Im}[Z_s] \quad (17)$$

$$\mathrm{Im}[Z_{in}] = -\mathrm{Im}[Z_s] \quad (18) \qquad \mathrm{Re}[Z_{in}] = \mathrm{Re}[Z_s] \quad (19)$$

Those conditions are re-expressed as follows

$$\frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)}+\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} = \mathrm{Re}[Z_s] \tag{20}$$

$$\frac{j\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)}+\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - sL_s = \mathrm{Im}[Z_s] \tag{21}$$

$$sL_s + \frac{1}{sC_t} = -\mathrm{Im}[Z_s] \quad (22)$$

$$\frac{g_m L_s}{C_t} = \mathrm{Re}[Z_s] \quad (23)$$

As mentioned above, for the advanced CMOS technology parameters, (21) is approximately equal to (22). Therefore, (22) can be dropped, which means that for the given value of L_s, the imaginary value of the optimum noise impedance becomes approximately equal to that of the input impedance with opposite sign, $\mathrm{Im}[Z_{in}] \approx -\mathrm{Im}[Z_s]$ automatically. Now then, the design parameters that can satisfy (20), (21), and (23) are V_{GS}, W (or C_{gs}), L_s, and C_{ex}. Since there are three equations and four unknowns, (20), (21), and (23) can be solved for an arbitrary value of Z_s, by fixing the value of one of the design parameters that can be the power dissipation or V_{GS}. Another word this LNA design optimization technique allows to design simultaneous noise and input matching at any given amount of power dissipation.

The limitation of the power-constrained simultaneous noise and input matching technique is high value of noise resistance. As can be seen in (13), the noise resistance, R_n, of the proposed topology is not affected by the addition of C_{ex}, but only the function of g_m. Therefore, the small transistor size and low power can lead to very high R_n. High R_n can be a serious limitation for the practical high yield LNA design therefore be careful when apply this technique.

The qualitative description of the proposed design process would be as follows. First choose the DC bias, V_{GS}, for example the bias point that provides minimum F_{min}. Then, choose the transistor size, W, based on the power constraint, P_D. Now choose the additional capacitance, C_{ex}, as well as the degeneration inductance, L_s, to satisfy (20) and (23) simultaneously. The value of C_{ex} should be chosen considering the compromise between the size of L_s and the available power gain. As described before, large L_s can lead to the increase in F_{min}, while large C_{ex} leads to the gain reduction due to the degradation of the effective cut-off frequency of the composite transistor (transistor including C_{ex}). At this point, the simultaneous noise and input matching is achieved. As the last step, if there exists any mismatch between Z_{in} and Z_s', as shown in Fig. 1 (b), an impedance matching circuit can be added.

2.2 Gain Enhancement Technique and Proposed LNA

One of the techniques that help to improve the gain of amplifier is using positive feedback. There is a widespread belief that systems, which use positive feedback, should be avoided because their sensitivity to process and environmental variations may cause them to become unstable [9]. This misconception is founded in the fact that standalone amplifiers using partial positive feedback do become unstable if too much positive feedback is applied [10]. In this work, to improve the gain of LNA, the simple positive feedback is applied. The positive feedback is implemented by simple poly resistor, R_{ex}, as shown in Fig. 2. The value of R_{ex} has to high enough in order to transistor M_2 operates in the saturation mode. The high value of R_{ex} will apply moderate amount of positive feedback to maintain the stability condition. Note that the noise contribution of R_{ex} on the overall NF of circuit can be neglected because which is used in the second stage. In Fig. 2, L_s and C_{ex} are used for simultaneous noise and input matching and L_g is for matched 50 Ω input impedance. The output-matching network is implemented by L_o and C_o. L_o is implemented by off-chip inductor that gives the higher linearity compare to the case of using on-chip [11].

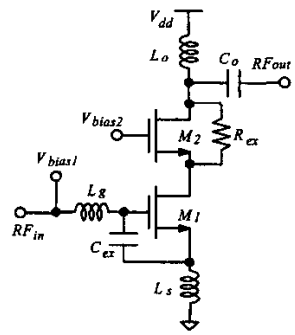

Fig. 2 The proposed LNA

3. Experiment Results

To demonstrate the potential of power-constrained simultaneous noise and input matching optimization technique, the current dissipation of the proposed LNA is fixed at 4 mA. Two LNA versions are designed based on 0.18 μm CMOS technology, the first circuit is simple cascode inductive degeneration topology and the second one is using the addition capacitor C_{ex}. The compared measurement results are shown in Fig. 3. As can be shown in Fig. 3, by using the power constrained simultaneous noise and input matching, the NF is lower than that for the case of simple cascode inductive degeneration. The improvement in NF can be understood as the satisfying the noise-matched condition. To make sure the effect of R_{ex} on the power gain performance of LNA, the third LNA version is fabricated which includes C_{ex} and R_{ex} as shown in Fig. 2. The compared measurement result of power gain is shown in Fig. 4. As can be seen in Fig. 4, the power gain is improved by 2 dB. Fig. 5 shows the measured result of input third order intermodulation product of the proposed LNA. The proposed LNA has power gain of 18 dB, NF of 1.5 dB at 5.25 GHz and IIP3 of –5 dBm. The microphotograph of the three circuits is shown in Fig. 6.

4. Conclusion

Very simple and insightful sets of noise parameter expressions for the power-constrained simultaneous noise and input matching LNA design optimization technique is newly introduced Based on the noise parameter expressions, the design principle, advantage, and the limitation for the power-constrained simultaneous noise and input matching technique are explained. High gain without increasing power dissipation can be obtained by using simple positive feedback technique. The positive feedback is implemented by using the resistor connecting from the

drain terminal of the cascode transistor to that of the common source transistor. In order to estimate the effect of C_{ex} and R_{ex}, three LNA circuits are fabricated based on a 0.18μm CMOS technology. Measured results of the proposed LNA at 5.25 GHz show the power gain of 18 dB, noise figure of 1.5 dB, and IIP3 of -5 dBm while dissipating 4 mA from supply voltage of 2.5 V.

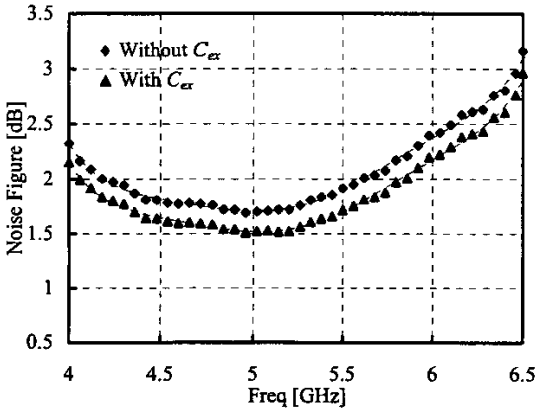

Fig. 3. NF comparison: with and without C_{ex}

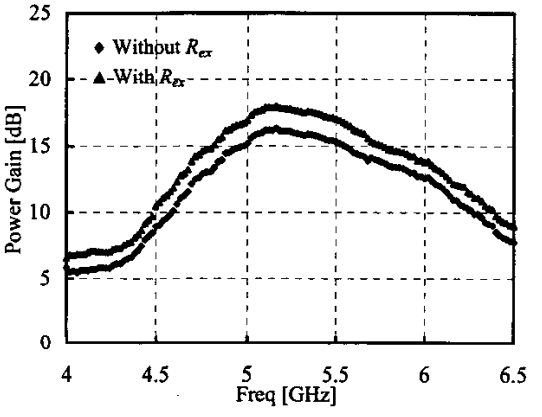

Fig. 4. Power gain comparison: with and without R_{ex}

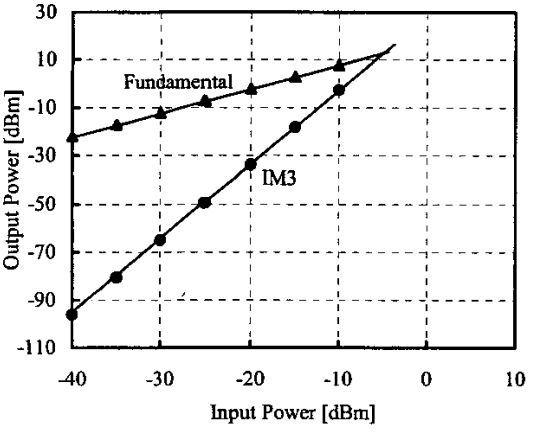

Fig. 5. IIP3 of the proposed LNA

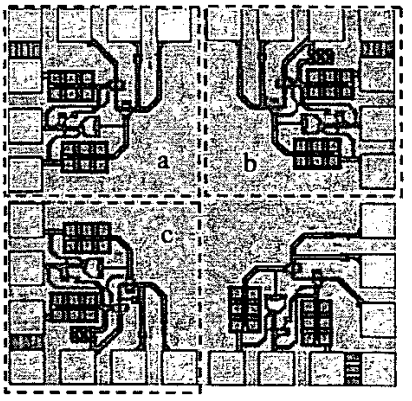

Fig.6. Die photos of simple cascode (a), simple cascode with C_{ex} (b) and Proposed LNA (c)

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