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dB-Linear V-I Converter Using Composite NMOS Transistor

QUOC-HOANG DUONG, TRUNG-KIEN NGUYEN, HOANG-NAM DUONG AND SANG-GUG LEE

Abstract -- **A new CMOS exponential V-I converter (EVIC), based on Taylor's concept and using NMOS transistor, is presented in this paper. The proposed-modified Taylor series expansion is used to extend the dB-linear output current range. In a 0.25 μm CMOS process, the simulations show more than 22 dB output current range and 17 dB linear range with the linearity error less than ± 0.5 dB. The power dissipation is less than 0.3 mW with ± 1.5 V supply voltage. The proposed EVIC can be used for the design of an extremely low-voltage and low-power variable gain amplifier (VGA) and automatic gain control (AGC).**

Index terms -- **dB-Linear, exponential function, Converter, VGA, and AGC.**

I. INTRODUCTION

Low-power VLSI circuits are of particular interest in the field of microelectronics. The advances in the CMOS VLSI technology and the market demand for portable and mobile electronic equipment lead to increasing reductions on the power consumption. With advances in CMOS digital signal processing technique, CMOS became a main fabrication process for analog and mixed signal processing circuitry.

The dB-linear V-I converter is the key component for the design of VGAs and AGCs, which are widely used in analog signal processing; such as in hearing aids, disk drive, and telecommunication applications [1-3]. This converter is not available in CMOS technology since CMOS transistors follow a square-law charac-teristic in strong inversion. However, it is easily obtained in bipolar technology. Unfortunately, the bipolar techniques for VGAs and AGCs are not compatible for monolithic low voltage CMOS-based analog and mixed-signal circuits. Moreover, good performance bipolar transistors are not readily available in the conventional technology, while BiCMOS solution may not be cost effective. Although CMOS transistors exhibit exponential characteristics in weak inversion, except the very low-speed application, the circuit could be too slow.

Since there is no intrinsic logarithmic MOS device operating in the saturation region for CMOS technologies, two following methods to generate the exponential characteristics are used. The first one is based on a "pseudo-exponential" generator [1-4], while the other one uses Taylor series expansion for realizing the exponential characteristics [5-7].

By applying the Taylor concept, the EVIC can be implemented by using the composition of a V-I squarer circuit, a linear V-I converter and a constant bias current [5,6], or by using composite NMOS transistors [7]. However, these previously reported EVICs tend to show very small dB-linear variation of the output current (less than 15 dB with a linearity error less than ± 0.5 dB) [6,7]. Moreover, EVICs in [6,7] are not power efficient (≅ 0.9 mW) [6,7]. Although the circuit in [7] is rather simple, the reported dB-linear range and the input voltage dynamic range are restricted.

To overcome these difficulties, this paper presents a new and very simple EVIC using the composite NMOS transistor and the Modified Taylor series expansion to increase the dB-linear output current range as well as the differential input swing. The Simulation results will be given to verify the validity of this approach.

II. BASIC CONCEPT

According to the Taylor's series expansion, a

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general exponential function can be expressed as

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \ldots + \frac{a^n}{n!}x^n + \ldots \quad (1)$$

where a and x are the coefficient and the independent variable, respectively. Obviously, for $|ax| \geq 1$ the exponential function cannot be implemented by a low-order polynomial. The exponential function can be approximated with small deviation from the ideal exponential function by eliminating the higher order terms for $|ax| << 1$. By neglecting the terms higher than second-order in Eq. (1), the approximation equation can be given as.

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (2)$$

for $|ax| \leq 1$, Eq. (2) provides 14 dB variation and 12 dB-linear variation with the error less than ± 0.5 dB as shown in Fig. 1 by the dashed line.

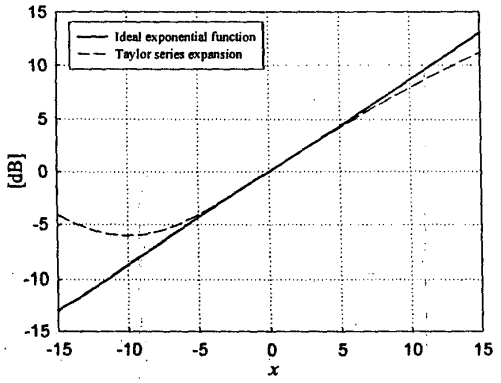

Fig. 1. Comparison between the Ideal exponential function and the approximation function in Eq. (2).

III. PROPOSED IDEA

Typically, the "pseudo-exponential" generator is of particular interest since it provides larger dB-linear range (about 15 dB with the error < ± 0.5 dB as shown in Fig. 2 by the diamond's symbol line) compared to that of the other one. Unfortunately, the "pseudo-exponential" method in which the exponential function is expressed as: $\exp(2x) \cong (1+x)/(1-x)$ is difficultly implemented due to the requirement of division function. Differently, the approximation function based on Taylor series expansion follows a squaring function and comprises only additive functions as shown in Eq. (2). Moreover, as mentioned previously, the CMOS transistors have square-law characteristics in strong inversion. Consequently, the approximation based on Taylor series expansion can be easily implemented in CMOS technology. Although this method results in small dB-linear output current range, its simplicity still attracts designers to design the dB-linear V-I convert simply by using building blocks [3], or by using composite NMOS transistors [4]. This paper proposed a new modified Taylor series approximation as follows:

$$e^{ax} \cong k + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (3)$$

For k = 1, Eq. (3) actually becomes Eq. (2) which provides 14 dB amplitude variation, and 12 dB range with linearity error less than ± 0.5 dB for $|x| \leq 1/a$ as shown in Fig. 1 by the dashed line.

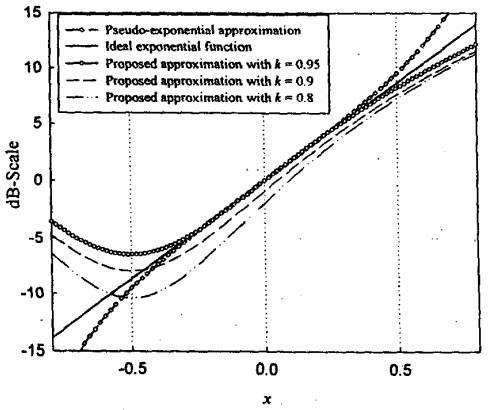

Fig. 2. Plot of various functions on a decibel scale

Using Matlab simulation tool for simulating Eq. (3), the results show that for k slightly less than 1, the approximation in Eq. (3) shows higher dB-linear range than that of Eq. (2). As shown in Fig. 2 by the o'symbol line for k = 0.95, the dB-linear range is extended to about 15 dB with linearity error less than ± 0.5 dB which is almost the same as the performance of the "Pseudo-exponential" approximation. While k decreases, the dB-linear ranges can be extended to even much higher values as depicted in Fig. 2 for k = 0.9 and 0.8. The proposed idea in this paper opens up a new possibility for designers to take full advantages of the approximation method based on Taylor series expansion.

IV. CIRCUIT DESCRIPTIONS

The circuit design is based on the composite NMOS transistor [8] as shown in Fig. 3 with the assumption that transistors M_1 and M_2 are identical and operating in saturation region without body

effects. The drain currents of M_1 and M_2 follows the below equation:

$$I_{d1} = \frac{K_n}{2}(V_{in} - V_Y - V_{tn})^2$$

$$I_{d2} = \frac{K_n}{2}(V_Y - V_1 - V_{tn})^2$$

where $K_n = \mu C_{ox} W/L$ is the process parameter and V_{tn} is the threshold voltage, V_{in} is the input voltage. The subtraction between the above two currents leads to the following equation

$$I_{d1} - I_{d2} = \frac{K_n}{2}(V_{in} - V_Y - V_{tn})^2 - \frac{K_n}{2}(V_Y - V_1 - V_{tn})^2 \quad (4)$$

In order to apply Eq. (3), a tunable bias current, $I_0 = K_n V_0^2/2$, is added to the Eq. (4). The voltage V_1 is equal to the negative supply voltage, V_{ss}, from Eq. (4) the following equation applies:

$$I_{out} = I_{d1} - I_{d2} + I_0 \quad (5)$$

$$= \frac{K_n}{2}\left[V_0^2 + (2V_{in} - V_{ss})(2V_Y + V_{ss}) - 2(V_Y + V_{in})V_{in} + V_{in}^2\right]$$

$$= \frac{K_n}{2}\left[V_0^2 + (2V_{in} - V_{ss})(2V_Y + V_{ss})\right] \times$$

$$\times\left[1 - \frac{2(V_Y + V_{in})}{\left[V_0^2 + (2V_{in} - V_{ss})(2V_Y + V_{ss})\right]}V_{in} + \frac{V_{in}^2}{\left[V_0^2 + (2V_{in} - V_{ss})(2V_Y + V_{ss})\right]}\right]$$

Obviously, the output current, I_{out}, is a squaring function of V_{in}. The I_{out} as an exponential approximation function of V_{in} as in Eq. (3) can be obtained by adjusting I_0 as well as V_0^2. From Eq. (5), the approximation as in Eq. (2) is achieved for I_0 satisfying the following equation

$$I_0 = \frac{K_n}{2}V_0^2$$

$$= \frac{K_n}{2}\left[2(V_Y + V_{in})^2 - (2V_{in} - V_{ss})(2V_Y + V_{ss})\right] \quad (6)$$

The proposed dB-linear V-I converter for realizing Eq. (5) is shown in Fig. 4. In Fig.4, the transistors M_1 and M_2 form the composite NMOS transistor, the transistor M_9 copies the drain current of M_1. This current is added to the bias current, I_0, and is subtracted to the drain current of M_2 to form the output current as in Eq. (5). For the proposed converter to operate properly, all of the transistors should be biased in the saturation region. Theoretically, the input range of this circuit should be

$$V_Y + V_{tn1} \le V_{in} \le V_{dd} - |V_{tp4}| + V_{tn1} \quad (7)$$

where V_{tn1} and V_{tp4} are the threshold voltage of transistors M_1 and M_4. As shown in Eq. (7), the smaller the V_Y the lager the input voltage swing is. Therefore, the V_Y is chosen closely to $V_{ss} + V_{tn1}$ so that very wide input dynamic range is achieved. In Fig. 4, the transistor M_3-M_6 are two current mirrors. Since $I_{d3}=I_{d4}=I_{d1}$, no current will flow from node X to node Y, and the transistors M_7 and M_8 force the V_Y closely to $V_{ss} + V_{tn1}$. In this paper, the V_Y is set to – 1 V, and the V_{tn1} and V_{tp4} are respectively 0.45 V and –0.6 V, the input range is therefore from -0.55 V to 1.35 V.

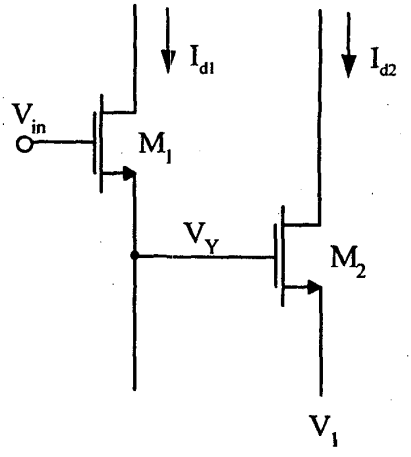

Fig. 3. Composite NMOS transistor

As shown in Fig. 4, the transistor M_7 and M_8 are NMOS and PMOS transistor, respectively. The M_7 has very small size so that the current flowing through these two transistors is rather small. Consequently, the total power consumption is reduced.

V. SIMULATION RESULTS

The aspect ratios of all transistors in Fig. 4 are listed in Table 1. The simulation results are shown in Fig. 5. In Fig. 5, as V_{in} varies from –0.55 to 1 V, and I_0 = 14 μA, the approximation as in Eq. (2) is achieved with 12 dB range and the linearity error is less than ± 0.5 dB. By reducing I_0, the dB linear ranges are increased as depicted in Fig. 5 by the dash-dotted, dash-dot-dotted, and o'symbol lines. The o'symbol line which corresponding to I_0=6 μA, shows 17 dB linear range with linearity error less than ± 0.5 dB over large input voltage range from –0.55 V to 0.8 V. When V_{in} > 0.8 V, the simulation result deviates from the ideal line due to neglecting the higher order terms in Eq. (1).

VI. CONCLUSION

A new dB-linear V-I converter based on the proposed modified Taylor series expansion is presented with the use of composite NMOS transistor. High dB-linear range (17 dB) over large input voltage swing (from –0.55V to 0.8V) is obtained with extremely low power consumption. The proposed circuit can operate at rather low supply voltage less than 3 V. However, the input voltage swing is proportional to the supply voltage. The circuit is compact and power-efficient. It could be used in the design of extremely low-voltage low-power VGA and AGC.

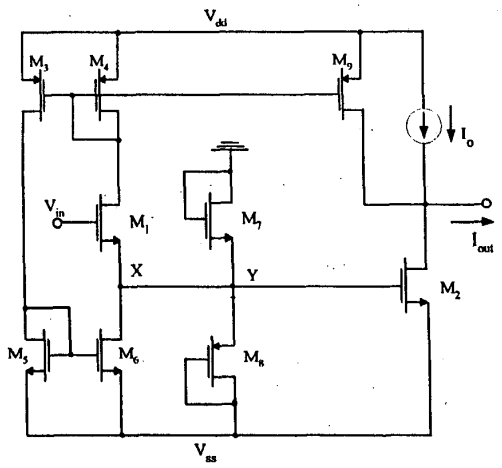

Fig. 4. The complete proposed exponential V-I converter using composite NMOS transistor.

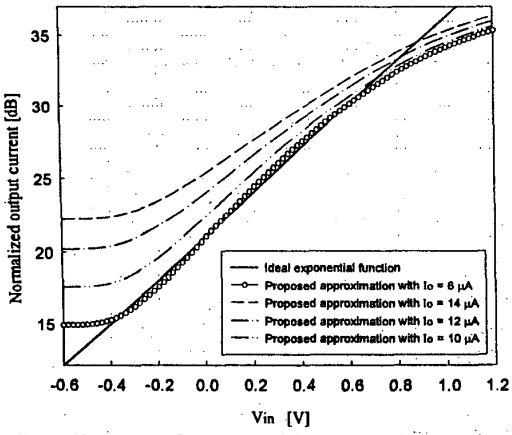

Fig. 5. The I-V performance of the proposed EVIC shown in Figure 4

TABLE I
ASPECT RATIOS OF TRANSISTORS IN FIG. 4.

Transistors	Aspect ratios μm/μm
M_1, M_2	1/4
M_3, M_4, M_5, M_6, M_9	4/1
M_7	2/1
M_8	40/1

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