All CMOS Current-Mode Exponential Function Generator

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Abstract-**This paper proposed an ultra low-voltage low-power all CMOS current-mode exponential function circuit. The design of the circuit is based on Taylor series expansion for realizing the exponential characteristic and composed of MOS transistors operating in the saturation region. The advantages of the circuit are that its input range can be tuned by adjusting the biased current and its output current presents a very low temperature coefficient. The simulations, based on a 0.25 μm CMOS process, show a 20 dB linear output current range and a 15 dB-linear range with the linearity error less than ± 0.5 dB at 1.25V supply voltage. The proposed circuit could be used for the design of an extremely low-voltage low-power automatic gain control (AGC) and variable gain amplifier (VGA).**

***Keywords*- dB-Linear, Exponential function, V-I converter.**

1.Introduction

Among the mostly used circuits in mixed signal VLSI circuits, are VGAs and AGCs, which play an important role in telecommunications applications, medical equipment, hearing aid, disk drives and others [1-3]. The key component for the design of VGAs and AGCs is the exponential function generator. Unfortunately, there is no intrinsic logarithmic MOS device that operates in saturation region, which is necessary to design such generators. Although CMOS transistors present exponential characteristics in weak inversion, their performance is poor in terms of speed and bandwidth. Though the exponential functions can be easily obtained in bipolar technology, bipolar techniques for AGCs and VGAs are not compatible for monolithic CMOS-based analog and mixed-signal circuits. On the other hand, BiCMOS technology may not be cost-effective. Consequently, to generate the exponential characteristics, a "pseudo-exponential" generator can be implemented [1-4]. Alternatively, the Taylor series expansion can also be used for realizing the exponential characteristics [5-8].

The Taylor series approximation can be easily implemented as in [6] where four current-mode building blocks are used to constitute the exponential approximation function. In this paper, the above current-mode building block is also used, however, only one block is used to form the exponential approximation function instead of four blocks as in [6] such that the proposed circuit is rather compact and the power consumption is reduced drastically (almost four times compared to [6]) at ultra low voltage applications. And, by using the proposed approximation based on Taylor concept, the proposed circuit can achieve high dB-linear out current range.

2.Basic concept and Proposed approximation function

A general exponential function, based on the Taylor series expansion, can be expressed as

$$\exp(ax) = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \ldots + \frac{a^n}{n!}x^n + \ldots \quad (1)$$

Mathematically, the exponential function can be approximated with small deviation by eliminating the high order Taylor series for $|ax| << 1$. The major deviation of exponential function results from the ignored orders of the Taylor series, the absolute range of x (≤ 1 or ≥ 1) and the coefficient "a". Obviously, for $|ax| > 1$, the exponential function cannot be implemented by a low-order polynomial.

The approximation equation, obtained by eliminating the higher order terms of Eq. (1) with small error for $|ax| << 1$, can be written as

$$\exp(ax) \cong 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (2)$$

The primary drawback of this method is that the region over which the above equation is valid is restricted to $|x| \leq 1/a$. Beyond this region, the difference between the original exponential function and the approximation function will be more than 2.6 dB. The comparison between the ideal exponential function and the approximation equation is depicted in Fig. 1 for $a = 1$ by the solid and o'symbol curves, respectively. As shown in Fig. 1, for $|x| << 1/a = 1$, the ideal exponential is closed to the approximation, otherwise the deviation between them is increased. For $|x| \leq 1/a$ the approximated function provides 14 dB amplitude variation, and the linearity error is less than ± 0.5 dB within 12 dB.

Typically, the "pseudo-exponential" approximation is of particular interest since it provides larger dB-linear range (about 15 dB with the error < ± 0.5 dB as shown in Fig. 1 by the dash-dotted curve) compared to that of the Taylor based approximation. However, the "pseudo-exponential" generator in which the exponential function is expressed as: $exp(2x) \cong (1+x)/(1-x)$ is difficultly implemented due to the requirement of division function (i.e. $(1+x)/(1-x)$). Since, MOS transistors have square law characteristic in saturation region, the Taylor approximation, which follows a squaring function and comprises only additive functions as shown in Eq. (2), is easily

implemented. Although this method results in small dB-linear output current range, its simplicity is still attractive. The comparison between the performances of these two methods is shown in Fig. 1.

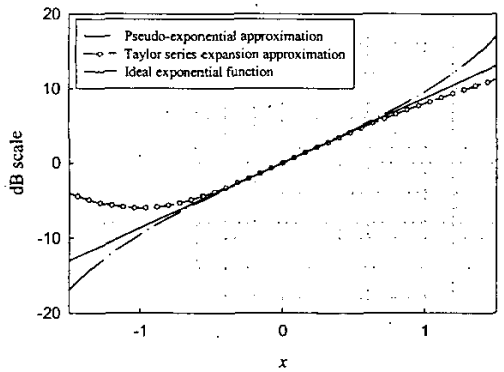

Fig 1. Plots of various functions on dB-scale

This paper proposed a new modified Taylor series approximation as follows:

$$f(ax) \cong k + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \qquad (3)$$

For k = 1, Eq. (3) actually becomes Eq. (2).Using Matlab simulation tool for simulating Eq. (3), the results show that for k slightly less than 1, the approximation in Eq. (3) shows higher dB-linear range than that of Eq. (2). As shown in Fig. 2 by the o'symbol line for k = 0.95, the dB-linear range is extended to about 15 dB with linearity error less than ± 0.5 dB. While k decreases, the dB-linear ranges can be extended to even much higher values as depicted in Fig. 2 for k = 0.9 and 0.8.

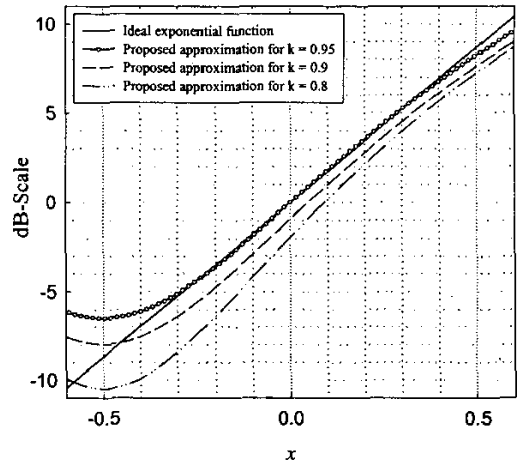

Fig 2. Plots of Eq. (3) for various k on dB-scale

from Eq. (2), the approximation function can be written as

$$\exp(ax) \cong (1/2)\left[1 + (1 + ax)^2\right] \qquad (4)$$

and the Eq. (3) can also be written as

$$f(ax) \cong (1/2)\left[(2k-1) + (1 + ax)^2\right] \qquad (5)$$

the circuit implementation of Eq. (5) will be discussed in section 3.

3. Circuit implementation

3.1 Circuit design

In this section, all transistors are in saturation region. The square-law behavior for the current-voltage relationship of the MOS transistor in saturation is assumed as

$$I_d = K(V_{gs} - V_t)^2 \qquad (6)$$

Considering the circuit in Fig. 1 (b), the drain currents of transistors M5 and M6 are given as

$$I_{d,M5,6} = K(V_{gs,M5,6} - V_t)^2 \qquad (7)$$

It is shown from [9] that the output current, $I_{out} = I_{d,M5} + I_{d,M6}$ of the circuit in Fig. 1 (b) can be given as

$$I_{out} = \frac{1}{2}K(V_2 - 2V_t)^2 + \frac{(I_{d,M6} - I_{d,M5})^2}{2K(V_2 - 2V_t)^2} \qquad (8)$$

to simplify the expression, a current-controlled biasing circuit is introduced in Fig. 1 (a) [9] which supplies the sum voltage V_2. The relation between the control current I_0 and the voltage V_2 is given as [9]

$$I_0 = \frac{1}{4}K(V_2 - 2V_t)^2 \qquad (9)$$

from Eq. (8) and (9) we have

$$I_{out} = I_{d,M6} + I_{d,M5} = 2I_0 + \frac{I_{in}^2}{8I_0} \qquad (10)$$

where $I_{in} = I_{d,M6} - I_{d,M5}$ as shown in Fig. 1(b).

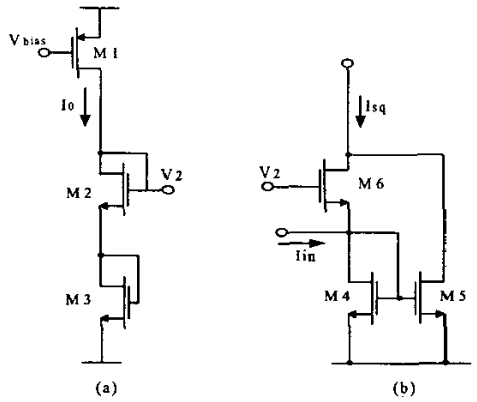

Fig. 3. (a) The bias circuit for the circuit in (b) (b) The current-mode building block for proposed exponential approximation.

Biasing with a current has the additional advantage of making the transfer function independent of process parameters and operating temperature.

In order to keep all devices in the ON state the input current must be restricted within the range

$$|I_{in}| < 4I_0 \tag{11}$$

The completed circuit implementations of the Eq. (3) are given in Fig. 4.

The output current, I_{out}, in Fig. 4 can be written as

$$I_{out} = 2I_0 + \frac{(I_{in} + k_1 I_0)^2}{8I_0} - k_2 I_0 \tag{12}$$

$$= \frac{k_1^2 I_0}{8}\left[\frac{8(2-k_2)}{k_1^2} + \left(1 + \frac{I_{in}}{k_1 I_0}\right)^2\right]$$

Similarly, the k_1 and k_2 have to satisfy the following condition

$$k_1 = \sqrt{8(2-k_2)} \tag{13}$$

then, from Eq. (12) we have the exponential approximation given as

$$I_{out} = \frac{k_1^2 I_0}{8}\exp\left(\frac{I_{in}}{k_1 I_0}\right) \tag{14}$$

The current, I_{out}, is thus an exponential approximation function of the input current I_{in}, where $a = 1/k_1 I_0$.

The Eq.(14) is valid in the range

$$|I_{in}| \le k_1 I_0 \tag{15}$$

out of this range, the deviation will be increased.

From Eq.(11), (13), (14) and (15) the k_1 should be

$$|I_{in} + k_1 I_0| \le |2k_1 I_0| \le 4I_0 \quad \Rightarrow \quad |k_1| \le 2 \tag{16}$$

From Eq. (12) one can also realize that by adjusting k_1 and k_2 in Eq. (12) can serve Eq. (5).

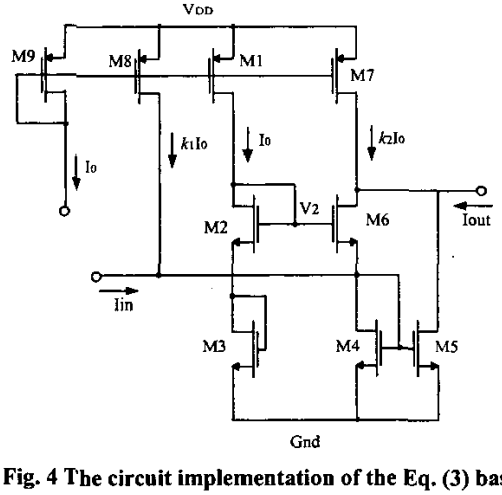

Fig. 4 The circuit implementation of the Eq. (3) based on the current-mode block shown in Fig. 3

3.2 Circuit discussion

Considering Eq. (14), the range of the input current is a function of the bias current, I_0, as shown in Eq. (15) such that it is tunable by adjusting the I_0. The Eq. (14) is also multiplied by a constant, $k_1^2 I_0/8$, however, this constant only dedicates to a dB-axis shift and will not affect the exponential function.

Now, we consider the temperature stability of the circuit in Fig.4. As the temperature changes, assume that the bias current and the output current will be varied by $I_0 + \Delta I_0$, and $I_{out} + \Delta I_{out}$, respectively. From Eq. (6) the following equation applies

$$\frac{I_{out} + \Delta I_{out}}{I_{out}} = \left(1 + \frac{\Delta I_0}{I_0}\right)\exp\left[\frac{-\Delta I_0/I_0}{k_1 I_0\left(1 + \Delta I_0/I_0\right)}\right] \tag{17}$$

because $\Delta I_0/I_0 << 1$, the Eq. (17) can be simplified as

$$\frac{I_{out} + \Delta I_{out}}{I_{out}} = \frac{(1 + \Delta M)}{\exp[\Delta M/k_1 I_0]} \tag{18}$$

where $\Delta M = \Delta I_0/I_0$.

From Eq. (18), it is obvious that while the temperature changes, both of the numerator and denominator of Eq. (18) are together increased or decreases, such that the circuit in Fig. 4 is very insensitive to the temperature.

4. Simulation results

The feasibility of the proposed circuit was verified through simulation, using 0.25 μm CMOS process. The aspect ratios of transistor M7 in Fig. 4 is 58μm/1μm while the other transistors were 32μm/1μm. The proposed circuit operate at 1.25 V supply voltage. The constant, k_1, is chosen to be unity. Therefore, to satisfy the condition of exponential approximation, the constant, k_2, must be set to the value of 15/8. Consequently, the aspect ratio of M7 in Fig. 4 should be 60μm/1μm. Then, the proposed circuit will provide 14 dB linear range. In our simulations, the exponential approximation is achieved for the aspect ratio of M7, which is equal to 56μm/1μm. And, the simulation result is shown in Fig. 5 by the solid curve. By increasing the aspect ratio of M7, the constant k_2 is increased such that the dB linear range is extended to 20 dB range, and 15 dB-linear range with the linearity error less than ±0.5 dB as depicted by the dash-dot-dotted curve in Fig. 5.

Fig. 5 depicts the I-V characteristic of the circuit in Fig. 4 for I_0 = 15 μA, therefore, the input current dynamic range is from –15μA to 15 μA.

Also, the input dynamic range of the proposed circuit can be tuned by the bias current I_0 as shown in Fig. 6. As depicted in Fig. 6 by the solid curve, the bias current is equal to 5 μA so that the dynamic range is from –5 μA to 5μA.

The proposed circuit consumes very low power that depends on the bias current, I_0, as summarized in table. 1.

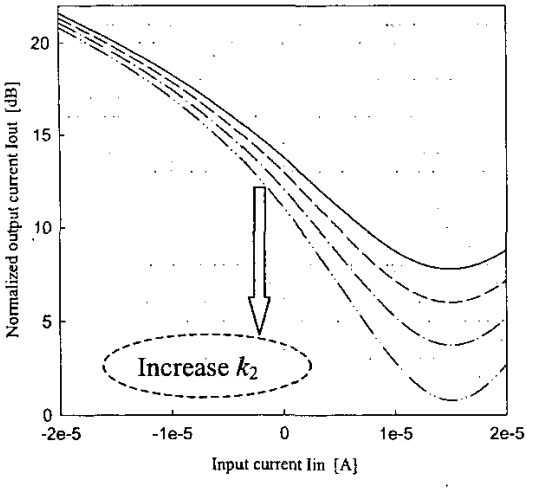

Fig. 5 The I-V characteristic of the proposed circuit shown in Fig. 4 for different ratios of k_1/k_2.

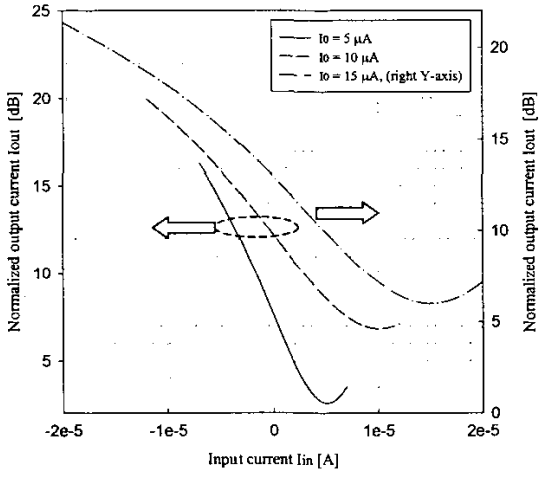

Fig. 6 The I-V performances of the circuit shown in Fig. 4 for various bias current I_0.

Table 1. The power consumption verses I_0 of the circuit in Fig. 4 with 20 dB linear output current range.

I_0 [μA]	2	5	10	15
Current dissipation [μA]	11	30	50	80

5. Conclusions

The current-mode exponential function generator has been introduced in this paper, based on the proposed modified Taylor series expansion and the square-law characteristics of MOS transistors in saturation. The proposed circuit uses only one current-mode building block compared to [6] such that the circuit is rather compact and the power dissipation is extremely low as summarized in Table. 1. The lowest power consumption can be less than 15 μW from 1.25 V supply voltage, while achieve 20 dB linear output current range and 15 dB range with the linearity error less than ±0.5 dB. The proposed circuit has its input current dynamic range tuned by the bias current I_0. Another advantage of this circuit is that it is very independence on the temperatures. The proposed circuit could be used for the design of an extremely low-voltage low-power AGC and VGA.

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