A 900MHz LOW VOLTAGE LOW POWER HIGHLY LINEAR MIXER FOR DIRECT-CONVERSION RECEIVERS

Moon-Su Yang, Hye-Ryoung Kim, Sang-Gug Lee

Information and Communications University, DaeJeon, Korea

ABSTRACT

This paper presents a 900MHz low voltage, low power down-conversion mixer with high linearity for direct-conversion receivers. As a way to improve the third-order linearity, this paper proposes a very linear transconductance amplifier in which the size of the transistors is optimized to minimize the third-order intermodulation distortion (IMD3). A folded mixer topology is used in the designed mixer to enable the mixer to operate at low supply voltage. The design is based on a standard 0.25μm CMOS technology, and the simulation results show 15dBm of input IP3, 80dBm of input IP2, and –6.5dB of power conversion gain while dissipating a total current of 3mA from 1.25V supply.

1. INTRODUCTION

The demand for the low power, low cost, and small-size RF transceivers has been increasing with the extensive researches on transceiver architecture and RF circuit design. In the last few years, the popularity of direct conversion architecture has been dramatically increased because of the possibility for the low power, low cost, and small-size one-chip transceiver [1], [2].

In implementing the RF transceivers, the low power consumption is one of the challenging requirements due to the battery lifetime. As a way to achieve low power consumption, many reported works have used a very low supply voltage [4], [6], [7], [8].

In addition, the down-conversion mixer is the key building block in a receiver system because it dominates the system linearity and noise figure, and determines the performance requirements of its adjacent blocks. Among many proposed active mixers, the Gilbert-cell mixer has been widely used due to the LO suppression at the output. The conventional Gilbert-cell mixer, however, is not suitable for low voltage operation because of the stack of the three saturated transistors. Besides, the direct-conversion mixer is required to use a resistor as the output load instead of reactive elements. In this case, the increase of the bias current of the transconductance amplifier in the conventional Gilbert-cell mixer results in the reduction of the output load resistance.

The down-conversion mixer is also required to provide a high linearity, low noise figure, and enough power conversion gain. The simultaneous achievement on these requirements is very challenging task in the mixer design. Especially, the high linearity requirement is the most difficult one to achieve since the mixer is required to operate at a very low supply voltage dissipating very little power. In addition, the third-order linearity improvement is difficult with a typical differential pair generally used in a transconductance amplifier since it is bound to the tail current source.

In this paper, we propose a low voltage, low power down-conversion mixer with very low third-order intermodulation distortion (IMD3) for direct-conversion receivers. High linearity is achieved using a linear transconductance amplifier in which the size of the transistors is optimized to minimize the IMD3. The folded mixer topology is used to guarantee enough voltage headroom in the transconductance amplifier under the low supply voltage.

2. LINEAR TRANSCONDUCTANCE AMPLIFIER DESIGN

Figure 1 shows a cross-coupled differential transconductance amplifier stage as reported in [3].

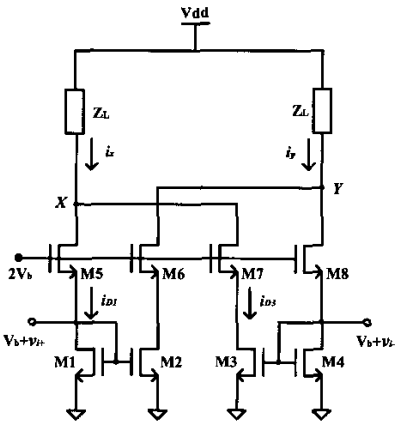

Figure 1. Cross-coupled transconductance amplifier

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In Figure 1, the transistors M1 through M4 and M5 through M8 are biased at V_B and $2V_B$, respectively, and all transistors are of the same size. The differential voltage input signals ($\pm v_i$) are applied to the diode-connected transistors M1 and M4. Each input voltage signal is converted into currents by two ways, the common source stage and the common gate stage. In Figure 1, the drain currents i_{D1} and i_{D3} are generated by the differential input with opposite polarity, and they are summed together at node X. Due to this combination, the transconductance amplifier shown in Figure 1 has the common mode rejection property. Provided that differential input signals are applied, this amplifier shows the differential-mode gain of $2g_mZ_L$, where g_m is the transconductance of the transistor M1, but common-mode gain of zero. This common-mode rejection characteristics can help suppress the effect of the common-mode input harmonics generated from the previous stage, thus the linearity is less affected.

In Figure 1, the differential output current of the transconductance amplifier i_o can be given by [3]

$$i_o = i_y - i_x = 2g_m v_i \tag{1}$$

As can be seen in equation (1), the differential output current i_o is linearly proportional to the input signal v_i as long as all transistors operate in saturation mode. Thus, equation (1) is valid for the input voltage range given by [3]

$$|v_i| \le 2\sqrt{\frac{I_D}{\mu_n C_{ox}\frac{W}{L}}} \tag{2}$$

where I_D is the DC current of each branch in Figure 1. Compared to the differential pair, the transconductance amplifier shown in Figure 1 shows $\sqrt{2}$ times larger input voltage range, which means the linearity is improved. Nonetheless, this transconductance amplifier has a limit in achieving high linearity due to the third-order intermodulation distortion (IMD3). In this paper, we propose the IMD3 minimization by optimizing the size of the transistors in the transconductance amplifier shown in Figure 1 as a way to achieve the better linearity.

The relation between drain current and the gate-source voltage of a transistor can be given by

$$i_d = g_m v_{gs} + \frac{1}{2}g_m' v_{gs}^{\ 2} + \frac{1}{6}g_m'' v_{gs}^{\ 3} + \cdots \tag{3}$$

In equation (3), the third order coefficient g_m'' is required to be as small as possible to improve the third-order linearity.

In Figure 1, the third-order component of the output current i_x consists of the third-order current components at the drain of the transistors M1 and M3, which are the third-order current components generated from the transistors M1 and M3, plus the third-order current component generated from the transistor M4 and then amplified by the transistor M3. Therefore, the third-order component of the current i_x can be given by

$$\begin{aligned} i_{x,3rd} &= i_{D1,3rd} + i_{D3,3rd} + g_{m3}\left(i_{D4,3rd}\cdot\frac{1}{g_{m8}}\right) \\ &= \frac{1}{6}\left(g_{m1}'' - g_{m3}'' + \frac{g_{m3}\cdot g_{m4}''}{g_{m8}}\right)v_i^{\ 3} \end{aligned} \tag{4}$$

Equation (4) shows that the IMD3 at node X can be cancelled out by optimizing the transconductance and the second derivative of the transconductance for the transistors M1 through M4. The simplest way is to change the size of the constituting transistors. Since the symmetry of the circuit is required for high second-order linearity, the size ratio of the transistors M1(M4) to M2(M3) is chosen as the design variable. Based on the simulation, the IMD3 of i_x decreases significantly as the transistor size ratio (M1/M2) increases. For the size ratio greater than 4.5, the linearity stays nearly the same, but the gain starts to decrease. Thus the size ratio of 4.5 is chosen for high linearity but least gain reduction.

Figure 2 shows the drain currents and the third-order coefficients at the drain of the transistor M1 and M3 when the transistors M1(M4) and M2(M3) are of the same size.

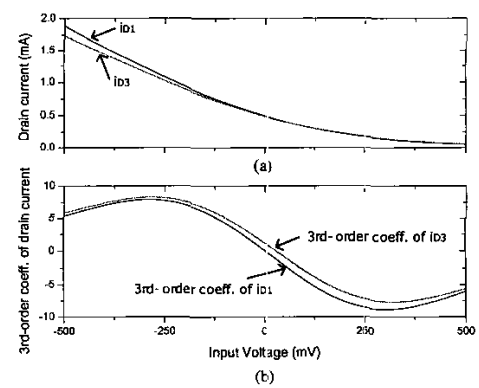

Figure 2. (a) Drain currents and (b) third-order coefficients when the transistors M1(M4) and M2(M3) are of the same size

As can be seen in Figure 2, the drain currents of each branch, i_{D1} and i_{D3}, and their third-order coefficients show quite similar behavior, respectively, and the third-order coefficients show large amplitude swing as the input voltage varies. With the similar behavior of the third-order coefficients of i_{D1} and i_{D3} for the input voltage, the overall third-order coefficient at the output current i_x

increases, which prevents the transconductance amplifier from achieving high linearity.

Figure 3 shows the drain currents and the third-order coefficients at the drain of the transistors M1 and M3 when the transistor size ratio (M1/M2) is 4.5.

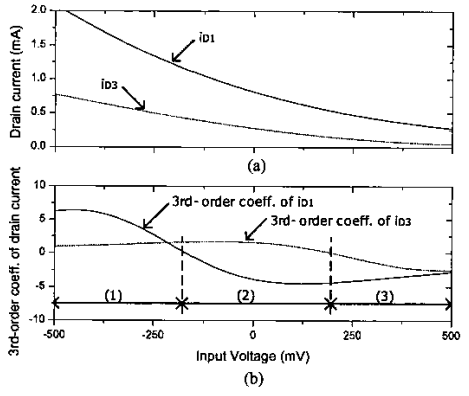

Figure 3. (a) Drain currents and (b) third-order coefficients when the transistor size ratio (M1/M2) is 4.5

As can be seen in Figure 3, the curves of the third-order coefficient of i_{D1}, i_{D3} are modified quite much with the increase of the size ratio, compared to the curves in Figure 2. In Figure 3, the increase of the size ratio of the transistors M1(M4) to M2(M3) not only reduces the magnitude of the third-order coefficient of i_{D3}, but also changes the location of its peak. Due to this change, the third-order coefficients of i_{D1} and i_{D3} no longer show the same behavior like the way shown in Figure 2. The input voltage range can be divided by three regions for the characteristics of the third-order coefficients of i_{D1} and i_{D3}, as can be seen in Figure 3(b). In the range of (2), the negative value of the third-order coefficient of i_{D1} is compensated with the positive value of the third-order coefficient of i_{D3}, which results in quite large reduction of the overall third-order coefficient. In the range of (1) and (3), although the polarity of the third-order coefficients of i_{D1} and i_{D3} is the same in each case, their absolute values are smaller than those in Figure 2, which leads to the better linearity.

3. HIGHLY LINEAR DOWN-CONVERSION MIXER DESIGN AND SIMULATION RESULTS

By utilizing the linear transconductance amplifier proposed in section 2, the highly linear down-conversion mixer is designed with standard 0.25μm CMOS technology for direct-conversion receivers. Due to the low supply voltage requirement, 1.25V supply, the folded mixer topology is used to provide enough voltage headroom in the transconductor stage. In Figure 4, a 900MHz differential RF signal and 910MHz differential LO signal are applied, and a 10MHz differential IF signal is obtained from the output. As can be seen from Figure 4, it is possible to control the DC current of the PMOS-based switching quad separately from the transconductor stage. The flicker noise in the direct-conversion mixer is one of the most critical problems, and it can be decreased as the DC current flowing the switching quad decreases according to [12]. Thus the amount of the current flowing the switching quad is designed to be very little as a way to reduce the flicker noise. This can help not only reduce the flicker noise but also increase the output load resistance R_L. The external inductors L_{ext} are used in the designed mixer instead of current source since the current source requires additional voltage headroom.

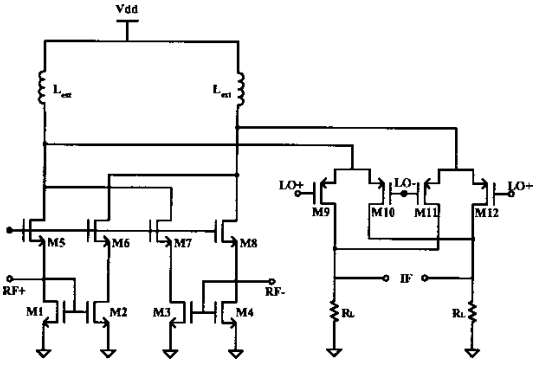

Figure 4. The highly linear down-conversion mixer

To demonstrate the advantage of the proposed transconductance amplifier, the linearity of the down-conversion mixers, adopting the previously reported transconductance amplifier [3] and the newly proposed, is estimated by simulation. Figure 5 shows the simulation results of each case.

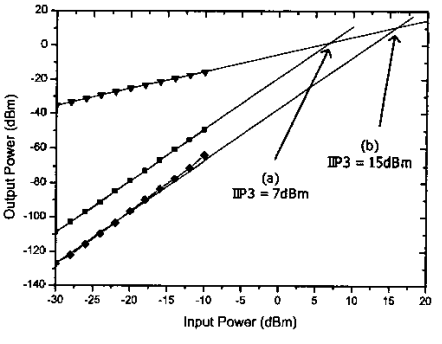

Figure 5. The simulated input referred IP3 of the down-conversion mixer with the transconductance amplifier (a) proposed in [3], (b) newly proposed in this paper

As can be seen in Figure 5, the transconductance amplifier proposed in [3] can provide good linearity compared to other conventional mixers. However, in the

newly proposed topology, much higher IP3, 15dBm at the input, can be achieved by optimizing the transistors size. The conversion gain of each case is almost the same. The proposed down-conversion mixer shows 15dBm of input IP3, 80dBm of input IP2, and –6.5dB of power conversion gain. Table 1 summarizes the simulated performance of the proposed down-conversion mixer and the results in the previously reported works.

Table 1. The simulated performance of the down-conversion mixer and comparison with other works

Parameters	This work	[4]	[5]	[6]	[7]	[8]	[9]
Supply Voltage (V)	1.25	1.5	2	1.2	0.9	1.2	2.5
Power Consumption (mW)	4	9	22	12	4.7	3	26
Input IP3 (dBm)	15	2	15	1	3.5	9.5	7
Conversion Gain (dB)	-6.5	9	-15	-10	2	-8	3

As can be seen from Table 1, the designed down-conversion mixer shows the outstanding value of input IP3 for the power consumption. Figure 6 shows the layout of the proposed down-conversion mixer drawn in 0.25μm technology.

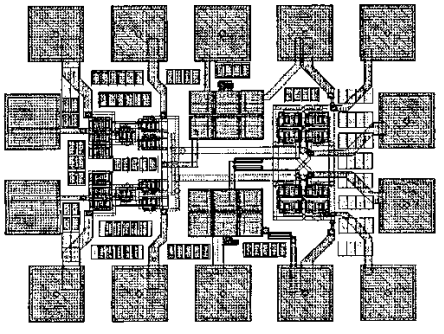

Figure 6. Layout of the proposed down-conversion mixer with a chip area of $700 \times 500 \mu m^2$

4. CONCLUSION

A low voltage, low power, and highly linear down-conversion mixer is proposed in this paper. High linearity is achieved by optimizing the size of the transistors in the cross-coupled transconductance amplifier. And the folded mixer structure is used to enable the mixer to operate at low supply voltage, 1.25V. From the simulation results, the designed mixer achieves 15dBm of input IP3, 80dBm of input IP2, and –6.5dB of power conversion gain, while dissipating a total current of 3mA from 1.25V supply.

5. ACKNOWLEDGEMENT

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6. REFERENCES

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