Overcome the phase noise optimization limit of differential LC oscillator with asymmetric capacitance tank structure

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Abstract **— A phase noise optimization method with asymmetric capacitance tank structure is proposed, which overcomes the shortcoming of the previous tank's L/C ratio optimization approach. The proposed phase noise optimization method with asymmetric capacitance tank structure can be applied to the complementary Colpitts(C-Colpitts) oscillator. The phase noise characteristics of the C-Colpitts explain well the excellence of asymmetric tank structure and which of the phase noise property is proved with simulation and experiment. Moreover, a differentially coupled C-Colpitts oscillator topology is proposed, which can achieve the better phase noise performance than that of the conventional differential LC oscillator.**

Index Terms **— CMOS, oscillator, phase noise, optimization, CMOS, complementary Colpitts.**

I. Introduction

With the advancement in sub-micron CMOS technology, CMOS technology becomes widely used in RFIC and the CMOS one-chip solutions integrated both of digital and RF circuits start to be provided. In these one-chip solutions, the differential LC oscillator is commonly adopted as local oscillator because of the better phase noise performance than that of ring oscillator in high frequency. With CMOS technology, to design and optimize the integrated low phase noise LC VCO has many technical obstacles such as noise of CMOS devices, low-Q inductor, substrate effect, supply limitation, etc. Thus, the strong research motivation is given in the design and optimization of integrated low phase noise LC CMOS VCO for mobile communication. According to recently published paper [1] for design optimization of LC VCO, the guideline of design optimization is provided and the limitation of the design optimization with high-Q spiral inductor [2] is described well.

The paper reports that when high-Q or high inductance of tank inductor is used, the maximum charge swing is not the achievable maximum charge swing because the oscillators oscillate in the supply voltage limited region in most case. As the solution of this aspect, the paper proposes the design optimization method through the proper selection of tank's L/C ratio (reduce additional tank inductance and increase tank capacitance). But the inductor with maximum Q-factor in wanted oscillation frequency cannot be used since reducing the additional tank inductance leads to the decrease in Q-factor of tank inductor. In other words, with this optimization approach, the best phase noise potential with maximum Q-factor inductor cannot be achieved.

In Section II, this paper proposes the phase optimization method using asymmetric capacitance tank structure. With proposed asymmetric capacitance tank structure, the phase noise can be optimized with the maximum Q-factor inductor in any oscillation frequency, which overcomes the shortcoming of the tank's L/C ratio optimization approach.

In Section III, the asymmetric capacitance tank structure is applied to the complementary Colpitts(C-Colpitts) oscillator[3] and the phase noise property and improvement of C-Colpitts is described. Based on the study of C-Colpitts oscillator, the differentially coupled C-Colpitts oscillator topology with asymmetric capacitance tank structure is introduced. In Section IV, reports the measurement results and concludes in Section V.

II. Asymmetric Capacitance Tank Structure

Fig. 1 shows the conventional differential LC oscillator and its symmetric capacitance tank structure. The Q-factor of LC tank circuit is dominated by the Q-factor of spiral inductor since the high-Q MIM capacitor is available in recent CMOS process technology. As shown in Fig. 1(b), the tank circuit has a parasitic resistance, R_s, only in the tank inductor. The tank capacitor of the differential LC oscillator is equivalently considered as the same two $2C_{tank}$ of capacitors connected to each end of the tank inductor as shown in Fig. 1(b), which can be called as symmetric capacitance tank structure.

Even though the supply voltage limited oscillation mainly comes from high-Q tank inductor, this supply-limited oscillation will not exist if the two drain nodes (D_1 and D_2) in Fig.1(a) do not experience the physical pushing within the supply voltage range. If the nodes in oscillator do not experience the supply pushing, the higher-Q inductor can be used and the better phase noise can be achieved.

The symmetric capacitance tank structure shown in Fig. 1(b) is the same with well-known π-matching network. It is known that π-matching network can freely control the Q-factor of matching network [4]. Fig. 2(a) and (b) shows

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π-resonant circuit and the equivalent LC parallel resonant circuit, where the series RLC branch shown from A and B nodes are changed the equivalent LR circuit. In π-resonant circuit, there exist two equivalent parallel LC resonant circuit as shown in Fig. 2(b) since Q_{left} and Q_{right} become different to the value of C_{left} and C_{right}.

The resonant frequency, ω_o, of π-resonant circuit is given as

$$\omega_o^2 = \frac{1}{L_{tank}C_{left}}\left(1+\frac{C_{left}}{C_{right}}\right) = \omega_{srl}^2\left(1+\frac{C_{left}}{C_{right}}\right)$$
$$\text{or} \quad = \frac{1}{L_{tank}C_{right}}\left(1+\frac{C_{right}}{C_{left}}\right) = \omega_{srr}^2\left(1+\frac{C_{right}}{C_{left}}\right) \quad (1)$$

where, ω_{srl} and ω_{srr} is the resonant frequency of the series RLC circuit shown from A and B nodes. The equivalent inductance (L_{eql} and L_{eqr}) of the equivalent LR circuit shown in Fig. 2(b) is given as

$$L_{eqr} = L_{tank}\left(1-\frac{1}{n_r^2}\right), \quad n_r = \frac{\omega_o}{\omega_{srr}} \quad (2)$$

$$L_{eql} = L_{tank}\left(1-\frac{1}{n_l^2}\right), \quad n_l = \frac{\omega_o}{\omega_{srl}} \quad (3)$$

where, n_l and n_r have relation as

$$\left(n_l^2-1\right)\left(n_r^2-1\right) = 1 \quad (4)$$

Finally, from (2), (3) and (4), Q_{left} and Q_{right} can be founded and $Q=Q_{left}+Q_{right}$ and $L_{tank}=L_{eql}+L_{eqr}$ in π-resonant circuit as shown in (5)

$$Q = Q_{left}+Q_{right} = \frac{j\omega_o\left(L_{eql}+L_{eqr}\right)}{R_s} = \frac{j\omega_o L_{tank}}{R_s} \quad (5)$$

From (5), Q_{left} and Q_{right} can be controlled freely by changing the value of C_{left} and C_{right} without changing the overall Q-factor of π-resonant circuit. Thus, by properly reducing the equivalent Q-factor (Q_{left} or Q_{right}), same with reducing the parallel equivalent resistance, in the nodes experiencing physical pushing within supply voltage such as D1 and D2 nodes in Fig.1(a), the supply limited oscillation can be avoided even though very high Q-factor of tank inductor is placed. In this case, the tank capacitance becomes asymmetric. This merit of asymmetric capacitance π-resonant circuit cannot be applied in the conventional differential LC oscillator since both of D1 and D2 nodes in Fig. 1(a) experience supply voltage pushing and asymmetric capacitance will increase the other equivalent Q-factor above the Q-factor with symmetric capacitance tank.

III. C-COLPITTS OSCILLATOR WITH ASYMMETRIC CAPACITANCE TANK STRUCTURE AND DIFFERENTIALLY COUPLED C-COLPITTS OSCILLATOR

The asymmetric capacitance tank structure discussed in previous chapter can be easily applied to the C-Colpitts oscillator shown in Fig.2(c). In Fig.2(c), C_g-L_{tank}-C_d becomes π-resonant circuit and the D node is the only supply voltage pushed node. Interestingly, the G node does not experience the physical supply voltage pushing during oscillation because the node is only connected to LC component. Thus, by reducing adequately the equivalent Q-factor (using the bigger C_d than C_g) of the series C_g-L_{tank} circuit shown from D node considering the supply voltage limitation, the supply pushed oscillation in C-Colpitts can be avoided with any Q-factor of tank inductor in any oscillation frequency.

The phase noise characteristic over the oscillation frequency of C-Colpitts oscillator can be derived from the $Q_{sr}=|j\omega_{sr}L_{tank}|/R_s$, $\omega_{sr}^2=1/L_{tank}C_g$ and $n=\omega_o/\omega_{sr}$ of the series C_g-L_{tank} resonant circuit. Where, Q_{sr}, ω_{sr} and R_s is the Q-factor, resonant frequency and the parasitic series resistance of L_{tank}, respectively. n is the index of oscillation frequency over the series resonance frequency.

From above relation, the phase noise equation of the C-Colpitts oscillator can be derived as

$$L(\Delta\omega) \approx \frac{2kT\Gamma_{rms}^2}{I_{DC}^2R_s^3C_{gs}^2\Delta\omega^2}\cdot\frac{\left[\left(n^2-1\right)^2+\left(\frac{n}{Q_{sr}}\right)^2\right]^4}{\left(n^2-1\right)^2\left\{\left[Q_{sr}\left(1-\frac{1}{n^2}\right)\right]^2+1\right\}^3} \quad (6)$$

In (6), the channel noise, 1/f noise, hot carrier effect and the non-linear characteristics of CMOS device are not considered.

To verify above argument, the simulation is carried out for the C-Colpitts oscillator shown in Fig. 2(c) using 0.35um CMOS technology with 2.0V and 2.93mA of supply voltage and dc bias current. The width of NMOS and PMOS transistor is 150μm and 300μm, respectively. The overall capacitance from gate-source is 1.645pF, which includes the intrinsic gate-source capacitance of N- and PMOS transistor and an ideal 1pF at gate-to-ground. The inductor is 5nH with 3Ω of series resistance. Simulation shows Q_{sr} and ω_{sr} of 14.66 and 1.755GHz, respectively. Fig.3(a) and (b) show the phase noise characteristics from the phase noise equation (6), where Γ_{rms}=0.5, and the circuit simulation result at 100kHz offset frequency as a function of $n=\omega_o/\omega_{sr}$. As already commented before, the phase noise performance from (6) shows large difference to the circuit simulation result, since the tank noise source is only considered in (6). But, both of the phase noise characteristics shown in Fig.3(a) and (b) are well matched on the behavior over the

oscillation frequency and achieve the minimum phase noise at almost same frequency region. The most important point in Fig.3(b) is that the phase noise of C-Colpitts with symmetric capacitance tank (equivalent condition with the conventional differential LC oscillator shown in Fig.1(1), where $n=\omega_o/\omega_{sr}=\sqrt{2}=1.414$) shows. about 20dBc worse performance than that of the minimum phase noise(optimal asymmetric capacitance tank) in Fig.3(b). And the difference becomes higher with higher Q-factor of series resonant circuit in Fig. 3(a). Thus, using asymmetric capacitance tank, the phase noise can be optimized to the better performance than that with symmetric capacitance tank.

Fig.4(a) shows the conventional differential LC oscillator with symmetric capacitance tank. Noticeably, without doted-line, it becomes C-Colpitts oscillator. The differential LC oscillator shown in Fig.4(a) can be considered as two C-Colpitts oscillator combined perfect symmetrically such like the image in the mirror. But, the perfect symmetric differential combination of C-Colpitts shown in Fig.4(a) make disappear the supply voltage un-limited G node in Fig.2(c). Fig.4(b) is the differentially coupled C-Colpitts oscillator topology which combines two C-Colpitts oscillators in order to preserve the G node. The differential oscillators shown in Fig.4(a) and (b) are based on the same basic structure(C-Colpitts) and have the difference only in the method combining C-Colpitts. Anyway, the differentially coupled C-Colpitts oscillator can still adopt the asymmetric capacitance tank and be optimized with very high-Q inductor avoiding supply voltage pushing regardless the bias current and oscillation frequency. Thus, as shown in Fig.3, with the differentially coupled C-Colpitts oscillator, the better phase noise performance can be achieved than that of the conventional differential LC oscillator.

IV. Measurement Results

To prove above discussions about the asymmetric capacitance tank structure, the schematics shown in Fig.5(a) is composed as a test module with C-Colpitts oscillator core chip using 0.35 μm CMOS technology and external chip components for tank shown in Fig.5(b). The performance of VCO module is measured with 2.5V of supply voltage and R_{ext}=110ohm bye changing the value of C_d for given V_{ctrl}, L_{tank} and C_g. DC current flows 4.3mA ~ 6.3mA, which has about 40% of variation to the value of C_d. Fig. 6(a) and (b) show the measured performances over the oscillation frequency for the cases of L_{tank}=10nH, C_g=4pF and L_{tank}=5.6nH, C_g=2pF. In Fig.6(a), the capacitance of C_d ranges 0(open)~22pF and the oscillation frequency covers 688MHz(C_d=22pF) ~ 1290MHz(C_d= open). In Fig.6(b), the capacitance of C_d ranges 0(open)~10pF and the oscillation frequency covers 1150MHz(C_d=10pF) ~1747MHz(C_d=open). In both cases, to measure Q_{sr} and ω_{sr} of L_{tank}-C_g branch is impossible, but, since the oscillation frequency becomes close to the ω_{sr} as the value of C_d increases, the frequency of ω_{sr} can be expected as near the frequency of 688MHz and 1150MHz from Fig. 6(a) and (b).

Even though the measurement results in Fig. 6(a) and (b) are not normalized as ω_o/ω_{sr}, both the measured results show the same phase noise trend with the results shown in Fig. 3(a) and (b). With symmetric (C_g=C_d) external chip capacitor value, the phase noise performance in Fig. 6(a) and (b) is about 10dBc and 6dBc worse than the minimum phase noise performance with optimal asymmetric external chip capacitor value, respectively. This result proves that the phase noise can be optimized to the lower value with asymmetric capacitance tank structure than that with symmetric capacitance tank structure.

Since the oscillation frequency changes over the value of C_d, the power-frequency normalized FOM (Figure-Of-Merit) is provided for the objective comparison of performances. As shown in Fig.6, FOM also follows the same trend with the phase noise property.

V. Conclusion

This paper describes the phase noise optimization method using asymmetric capacitance tank structure, which overcomes the optimization limit of the recently published noise optimization approach using tank's L/C ratio optimization. The asymmetric capacitance tank structure can be easily applied to the C-Colpitts oscillator and the C-Colpitts oscillator shows the best phase noise in the oscillation frequency with optimal asymmetric capacitance combination. Moreover, the differentially coupled C-Colpitts oscillator is proposed, which can adopt the asymmetric capacitance tank structure. Thus, the proposed differentially coupled C-Colpitts oscillator topology can achieve the better phase noise performance than the conventional differential LC oscillator with symmetric capacitance tank structure.

Finally, a VCO test module is composed with C-Colpitts core chip using 0.35μm CMOS technology and two cases of external tank options: (a) L_{tank}=10nH, C_g=4pF and (b) L_{tank}=5.6nH, C_g=2pF. The measurement result shows that the minimum phase noise performance with optimal asymmetric capacitance is 10dBc and 6dBc better than that with the symmetric external capacitance. This proves the excellence of the asymmetric capacitance tank structure.

REFERENCES

[1] Donhee Ham and Ali Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," *IEEE JSSC*, Vol.36, No.6, June 2001.

[2] B. Razavi, "A 1.8-GHz CMOS voltage-controlled oscillator," in *ISSCC Dig. Tech. Papers*, 1997, pp. 388–389.

[3] Choong-Yul Cha and Sang-Gug Lee, "A Complementary Colpitts Oscillator based on 0.35 μm CMOS Technology", *ESSCIRC*, Portugal, Sep. 2003.

[4] Thomas H. Lee, *The Design of CMOS Raio-Frequency Integrated Circuits*, Cambridge University Press, 1998.

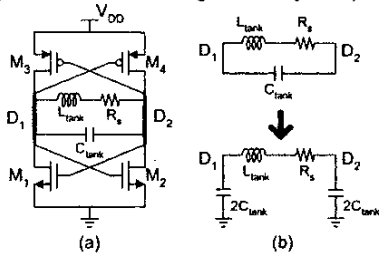

Fig.1 (a) differential LC oscillator (b) symmetric capacitance tank structure

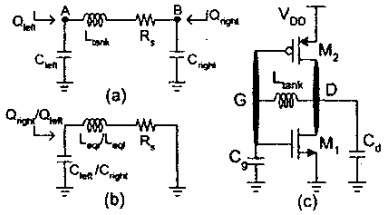

Fig.2 (a) π resonant circuit (b) equivalent parallel LC resonant circuit (c) complementary colpitts oscillator

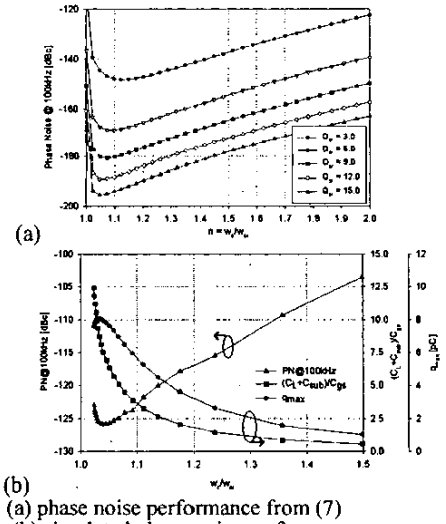

Fig. 3 (a) phase noise performance from (7)
(b) simulated phase noise performance

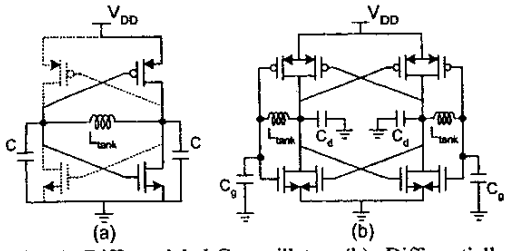

Fig.4 (a) Differential LC oscillator (b) Differentially coupled C-Colpitts oscillator

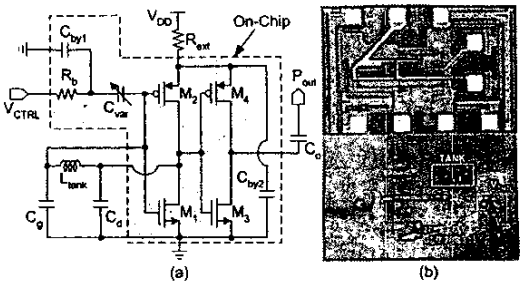

Fig.5 (a) C-Colpitts oscillator schematic (b) C-Colpitts core micrograph(top) and VCO module(bottom)

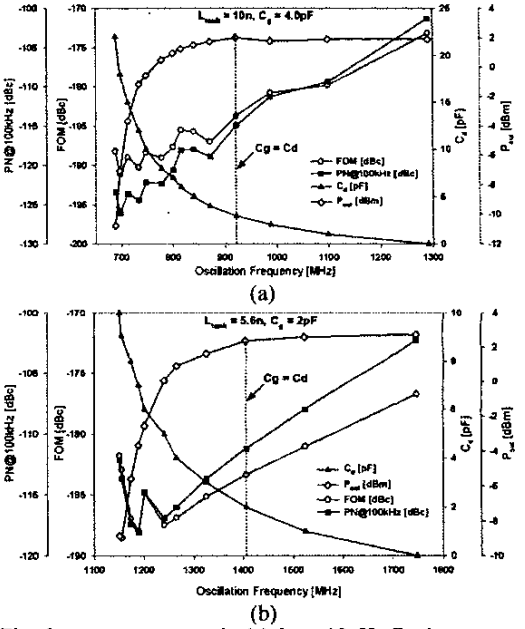

Fig. 6 measurement result: (a) L_{tank}=10nH, C_g=4p
(b) L_{tank}=5.6nH, C_g=2pF