A POWER CONSTRAINED SIMULTANEOUS NOISE AND INPUT MATCHED LOW NOISE AMPLIFIER DESIGN TECHNIQUE

Trung-Kien Nguyen, Yang-Moon Su, and Sang-Gug Lee

Information and Communications University
58-4 Hwa-am dong, Yuseong-gu, Daejeon, 305-732 South Korea
Email ntkienvn@icu.ac.kr

ABSTRACT

In this paper, very simple and insightful sets of noise parameters expressions for power-constrained simultaneous noise and input matching (PCSNIM) CMOS LNA design technique are newly introduced. Based on the noise parameters expression, the design principle, advantages, and limitations are clearly explained. The proposed LNA is optimized for low voltage, low power 900 MHz Zigbee applications based on 0.25 μm CMOS technology. Measurement results show power gain of 12 dB, NF and NF_{min} of 1.35 dB, and IIP3 of -4 dBm while dissipates the DC current of 1.6 mA (only 0.7 mA for NMOS transistor) at supply voltage of 1.25 V.

1. INTRODUCTION

In typical receiver architectures, a low noise amplifier (LNA) is one of the key components that determine the sensitivity of the receiver [1], [2]. Generally, the goal of LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation. A number of LNA design techniques have been reported to satisfy these goals [3]-[6]. The LNA design optimization technique proposed in [6] can be applied for power-constrained simultaneous noise and input matching. However, as discussed in [6], the fully potential of this technique is not provided clearly. This paper attempts to analyze and try to provide consistent and perspective understanding of this technique based on the noise parameter expressions. In addition, by using the noise parameter expressions, the design principle, advantages and practical limitation for the power-constrained simultaneous noise and input matching technique are explained. The proposed folded cascode LNA is fabricated based on 0.25 μm CMOS technology for 900 MHz Zigbee applications. Measurement results show power gain of 12 dB, NF and NF_{min} of 1.35 dB, IIP3 of -4 dBm while dissipates current of 1.6 mA (only 0.7 mA for NMOS transistor) from supply voltage of 1.25 V.

2. A POWER CONSTRAINED SIMULTANEOUS NOISE AND INPUT MATCHING TECHNIQUE

Fig. 1-(a) shows the schematic of a cascode topology that is adopted to explain the power constrained simultaneous noise and input matching (PCSNIM) LNA design technique. The LNA shown in Fig. 1-a differs by one additional capacitor C_{ex} compare to the typical cascode LNA. This LNA topology was first introduced in [6] as a solution to reduce the NF at low power dissipation, however, the potential and the theoretical analysis as a power-constrained (i.e., low power) simultaneous noise and input matchable LNA topology has not been recognized. Fig. 1-b shows the simplified small-signal equivalent circuit of the cascode amplifier shown in Fig. 1-a for the noise analysis. In Fig. 1-b, the effects of M_2 on the noise and frequency response are neglected [2], [3], as well as the parasitic resistances of gate, body, source, drain terminals, and the gate-drain capacitance of M_1.

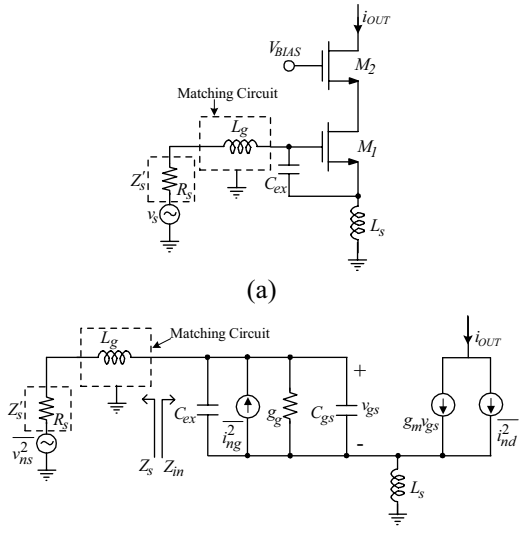

Fig. 1. Simple cascode LNA to adopt the PCSNIM technique (a) and its small-signal equivalent circuit (b)

In Fig. 1-(a), the mean-squared channel noise current is given by [7]

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f \qquad (1)$$

Here g_{do} is the drain-source conductance at zero drain-source voltage V_{DS}, k a Boltzmann constant, T absolute temperature and Δf bandwidth. The parameter γ has a

value of unity at zero V_{DS} in long-channel devices, 2/3 in saturation and increases more than two in short-channel devices and/or at high V_{GS} and V_{DS}. The fluctuating channel potential due to channel noise current in (1) couples capacitive into the gate terminal, leading to a noisy gate current. As in [7], the mean-squared gate-induced noise current is

$$\overline{i_{ng}^2} = 4kT\delta_{eff} g_g \Delta f \tag{2}$$

where $g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}$, $\delta_{eff} = \delta.\left(\frac{C_{gs}^2}{C_t^2}\right)$ and $C_t = C_{gs} + C_{ex}$

Here δ has a value of 4/3 in long-channel devices, whose value is twice of γ. The value δ also increases in short-channel devices and at high V_{GS} and V_{DS}.

As shown in Fig. 1, the mean-squared output noise current by the source matching circuit is

$$\overline{i_{o,ns}^2} = \left|\frac{R_s}{D}\cdot g_m\right|^2 \cdot \overline{i_{ns}^2} \tag{3}$$

When the source admittance is

$Y_s = G_s + jB_s = \left(R_s + sL_g\right)^{-1}$, the mean squared noise current by source is $\overline{i_{ns}^2} = 4kTG_s\Delta f$

The mean-squared output noise current by the gate induced noise source are given by

$$\overline{i_{o,ng}^2} = \left|\frac{R_s + sL_g + sL_s)}{D}\cdot g_m\right|^2 \cdot \overline{i_{ng}^2} \tag{4}$$

Since the mean-squared output noise current by the channel noise source is changed by the feedback source inductance L_s, so that the expression is

$$\overline{i_{o,nd}^2} = \left|\frac{1 + sC_{gs}(sL_g + sL_s) + sC_{gs}R_s}{D}\right|^2 \cdot \overline{i_{nd}^2} \tag{5}$$

where $D = 1 + sC_t(sL_g + sL_s) + sC_tR_s + g_m.sL_s)$ (6)

To consider the correlation between gate-induced and channel noise sources, the gate induced noise current is expressed as sum of uncorrelated and correlated portion. The mean-squared expression is

$$\overline{i_{ng}^2} = \overline{i_{ngu}^2} + \overline{i_{ngc}^2} = 4kT\delta g_g(1-|c|^2) + 4kT\delta g_g |c|^2 \tag{7}$$

The coefficient of cross-correlation between gate-induced and channel noise sources is c = 0.395j

Considering correlation, the total output noise current consists of the output current from source termination, gate-induced and channel noise sources. It is expressed as

$$\begin{aligned}\left|i_{o,total^2}\right|^2 &= \left|i_{o,ns} + i_{o,ng} + i_{o,nd}\right|^2 \\ &= \left|i_{o,ns}\right|^2 + \left|i_{o,ngc} + i_{o,nd}\right|^2 + \left|i_{o,ngu}\right|^2\end{aligned} \tag{8}$$

Noise factor can also be calculated as follows [2]

$$F = F_{min} + \frac{R_n\left|Y_s - Y_{opt}\right|^2}{G_s} \tag{9}$$

Here Y_s and Y_{opt} are source admittance and optimum source admittance, respectively.

Since the noise factor is defined as the ratio between total mean-squared output noise current and mean-squared output noise current due to input source only, therefore using (1)-(8), the noise factor is given expressed as

$$F = 1 + \frac{1}{g_m^2 R_s}\cdot\left\{\begin{array}{l}\gamma g_{d0}\cdot\left\{\begin{array}{l}\left[1 + s^2C_t\left(L_g + L_s\right)\left(1 + |c|\alpha\sqrt{\frac{\delta_{eff}}{5\gamma}}\right)\right]^2 \\ -\left(sC_tR_s\right)^2\left(1 + |c|\alpha\sqrt{\frac{\delta_{eff}}{5\gamma}}\right)^2\end{array}\right\} \\ -\frac{\alpha\delta_{eff}}{5}\left(1 - |c|^2\right)g_m\left(sC_t\right)^2\left(R_s^2 - sL_g^2\right)\end{array}\right\} \tag{10}$$

The noise parameters are obtained by comparing (9) and solving the zero solutions after differentiating (10) with respect to R_s and L_g respectively. The noise parameters are given by (11) – (13)

$$F_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{11}$$

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}} + j\left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\frac{C_t}{C_{gs}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \tag{12}$$

$$R_n = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m} \tag{13}$$

Note that, interestingly, as can be seen from (11) and (13), the minimum noise figure F_{min} and the noise resistance R_n are not affected by the addition of C_{ex}.

From Fig. 1-(b), the input impedance of the LNA is given by

$$Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_mL_s}{C_t} \tag{14}$$

As can be seen in (14), the source degeneration generates real part at the input impedance. This is important because there is no real part in the input impedance without degeneration while there is in the optimum noise impedance. Therefore, L_s helps to reduce the discrepancy between the real parts of the optimum noise impedance and the LNA input impedance. Furthermore, from (13), the imaginary part of Z_{in} is changed by sL_s, and this is followed by nearly the same change in Z_{opt} in (12), especially with advanced technology considering the value of c is higher than 0.4 (e.g., $c \approx 0.5$ with 0.25 μm technology), and α becomes lower than 1 [8].

Now, for the circuit shown in Fig. 1-(a), the condition that allows the simultaneous noise and input matching is

$$Z_{opt} = Z_{in}^* \tag{15}$$

From (11)-(14), (15) can be satisfied when the following conditions are met:

$$\mathrm{Re}[Z_{opt}] = \mathrm{Re}[Z_s] \quad (16) \qquad \mathrm{Im}[Z_{opt}] = \mathrm{Im}[Z_s] \quad (17)$$

$$\mathrm{Im}[Z_{in}] = -\mathrm{Im}[Z_s] \quad (18) \qquad \mathrm{Re}[Z_{in}] = \mathrm{Re}[Z_s] \quad (19)$$

Those conditions are re-expressed as follows

$$\frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)}+\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} = \mathrm{Re}[Z_s] \quad (20)$$

$$\frac{j\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)}+\left(\frac{C_t}{C_{gs}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - sL_s = \mathrm{Im}[Z_s] \quad (21)$$

$$sL_s + \frac{1}{sC_t} = -\mathrm{Im}[Z_s] \quad (22) \qquad \frac{g_m L_s}{C_t} = \mathrm{Re}[Z_s] \quad (23)$$

As mentioned above, for the advanced CMOS technology parameters, (21) is approximately equal to (22). Therefore, (22) can be dropped, which means that for the given value of L_s, the imaginary value of the optimum noise impedance becomes approximately equal to that of the input impedance with opposite sign. Now then, the design parameters that can satisfy (20), (21), and (23) are V_{GS}, W (or C_{gs}), L_s, and C_{ex}. Since there are three equations and four unknowns, (20), (21), and (23) can be solved for an arbitrary value of Z_s, by fixing the value of one of the design parameters that can be the power dissipation or V_{GS}. Another word this LNA design optimization technique allows to design simultaneous noise and input matching at any given amount of power dissipation.

The limitation of the power-constrained simultaneous noise and input matching technique is high value of noise resistance. As can be seen in (13), the noise resistance, R_n, of the proposed topology is not affected by the addition of C_{ex}, but only the function of g_m. Therefore, the small transistor size and low power can lead to very high R_n. High R_n can be a serious limitation for the practical high yield LNA design therefore be careful when apply this technique.

The qualitative description of the proposed design process would be as follows. First choose the DC bias, V_{GS}, for example the bias point that provides minimum F_{min}. Then, choose the transistor size, W, based on the power constraint, P_D. At this point, the value of Re[Z_{opt}] is determined. Now choose the additional capacitance, C_{ex}, as well as the degeneration inductance, L_s, to satisfy Re[Z_{opt}] = Re[Z_{in}]. The value of C_{ex} should be chosen considering the compromise between the size of L_s and the available power gain. As described before, large L_s can lead to the increase in F_{min}, while large C_{ex} leads to the gain reduction due to the degradation of the effective cut-off frequency of the composite transistor (transistor including C_{ex}). At this point, the simultaneous noise and input matching is achieved. As the last step, if there exists any mismatch between Z_{in} and Z_s^*, as shown in Fig. 1 (b), an impedance matching circuit can be added. The limitations of the PCSNIM technique are high R_n and low effective cut-off frequency. High R_n can be a serious limitation for the practical high yield LNA design. Fig. 2 shows the simulated *NF* and input return loss S_{11} as a function of frequency for the LNA topology shown in Fig. 1-a for three transistor sizes. In Fig. 2, the simulation is based on 0.25 μm CMOS technology with the supply voltage of 1.25 V. The amount of power dissipation is varied by changing the transistor size, with the supply current of 1.6, 4.8 and 9.6 mA, for a given value of gate-source voltage. In Fig. 2, in addition to the good input matching, for all power levels, the NF of the designed LNAs coincides with the F_{min} of the transistor at the frequency of interest. Note that, with reduction in the amount of power dissipation (smaller transistor size), due to the larger R_n, the NF of LNAs increases sharply at the frequencies away from the optimum point.

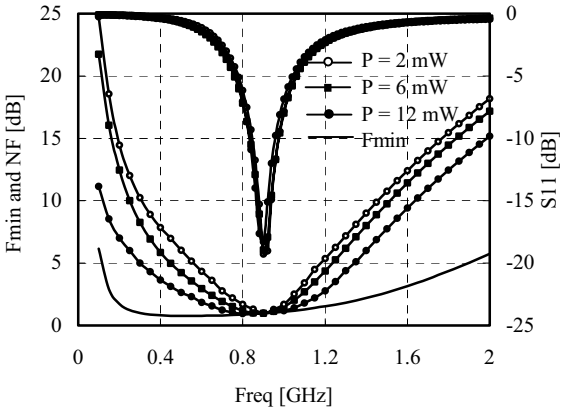

Fig. 2. The simulated NF, F_{min}, and S_{11} of the LNA shown in Fig. 1

3. MEASUREMENT RESULTS

As a demonstration for the proposed design principle of the PCSNIM technique, a very low power folded cascode LNA shown in Fig. 3 is implemented based on 0.25 μm CMOS technology for 900 MHz ZigBee [9] application, which requires very low power dissipation and low supply voltage. In Fig. 3, the folding helps to extend the cut-off frequency of the M_1. The parasitic capacitances at the drain node of M_1 can be eliminated by the resonance with L_d, which helps to suppress the noise contribution of M_2 at the output and avoid the signal loss into the silicon substrate. In Fig. 3, the size of C_{ex} and L_s are chosen following the design principle of the PCSNIM technique, and L_g is inserted for the input matching to the signal source impedance of 50 Ω. A simple L-C network using

an off-chip inductor L_o and an on-chip capacitor C_o are used to match the output of the LNA. In Fig. 3, the LNA dissipates the total current of 1.6 mA from the supply voltage of 1.25 V (NMOS transistor consumes only 0.7 mA). Fig. 4 shows the measurement results of the LNA shown in Fig. 3. In Fig. 4, the LNA shows power gain of 12 dB, NF of 1.35 dB, and S_{11} of –18 dB, respectively, at 910 MHz. In Fig. 4, the F_{min} of the LNA is also shown as a function of frequency, and as can be seen the NF of the LNA coincides well with F_{min} at the frequencies of interest showing good agreement with analysis. Fig. 5 shows the measured IIP3 of – 4 dBm and Fig. 6 shows the microphotograph of the LNA.

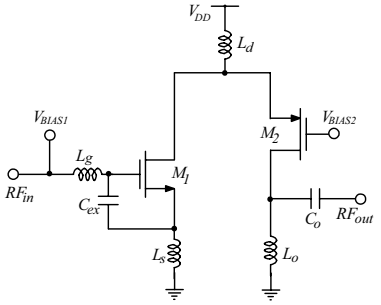

Fig. 3 Schematic of the proposed folded cascode LNA

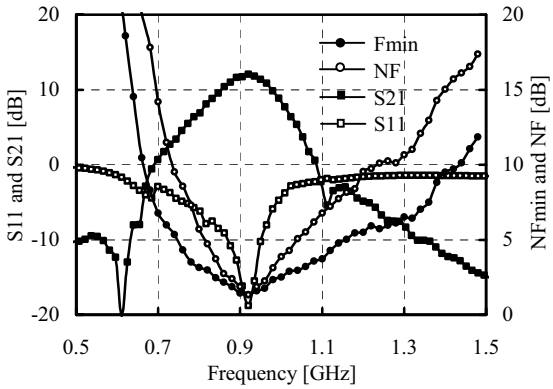

Fig. 4 The measured results of the folded cascode LNA

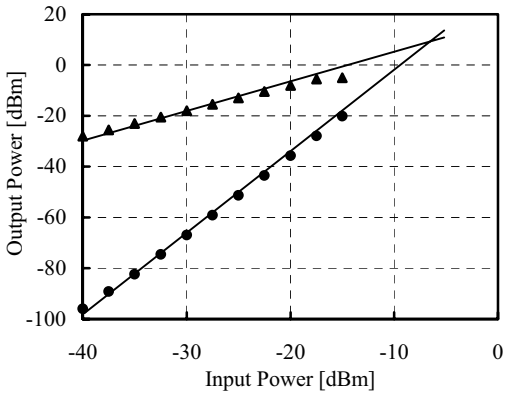

Fig. 5 IIP3 of the proposed folded cascode LNA

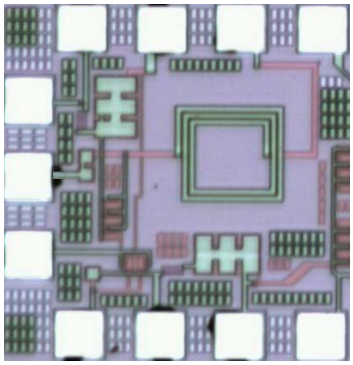

Fig. 6 Microphotograph of the folded cascode LNA

4. CONCLUSION

A power-constrained simultaneous noise and input matching (PCSNIM) for CMOS low noise amplifier optimization technique is introduced. Very simple and insightful sets of noise parameters are analyzed and the design principle is described. Based on the noise parameter expressions, the design principles, advantages, and limitations of PCSNIM technique are discussed. As the demonstration, a very low voltage, low power LNA is designed for 900 MHz Zigbee applications. The measured results show the 12 dB of power gain, 1.35 dB of NF (also equal to F_{min}) and – 4 dB of IIP3. The measured results show a very good agreement with analysis.

5. REFERENCES

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