

# ULTRA LOW-VOLTAGE LOW-POWER EXPONENTIAL VOLTAGE-MODE CIRCUIT WITH TUNABLE OUTPUT RANGE

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## ABSTRACT

In this paper, an ultra low-voltage and low-power exponential voltage-mode circuit is developed using the “pseudo-exponential” approximation for realizing the exponential characteristics. The proposed circuit provides controllable output voltage range at very low-voltage applications (less than 1.2 V). In a 0.25  $\mu\text{m}$  CMOS process, the simulations show more than 35 dB output voltage range and 27 dB range with the linearity error less than  $\pm 0.5$  dB. The average power dissipation is less than 0.2 mW. The proposed circuit can be used for the design of an extremely low-voltage and low-power variable gain amplifier (VGA) and automatic gain control (AGC).

## 1. INTRODUCTION

The exponential voltage-mode circuit is the key component for the design of VGAs and AGCs, which are widely used in analog signal processing; such as in hearing aids, disk drives, and telecommunication applications [1-3]. This circuit is not available in CMOS technology since CMOS transistors follow a square-law characteristic in the strong inversion. However, it is easily obtained in bipolar technology. Unfortunately, the bipolar techniques for VGAs and AGCs are not compatible for monolithic low voltage CMOS-based analog and mixed-signal circuits. Moreover, good performance bipolar transistors are not readily available in the conventional technology, while BiCMOS solution may not be cost-effective. Although CMOS transistors exhibit exponential characteristics in weak inversion, except the very low-speed application, the circuit could be too slow.

Since there is no intrinsic logarithmic MOS device operating in the saturation region for CMOS technologies, the exponential characteristics can be implemented by using a “pseudo-exponential” generator [1-4], or Taylor series expansion for realizing the exponential characteristics [5-7]. The “pseudo-exponential” generator is

often used, because it offers higher dB range compared to the Taylor based method.

The advances in the CMOS VLSI technology and the market demand for portable and mobile electronic equipment lead to increasing reductions on the power consumption. CMOS devices feature high-input impedance, extremely low-offset switches, high packing density, low-switching power consumption, and most importantly, they are easily scaled. Scaling down the transistor sizes can then integrate more circuit components in a single chip so the circuit area, and thus its cost, will be reduced. When a MOS transistor size is decreased, not only are its channel length and width reduced, but also the thickness of the gate oxide. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced. As a result, low-voltage and low-power CMOS VLSI circuits are of particular interest.

The most effective way of reducing power consumption is to lower the supply voltage. However, many of the existing CMOS analog building blocks, designed to operate with higher supply voltages, will lose a significant amount of operating range and need to be reconsidered [8].

In this paper, the authors propose a new idea to turn the limitations of low-voltage circuit into advantages that the dB output voltage range is extended from 15 dB to 27 dB with error less than  $\pm 0.5$  dB and the input range is improved, as well. And thus low-voltage and low-power circuits are obtained. The Simulation results will be given to verify the validity of this approach.

## 2. PROPOSED IDEAS

According to the Taylor series expansion, a general exponential function can be expressed as

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \dots + \frac{a^n}{n!}x^n + \dots \quad (1)$$

Where  $a$  and  $x$  are the coefficient and the independent variables, respectively. From the Taylor series expansion, the “pseudo-exponential” function is given as

$$f(x) = e^{2ax} = \frac{e^{ax}}{e^{-ax}} \approx \frac{1+ax}{1-ax} \quad (2)$$

for  $a = 0.1$ , the plots of the pseudo-exponential approximation and the Taylor series approximation are given in Fig. 1 by the dashed and dotted lines, respectively ( $x = f_1(t) = t$  as shown in Fig. 2 by the solid line). As shown in Fig. 1 by the dashed line, the pseudo-exponential approximation offers 15 dB linear range with the linearity error less than  $\pm 0.5$  dB for  $|x| < 4.2$ . Otherwise, the deviation of the pseudo-exponential approximation from the ideal exponential will be increased drastically. As a result, the dB linear range as well as the input range are critically limited.

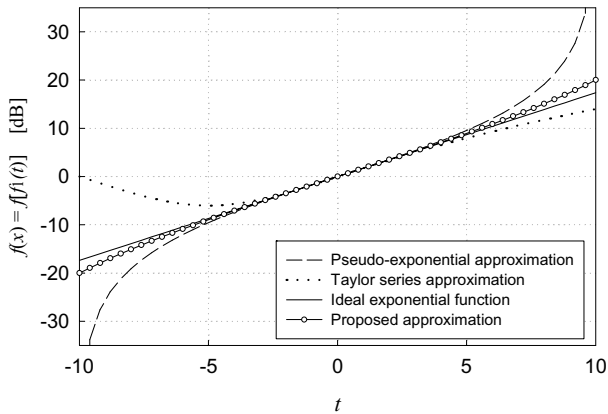


Fig. 1 Plots of various functions on dB-scale

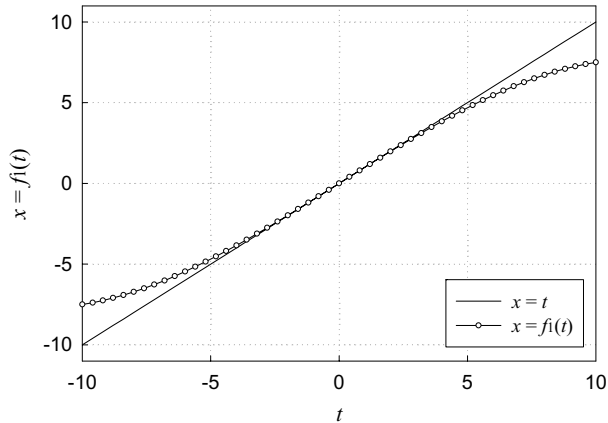


Fig. 2 Plots of  $x$  versus  $t$  for various functions

In this paper, the variable  $x$  is considered as a function of  $t$  as depicted in Fig. 2, the  $x$  is relatively linear function of  $t$  for  $|t| \ll 5$  (i.e  $x = t$ ). In this region, the  $f(x) = f(t)$  is closed to the ideal exponential function as depicted in Fig.1 by the dashed and o'symbol lines. Otherwise, it is a nonlinear function of  $t$  as shown in Fig. 2 by the o'symbol line. In Fig. 2, for positive  $t$ -value, the variable  $x$  goes down such that the numerator of Eq. (2) as a function of  $t$

decreases while the denominator of Eq. (2) as a function of  $t$  increases (assume that  $a > 0$ ). As a result, the  $f(x) = f[f_1(t)]$  as a function of  $t$  will move close to the ideal exponential function as shown in Fig. 1 by the o'symbol line. Similarly, in the negative  $t$ -value, the  $f(x) = f[f_1(t)]$  as a function of  $t$  will move close to the ideal exponential. Consequently, the dB-linear range and the input range are improved.

In this paper, the variable  $x$  and  $t$  are chosen to be current and voltage parameters, respectively. Hence, the output voltage  $f(x)$  is a function of the input voltage  $t$ .

As discussed earlier, to lower the power consumption of the circuit, the most effective solution is to lower the supply voltage. Unfortunately, this will degrade the performance of the circuit as can be seen in [8]. The ideas in this paper allow designers not only to resolve the limitations of low-voltage applications, but also improve the dB-output as well as the input dynamic ranges. This will be discussed more lately.

### 3. CIRCUIT DESCRIPTIONS

#### 3.1 Nonlinear V-I conversion circuit

As mentioned in section 2, the variables  $x$  and  $t$  are respectively chosen to be current and voltage parameters, therefore, the nonlinear V-I conversion circuit with the I-V characteristics as shown in Fig. 2 is required. This paper used the linear V-I converter which is adopted from [8].

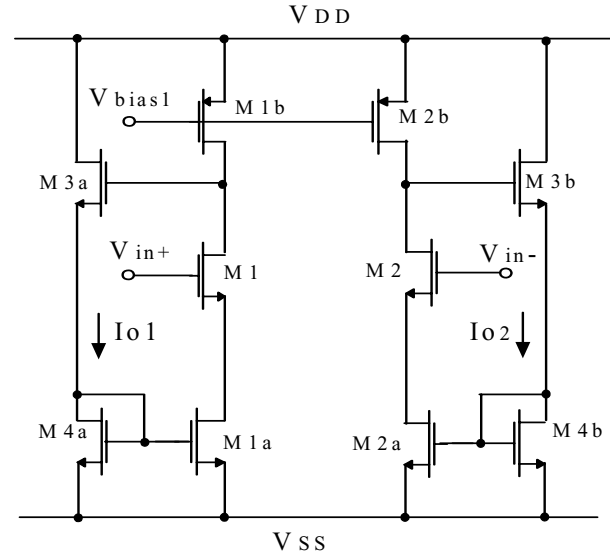


Fig. 3 Nonlinear V-I conversion circuit

As in [8], the input differential voltage is applied to the gate of transistors M1 and M2 which are biased in the saturation region. The transistor M1b,2b and M1a,2a are biased in the triode region. The feedback loops M3a,4a and M3b,4b maintain triode operation of M1b,2b and M1a,2a. By mirroring the differential current through M1a,4a and M2a,4b and subtracting them, a linear  $I_1 = I_{o1} - I_{o2} = k(V_{in+}$

$-V_{in-}) = kV_d$  can be obtained, where  $k$  is a constant.

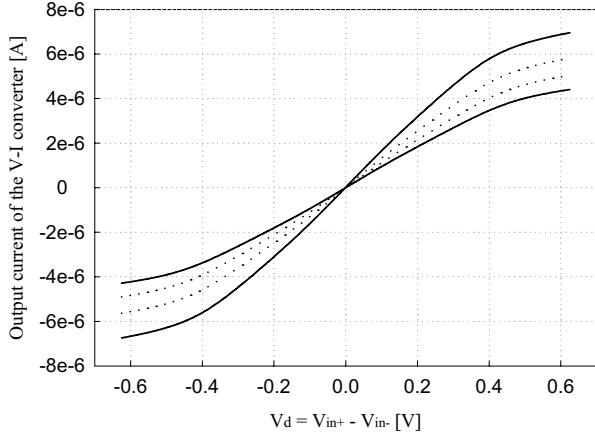


Fig. 4 I-V characteristic of the nonlinear V-I conversion circuit shown in Fig. 3 for various  $V_{bias1}$ .

At low voltage applications, [8] shows that the linear I-V characteristic no longer exists when the differential voltage  $V_d = V_{in+} - V_{in-}$  increases. The performance of the nonlinear V-I converter at 1.2 V supply voltage is given in Fig. 4. as shown in Fig. 4, for different  $V_{bias1}$ , various I-V characteristics are generated. This will help to control the output range of the overall circuit.

### 3.2 Proposed exponential voltage-mode circuit

The complete exponential voltage-mode circuit is given in Fig. 5. As shown in Fig. 5, transistors M5a and M5b,5c copy the current  $I_{01}$  and  $I_{02}$ , respectively. The transistors M6a,6b,6c copy the current  $I_{01}$  and subtract them to the current  $I_{02}$  to generate two identical current signals  $I_1$  ( $= I_{01} - I_{02}$ ). Then, these two identical signals are respectively added and subtracted to the bias current  $I_0$  to generate the signal  $(I_1 + I_0)$  and  $(I_1 - I_0)$  as shown in Fig. 5. The current  $(I_1 - I_0)$  is copied to the drain current of the transistor M10, while the current  $(I_1 + I_0)$  is fed to the drain of transistors M7 and M8. As reported in [10] the transistors M7 and M8 constitute the linear I-V converter, and the output voltage of this converter is given as [11]

$$V_{GM12} = \frac{V_{DD} - |V_{Tp}| + V_{Tn}}{2} - \frac{(I_1 + I_0)}{K(V_{DD} - |V_{Tp}| - V_{Tn})} \quad (3)$$

Where  $V_{G,M12}$  is the output voltage of this converter which is also the gate voltage of transistor M12. The transistor M12 is assumed to be in the triode region and acts as a voltage controlled resistor. For small drain-source voltage, the resistance exhibited by M12 is given as

$$R_{DS} \square \frac{1}{K_{M12}(V_{G,M12} - V_{TH})} \quad (4)$$

Consequently, the current  $(I_1 - I_0)$  flowing through M12 will generate a drain-source voltage,  $V_{DS} = R_{DS}(I_1 - I_0)$ ,

proportional to  $(I_1 - I_0)/(I_1 + I_0)$ . Hence, the following equation applies

$$V_0 = V_{DS,M12} \approx \alpha \frac{I_1 - I_0}{I_1 + I_0} \quad (5)$$

where  $\alpha$  is a constant. In Eq. (5), the output voltage  $V_0$  is pseudo-exponential function of the current  $I_1$  as in Eq. (2). The  $I_1$  is a nonlinear function of the input differential voltage  $V_d = V_{in+} - V_{in-}$ . Finally, the pseudo-exponential approximation of the proposed circuit shown in Fig. 5 is given as

$$V_0 = \alpha \frac{kV_d - I_0}{kV_d + I_0} = \alpha \frac{kV_d/I_0 - 1}{kV_d/I_0 + 1} \quad (6)$$

the  $V_0$  is thus a pseudo-exponential function of input differential voltage  $V_d$  as in Eq. (2), where  $a = k/I_0$ .

## 4. SIMULATION RESULTS

The proposed circuit was verified in a 0.25  $\mu\text{m}$  CMOS technology with the supply voltage of 1.2 V. For various  $V_{bias1}$ , the I-V characteristics of the nonlinear V-I converter is shown in Fig. 4, which is relatively linear function for small value of  $|V_d|$ . From these I-V curves, the  $I_0$  is determined to satisfy the condition  $|ax| \ll 1$ . This means that  $V_d \ll I_0/k$ . Then, 15 dB linear output voltage range with the error less than  $\pm 0.5$  dB can be obtained. When  $V_d$  is out of the linear region, the output current is nonlinear function of  $V_d$ , which helps to move the approximation close to the ideal exponential function.

The performance of the proposed circuit shown in Fig. 5 for various  $V_{bias1}$  is given in Fig. 6. As shown in Fig. 6, the solid line show 35 dB range, and 27 dB-linear range with error less than  $\pm 0.5$  dB over large differential input voltage  $V_d$  from  $-0.52$  V to  $0.48$  V. Also shown in Fig. 6, the dashed line shows 10 dB range.

The proposed circuit has its transfer function controlled by the  $V_{bias1}$ . The output range can be controlled from 10 dB to 27 dB with error less than  $\pm 0.5$  dB. This characteristic is useful for analog and mixed-mode circuits such as VGAs [8] and AGCs.

## 5. CONCLUSIONS

This paper proposed a simple circuit to achieve the pseudo-exponential approximation function. The proposed ideas in this papers are very useful for circuits operating at low-voltage applications. This circuit can increases the output voltage from 15 dB (i.e traditional pseudo-exponential approximation) to 27 dB linear range with error less than 0.5 dB at ultra low-voltage (less than 1.2 V) and low-power (less than 0.2 mW) applications. Moreover, this circuit also offers controllable output range, which is useful for VGAs [9] and AGCs applications. The proposed circuit could be used as a current-to-voltage converter by adding the linear I-V converter to the input as discussed in section 3.2.

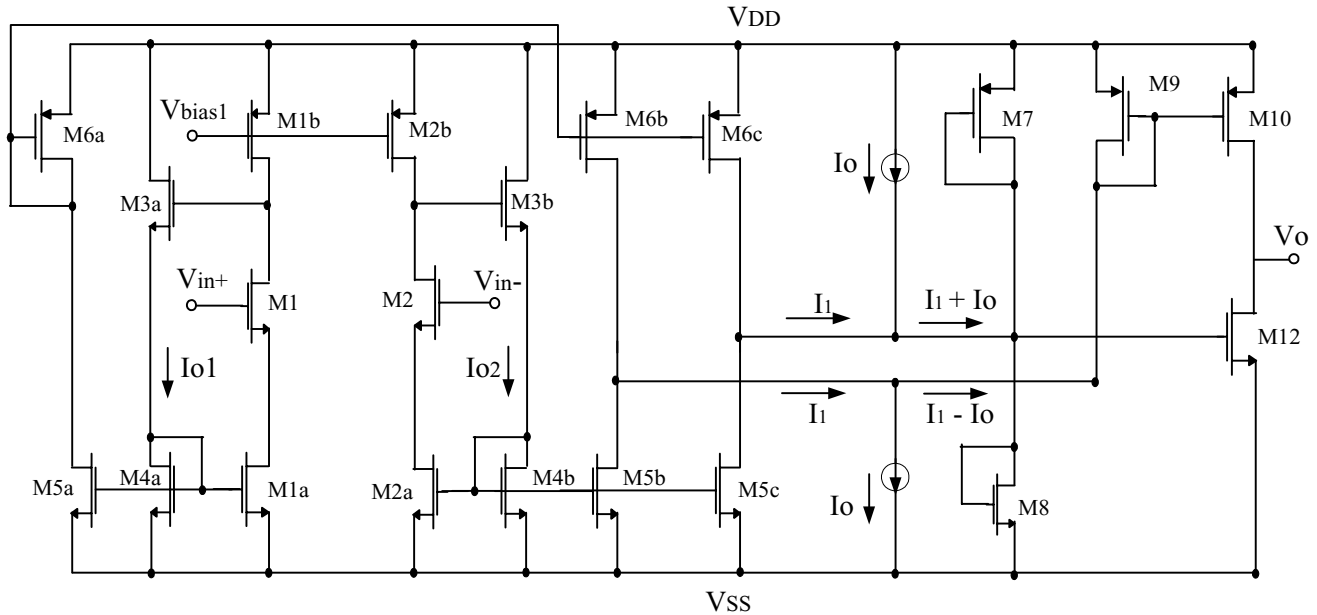


Fig. 5 The proposed exponential voltage-mode circuit

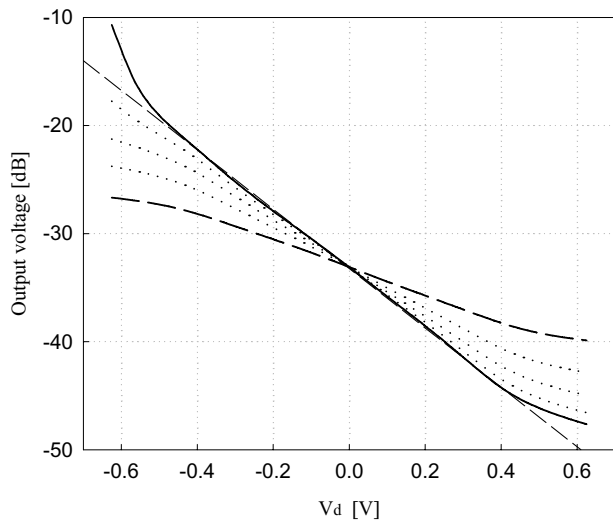


Fig. 5 The performance of the proposed circuit shown in Fig. 5 for various  $V_{bias1}$ .

## 6. REFERENCES

- [1] R. Harijani, "A Low-power CMOS VGA for 50 Mb/s Disk Drive Read Channels," *IEEE Trans. Circuits and Syst.* vol. 42, no. 6, pp. 370-376, June, 1995.
- [2] K. M. Abdelfattah and A. M. Soliman, "Variable Gain Amplifier Based on a New Approximation Method to Realize the Exponential Function," *IEEE Trans. Circuits Syst.*, vol. 49, no. 9, Sep 2002.
- [3] H. Elwan, A. M. Soliman, and M. Ismail, "A. digitally controlled dB-linear CMOS variable gain amplifier," *Elect. Lett.*, vol. 35, no.20, pp. 1725-1727, 1999.

- [4] A. Motanemd, C. Hwang and M. Ismail, "CMOS exponential current-to-voltage converter," *Elect. Let.*, vol. 33, no. 12, pp. 998-1000, 5<sup>th</sup> June, 1997.
- [5] Lin, C., Pimenta, T., and Ismail, M., "Universal exponential function implementation using highly-linear CMOS V-I converters for dB-linear (AGC) application". *Proc. 1998 IEEE Midwest symp. Circuits and Sys.*, 1999, pp. 360-363.
- [6] W. Liu, C. Chang, and S. Liu, "Realisation of Exponential V-I Converter using composite NMOS transistors," *Elect. Let.*, vol. 36, no. 1, pp. 8-10, 6<sup>th</sup> Jan, 2000.
- [7] Quoc-Hoang Duong, T.Kien N, and Sang-Gug Lee, "Low-Voltage Low-Power High dB-Linear CMOS Exponential Function Generator Using Highly-linear V-I Converter," *IEEE International symposium on Low Power Electronics and Designs*, to be published on August, 2003.
- [8] C.-H. Lin, M. Ismail and T. Pimenta "A 1.2 V Micropower CMOS Class AB V-I converter for VLSI Cells Library Design," *IEEE Midwest Symp. on Circuit and Systems*, September, 1998.
- [9] W.C. Song, C. J. Oh, G.H. Cho and H.B. Jung "High frequency/high dynamic range CMOS VGA," *IEE Electronics letters*, vol. 36, pp. 1096-1098, June 2000.
- [10] H. Wasaki, Y.Horio, and S. Nakamura, "Current multiplier/divider circuit," *IEE Electronics letters*, vol. 27, pp. 504-506, March 1991.
- [11] A. Motamed, C.Hwang, and M.Ismail, "CMOS exponential current-to-voltage converter," *IEE Electronics letters*, vol. 33, pp. 998-1000, June 1997.

## 7. ACKNOWLEDGEMENT

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