

CMOS EXPONENTIAL CURRENT-TO-VOLTAGE CIRCUIT BASED ON NEWLY PROPOSED APPROXIMATION METHOD

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ABSTRACT

This paper proposed a low-voltage and low-power current-to-voltage converter with controllable transconductance. The proposed circuit uses a newly proposed approximation function to increase the dB-linear output range. In a 0.25 μm CMOS process, the simulations show a 58 dB output voltage range and a 46 dB with the linearity error less than ± 0.5 dB. The average power dissipation is less than 0.8 mW at 1.5 V supply voltage. The proposed circuit can be used for the design of an extremely low-voltage and low-power variable gain amplifier (VGA) and automatic gain control (AGC).

1. INTRODUCTION

The advances in the CMOS VLSI technology and the market demands for portable and mobile electronic equipments lead to increasing reductions on the power consumption. CMOS devices feature high-input impedance, extremely low-offset switches, high packing density, low-switching power consumption, and most importantly, they are easily scaled. Scaling down the transistor sizes can then integrate more circuit components in a single chip, so that the circuit area, and thus its cost, will be reduced. When a MOS transistor's size is decreased, not only are its channel length and width reduced, but also the thickness of the gate oxide. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced. Also, lowering the supply voltage is the most efficient way to lower the power consumption. As a result, low-voltage and low-power CMOS VLSI circuits are of particular interest.

Among the mostly used circuits in mixed signal VLSI circuits are VGAs and AGCs, which play an important role in telecommunications applications, medical equipments, hearing aids, disk drives and others [1-3]. The key component for the design of VGAs and AGCs is the exponential function generator. This circuit is not available in CMOS technology since CMOS transistors follow a square-law characteristic in strong inversion. However, it is easily obtained in bipolar technology. Unfortunately, the bipolar techniques for VGAs and AGCs are not compatible for monolithic low voltage CMOS-based analog and mixed-signal circuits. Moreover, good performance bipolar

transistors are not readily available in the conventional technology, while BiCMOS solution may not be a cost-effective solution.

Since there is no intrinsic logarithmic MOS device operating in the saturation region for CMOS technologies, the exponential characteristics can be implemented by using a "pseudo-exponential" generator [1-4], or the Taylor series expansion for realizing the exponential characteristics [5-7]. However, these previously reported approaches show very small dB-linear output ranges less than 20 dB [5-7]. Though [4] reported higher dB-linear range (30 dB) by implementing the square of 'pseudo-exponential' function, the dB-linear range is still restricted.

This paper proposes a newly exponential approximation function that can extend the dB-linear range up to very high value. The proposed circuit provides a 58 dB range and a 46 dB with the linearity error less than ± 0.5 dB, while consumes extremely low power (less than 0.8 mW) at low-voltage applications (less than 1.5 V). Moreover, the proposed circuit offers controllable transconductance by adjusting the bias current. This feature is very useful for analog and mixed-mode circuits such as VGAs and AGCs. The simulation results will be given to verify the validity of these approaches.

2. NEWLY PROPOSED EXPONENTIAL APPROXIMATION FUNCTION

According to the Taylor series expansion, a general exponential function can be expressed as

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \dots + \frac{a^n}{n!}x^n + \dots \quad (1)$$

Where a and x are the coefficient and the independent variables, respectively. For $|ax| \ll 1$, the Eq. (1) can be approximated as

$$e^{ax} \approx 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 = \frac{1}{2} \left[1 + (1+ax)^2 \right] \quad (2)$$

The "pseudo-exponential" approximation function is given as

$$e^{ax} = \frac{e^{ax/2}}{e^{-ax/2}} \cong \frac{1+ax/2}{1-ax/2} \quad (3)$$

for $a = 0.1$, the plots of the pseudo-exponential approximation and the Taylor series approximation are given in Fig. 1 by the dash-dotted and dashed lines, respectively.

As shown in Fig. 1, the Taylor series approximation and the pseudo-exponential approximation provide 12 dB and 15 dB ranges with the linearity error less than ± 0.5 dB, respectively.

This paper introduced a new approximation function, which is given as

$$e^{ax} = \frac{e^{ax/2}}{e^{-ax/2}} \cong \left[\frac{k + (1 + ax/2)^2}{k + (1 - ax/2)^2} \right] \quad (4)$$

for $k = 1$, the numerator and denominator in Eq. (4) are all Taylor series approximation functions. Also, for $k = 1$, the Eq. (4) provides about 20 dB with linearity error less than ± 0.5 dB as depicted in Fig. 1 by the o'symbol line. However, for the k slightly less than unity, the dB-linear range of Eq. (4) is extended drastically. For instance, $k = 0.8$, the dB range is extended from 20 dB to 40 dB with error less than ± 0.5 dB. Also shown in Fig. 1 by the solid line, for $k = 0.6$, the dB-linear range is extended to about 50 dB with error less than ± 0.5 dB.

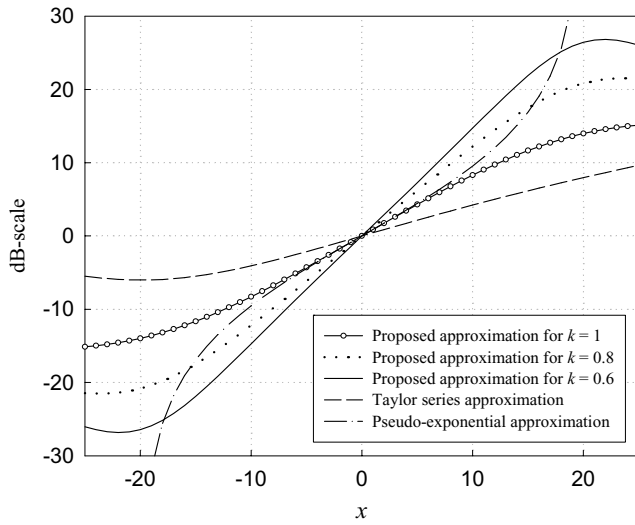


Fig. 1 Plots of various functions on dB-scale

The newly proposed approximation method in this paper can obtain very high dB range compared to that of the traditional methods such as Taylor series expansion and pseudo-exponential approximations. Moreover, the input dynamic ranges are also extended as shown in Fig. 1 by the o'symbol, dotted, and solid lines.

The proposed circuit to implement Eq. (4) will be developed in section 3.

3. CIRCUIT DESCRIPTIONS

3.1 Basic circuit

To implement the Eq. (4), the Taylor series expansion approximation function is needed. This section presents a basic and very compact circuit for realizing the Taylor approximation as shown in Fig. 2 (b) [9]. The current-mode functional circuit in this section is adopted from [9] where all transistors are supposed to be in saturation region. Then the drain currents of transistors M5 and M6 in Fig. 2 (b) are given as

$$I_{d,M5,6} = K(V_{gs,M5,6} - V_t)^2 \quad (5)$$

It is shown from [10] that the output current, $I_{sq} = I_{d,M5} + I_{d,M6}$ of the circuit in Fig. 2 (b) can be given as

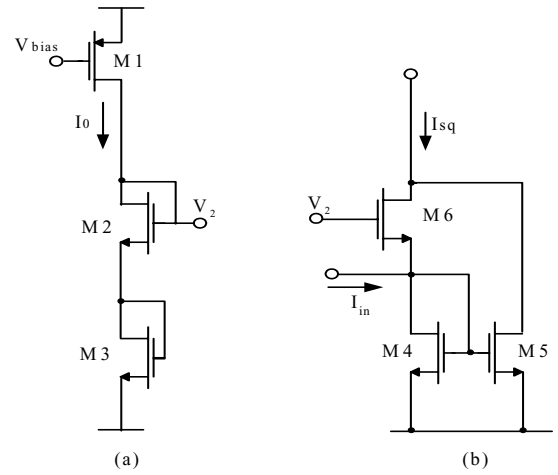
$$I_{sq} = \frac{1}{2} K(V_2 - 2V_t)^2 + \frac{(I_{d,M6} - I_{d,M5})^2}{2K(V_2 - 2V_t)^2} \quad (6)$$

by using the bias circuit as shown in Fig. 2 (a), the Eq. (6) can be written as

$$I_{sq} = I_{d,M6} + I_{d,M5} = 2I_0 + I_{in}^2 / 8I_0 \quad (7)$$

where the I_0 is given as $I_0 = (K/4)(V_2 - 2V_t)^2$,

and $I_{in} = I_{d,M6} - I_{d,M5}$ as shown in Fig. 2(b).



**Fig. 2. (a) The bias circuit for the circuit in (b)
(b) The current-mode building block for proposed exponential approximation.**

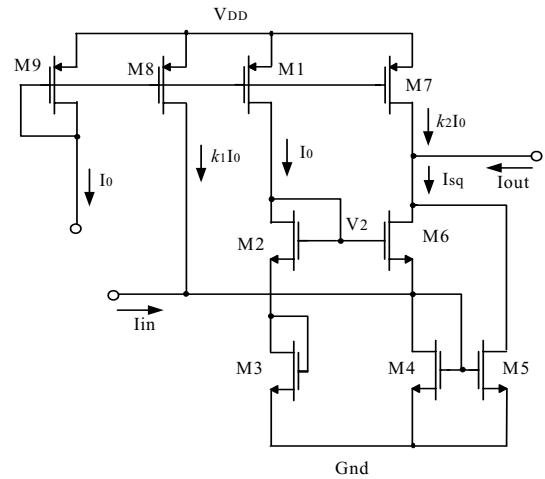


Fig. 3 The circuit implementation of the Eq. (2) based on the current-mode block shown in Fig. 2

In order to keep all devices in the ON state the input current should be in the range $|I_{in}| < 4I_0$.

The completed circuit to implement the Taylor series approximation is given in Fig. 3. It can be shown that the output current, I_{out} , in Fig. 3 can be written as

$$I_{out} = 2I_0 + \frac{(I_{in} + k_1 I_0)^2}{8I_0} - k_2 I_0$$

$$= \frac{k_1^2 I_0}{8} \left[\frac{8(2 - k_2)}{k_1^2} + \left(1 + \frac{I_{in}}{k_1 I_0} \right)^2 \right] \quad (8)$$

for $k_1 = \sqrt{8(2 - k_2)}$ the exponential approximation in Eq.(2) is achieved and given as

$$I_{out} = \frac{k_1^2 I_0}{8} \exp\left(\frac{I_{in}}{k_1 I_0}\right) \quad (9)$$

The current, I_{out} , is thus a Taylor exponential approximation function of the input current I_{in} , where $a = 1/(k_1 I_0)$. From the basic circuit discussed in this section, the overall exponential current-to-voltage will be discussed in section 3.2.

3.2 Proposed exponential current-to-voltage circuit

As presented earlier, the current-mode functional circuit has its transfer function shown in Eq. (8). For the inverse input current (*i.e.* $-I_{in}$), the output current is given as

$$I_{out1} = \frac{k_1^2 I_0}{8} \left[\frac{8(2 - k_2)}{k_1^2} + \left(1 - \frac{I_{in}}{k_1 I_0} \right)^2 \right]$$

$$\cong \frac{k_1^2 I_0}{8} \exp\left(-\frac{I_{in}}{k_1 I_0}\right) \quad (10)$$

from Eq. (8) and (10), the division of these two currents leads to the following equation

$$I_{exp} = \frac{I_{out1}}{I_{out}} = \frac{\left[\frac{8(2 - k_2)}{k_1^2} + \left(1 - \frac{I_{in}}{k_1 I_0} \right)^2 \right]}{\left[\frac{8(2 - k_2)}{k_1^2} + \left(1 + \frac{I_{in}}{k_1 I_0} \right)^2 \right]} \quad (11)$$

obviously, the Eq. (11) is actually the approximation given in Eq. (4), where $k = 8(2 - k_2)/k_1^2$ and $a = -1/k_1 I_0$.

The circuit implementation of Eq. (11) is given in Fig. 4, where two identical current-mode functional circuits shown in Fig. 3 are used to generate two signals I_{out} and I_{out1} , respectively. As shown in Fig. 4, the current mirror M10-M11 is used to direct the current I_{out} to the drain of transistors M12 and M14, which operates in saturation region. The other current I_{out1} is also directed to the drain current of transistor M13, which is in triode region. A constant resistance, R_{in} , seen at the common drain node of the two diode connected transistors M12 and M14 can be given as [4]

$$R_{in} = \frac{1}{K(V_{DD} - |V_{Tp}| - V_{Tn})} \quad (12)$$

this resistance converts the current I_{out} to a gate voltage of transistor M13, $V_{G,M13}$. Transistor M13 operates in the triode region and acts as a voltage controlled resistor. For small drain-source voltages, the resistance exhibited by M13 is $R_{DS} \cong 1/K_{M13}(V_{G3} - V_{Tn})$. Hence, I_{out1} flows through M13 and generates a drain-source voltage, $V_{DS} = R_{DS}I_{out1}$, proportional to I_{out1}/I_{out} .

4. SIMULATION RESULTS

The proposed circuit was verified in 0.25 μm CMOS technology with the supply voltage of $V_{DD} = 1.5$ V. For $I_0 = 35$ μA , the input range will from -35 μA to 35 μA . For $k_1 = 1$, and $k_2 = 15/8$, the approximation in Eq. (4) with $k = 1$ is achieved, therefore, 20 dB with linearity less than 0.5 dB over the input current from -35 μA to 35 μA is obtained as shown in Fig. 5 by the dash-dotted line. While k_2 increases, from Fig.1, Eq. (11) and Eq. (4) the constant k decreases such that the dB-linear range of the overall circuit is extended as shown in Fig. 5 by the dotted and solid lines. Fig. 6 show the I-V characteristic of the proposed circuit shown in Fig. 4 which can achieve 58 dB range and 46 dB with the linearity error less than ± 0.5 dB over the input range from -36 μA to 32 μA . As shown in Eq. (11), by controlling the bias current I_0 , the transconductance and the input range of the overall proposed circuit can be controllable.

5. CONCLUSIONS

The proposed circuit in this paper has advantages over previously reported approaches [3-9] that it can achieve very high dB output voltage range, and the transconductance and the input range can be controlled by the bias current I_0 . The proposed circuit can achieve 58 dB ranges and 46 dB with the linearity error less than ± 0.5 dB at low-power consumption (less than 0.8 mW) and low-voltage applications (less than 1.5 V). The proposed circuit can be used for the design of extremely low-voltage and low-power VGAs and AGCs.

6. REFERENCES

- [1] R. Harijani, "A Low-power CMOS VGA for 50 Mb/s Disk Drive Read Channels," *IEEE Trans. Circuits and Syst.* vol. 42, no. 6, pp. 370-376, June, 1995.
- [2] K. M. Abdelfattah and A. M. Soliman, "Variable Gain Amplifier Based on a New Approximation Method to Realize the Exponential Function," *IEEE Trans. Circuits Syst.*, vol. 49, no. 9, Sep 2002.
- [3] H. Elwan, A. M. Soliman, and M. Ismail, "A. digitally controlled dB-linear CMOS variable gain amplifier," *Elect. Lett.*, vol. 35, no.20, pp. 1725-1727, 1999.
- [4] A. Motanemd, C. Hwang and M. Ismail, "CMOS exponential current-to-voltage converter," *Elect. Lett.*, vol. 33, no. 12, pp. 998-1000, 5th June, 1997.
- [5] Quoc-Hoang Duong, T.Kien N, and Sang-Gug Lee, "Low-Voltage Low-Power High dB-Linear CMOS Exponential Function Generator Using Highly-linear V-I Converter," *IEEE International symposium on Low Power Electronics and Designs*, pp. 349-352 August 2003.

- [6] Cheng-Chieh Chang and Shen-luan Liu, "Current-mode pseudo-exponential circuit with tunable input range," *Electronic Letter*, vol. 36, no. 16, pp 1335-1336, 3rd August, 2000.
- [7] W. Liu, C. Chang, and S. Liu, "Realization of Exponential V-I Converter using composite NMOS transistors," *Elect. Let.*, vol. 36, no. 1, pp. 8-10, 6th Jan, 2000.
- [8] Quoc-Hoang Duong and Sang-Gug Lee, "A low-voltage, low-power, and high db-linear all CMOS exponential function generator for AGC and VGA applications," *IEEE, AMPC'03 Conference*, pp 413-416, November 2003.
- [9] Quoc-Hoang Duong and Sang-Gug Lee, "All CMOS Current-Mode Exponential Function Generator With Tunable Input Range," will be presented at IEEE ICACT04, Feb, Korea.
- [10] K. Bult and H. Wallinga, "A Class of Analog CMOS Circuits Based on the Square-Law Characteristic of an MOS Transistor in Saturation," *IEEE J. of Solid-State Circuits*, vol. sc-22, no. 3, June 1987.

7. ACKNOWLEDGEMENT

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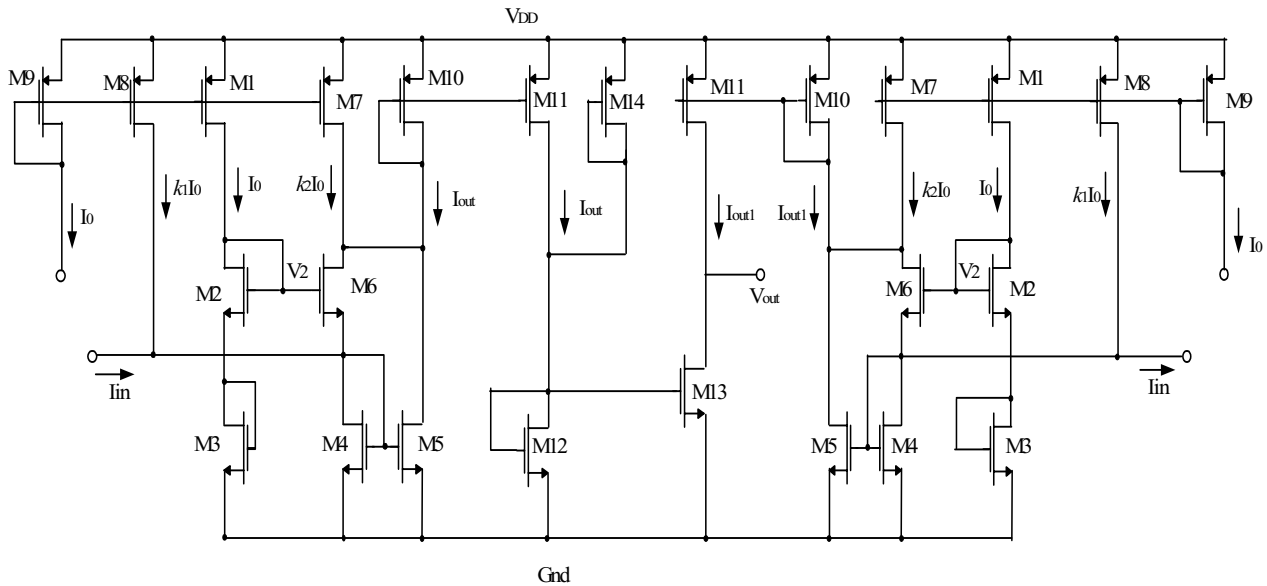


Fig. 4 The newly proposed current-to-voltage converter.

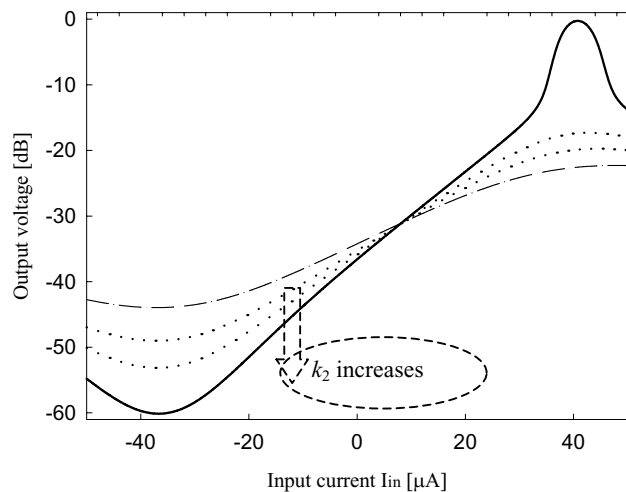


Fig. 5 The I-V characteristics of the proposed circuit shown in Fig. 4 for $I_0 = 35\mu\text{A}$, $k_1 = 1$, and various k_2 .

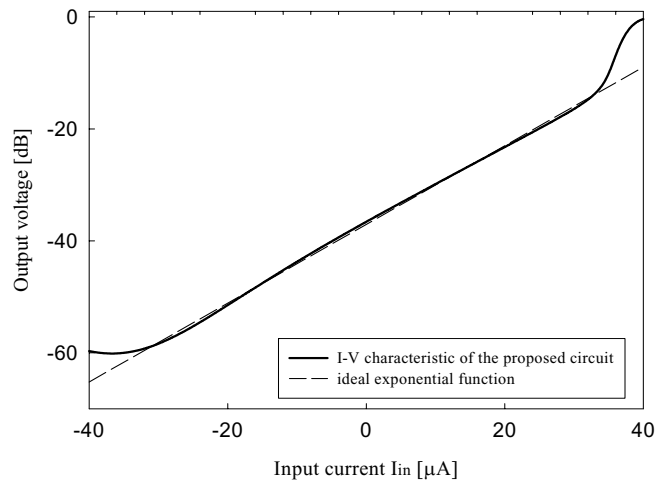


Fig. 6 The I-V characteristics of the proposed circuit shown in Fig. 4 for $I_0 = 35\mu\text{A}$, $k_1 = 1$, and $k_2 = 0.65$.