26.3 Burst-Mode Receiver for 1.25Gb/s Ethernet PON with AGC and Internally Created Reset Signal

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The recent introduction of an Ethernet passive optical network (EPON) brings about design challenges for the IC designer, especially the receiver IC in an optical line terminal (OLT) uplink. The receiver has to receive burst signals with different amplitudes requiring both high sensitivity and wide dynamic range in burst-mode operation.

The block diagram of the proposed receiver is depicted in Fig. 26.3.1. The receiver consists of a transimpedance amplifier (TIA), a single-to-differential amplifier (S2D), several limiting amplifiers (LA) and a buffer for LVPECL output matching. Dc coupling between curcuits is required for burst-mode operation. The S2D is a differential amplifier with its main input receiving a signal from the TIA and its auxiliary input biased at the dc level of the TIA output. The dc level is detected at the beginning of a burst by top-hold (TH) and bottom-hold (BH) circuits and a resistive divider [1] as shown in Fig. 26.3.2. Hence, the outputs of the S2D stage are roughly differential. The LAs are also differential amplifiers; therefore the outputs of the receiver are virtually symmetric.

The TIA uses a cell-based AGC concept [2] with some modification. For the TIA schematic shown in Fig. 26.3.2, the variable feedback network consists of R_{FIX}, R_{AGC}, M_{FB} and C_{FB}. Depending on the dc level of TIA output, the gain control circuit (GCC) generates a bias voltage to control V_{GS} of M_{FB}, thereby controlling total feedback resistance and thus the TIA gain. The dc level of the TIA output is chosen for AGC operation as this level has a shorter settling time than the bottom-hold level in [2]. In addition, resistor R_{FIX} sets a minimum transimpedance gain and, along with a small capacitor C_{FB}, helps to improve the stability at high frequencies. The TH and BH circuits, which employ a super diode configuration, are discussed in [1] and [3].

To avoid offset being accumulated and amplified in S2D and LAs, each of them has its own auto-offset-cancellation function (LA-AOC). All the LA-AOCs have the same topology and detailed operation is discussed in [1].

For burst-mode operation, the TH, BH and all the LA-AOCs are reset before each burst. The new EPON standard adopts a dynamic bandwidth arrangement in which burst timing is not fixed; thus obtaining the reset timing from network layer complicates system design significantly It is desirable to create a reset signal on-chip based on the incoming burst signal only.

In an EPON system, upstream signals contains bursts with different amplitudes and between bursts are the periods with no signal (gap time). Based on this characteristic, reset signal can be created on-chip. Figure 26.3.3 shows reset-creation circuit topology. With a bottom-level envelope (BLE) detector connected to one output, the resultant envelope signal rises up during gap time, and falls down during the burst period. In Fig. 26.3.3, the envelope signals of both outputs are compared to reference levels located between the signal's high and low values. From the comparators' outputs, with some additional digital circuits, internal reset is turned on during gap time between bursts and turned off during burst period. To change reset from on to off at the beginning of a burst, especially a burst with small amplitude, the receiver needs adequate gain to creates a sufficient output swing to lower the envelope signal. The TH, BH and LA-AOCs circuits are designed with this consideration.

The proposed receiver is fabricated in 0.18μm CMOS technology with all components on-chip and tested in a chip-on-board configuration. A pig-tailed photodiode with intrinsic parasitic capacitance of 1pF is used in the module. If a die photodiode without additional package parasitic capacitance is used instead, the receiver has a larger bandwidth and lower noise. It is a normal practice to package the die photodiode and receiver IC in a high-frequency pig-tailed butterfly module. The Agilent ParBERT 81250 parallel BER tester is used to test burst-mode performance.

The measured waveforms at two outputs and an anticipated reset signal are depicted in Fig. 26.3.4. After a burst finishes, the bottom-level envelope detector needs a period to catch up with the output signal, thereby creating delay in the reset turn-on. Similarly, when a new burst comes in, the first part of the burst signal is distorted due to the delay in reset turn-off. The abrupt change of the output signal in the gap time indicates reset-turn-on, and a fast increase of output swing during burst time indicates reset-turn-off. The waveforms also show negligible offset between the two differential outputs.

With photodiode responsivity of 0.85A/W, the receiver shows sensitivity of -22dBm and overload of -3.5dBm with BER < 10^{-12} and 2^{23}-1 random sequence. Loud/soft ratio, the ratio between the largest and the smallest amplitudes of consecutive bursts that the receiver can detect properly, is 17.5dB. A summary of the receiver's performance is given in Fig. 26.3.5. All timing parameters are better than the requirement in the current IEEE 802.3ah standard [4].

Figure 26.3.6 shows the single-ended output eye diagrams at different burst amplitudes. The first two eye diagrams are measured under loud/soft ratio of 18.5dB. The last eye diagram belongs to a normal condition.

To the best of authors' knowledge, this work is the first reported burst-mode receiver IC for 1.25Gb/s EPON system, especially with an internally created reset signal. An improved version is currently in development and focused on improving sensitivity. The die photograph is shown in Fig. 26.3.7, with die size of 0.9mm x 1.9mm.

References:

[1] Quan Le, Yong-Hoon Oh and Sang-Gug Lee, "Integrated Differential Preamplifier for 155Mb/s ATM-PON System with Fast Response, High Sensitivity and Wide Dynamic Range," *Asia-Pacific Microwave Conference (AMPC)*, vol. 2, pp. 478-481, Nov. 2002.
[2] S. Yamashita et al., "Novel Cell-AGC Technique for Burst-Mode CMOS Preamplifier with Wide Dynamic Range and High Sensitivity for ATM-PON System," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 881-886, July 2002.
[3] M.Nakamura et al., "A 156-Mb/s CMOS Optical Receiver for Burst-Mode Transmission," *IEEE J. Solid-State Circuits*, vol. 33, no. 8, pp. 1179-1187, Aug. 1998.
[4] IEEE 802.3ah Draft Standard , May 2003.

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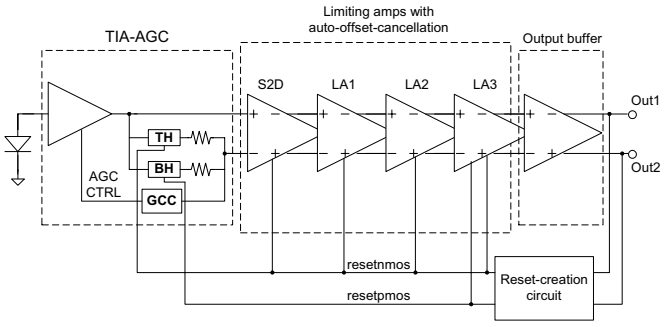

Figure 26.3.1: Receiver block diagram.

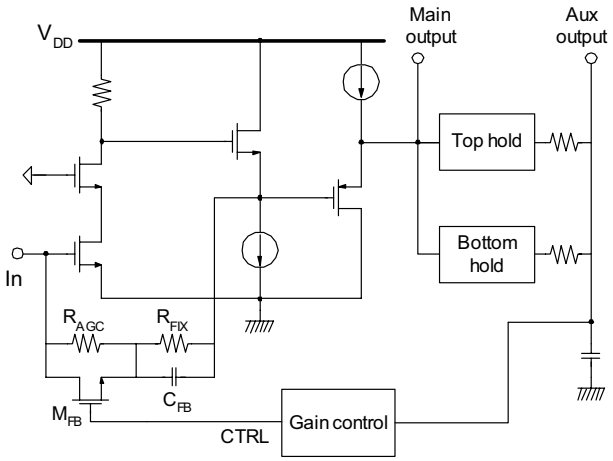

Figure 26.3.2: TIA-AGC circuit.

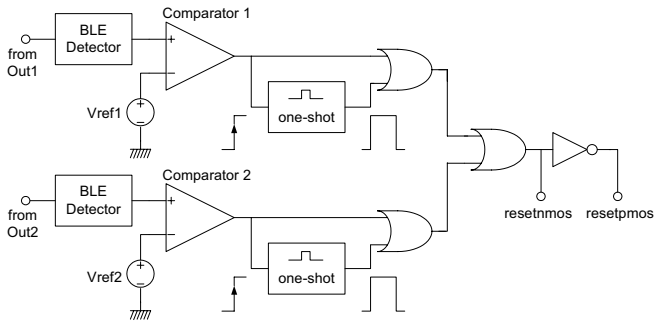

Figure 26.3.3: Reset creation circuit.

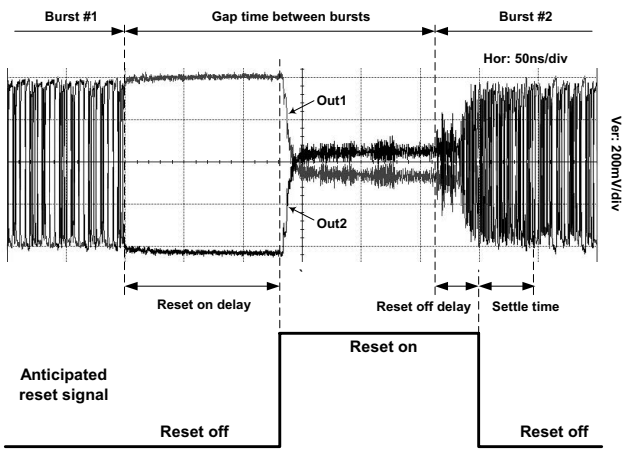

Figure 26.3.4: Measured waveforms at two outputs and anticipated reset signal.

Spec	Standard	This work	Note
Sensitivity	-24dBm	**-22dBm**	
Overload	-3dBm / -5dBm	**-3.5dBm**	Short range / Long range
Loud/soft ratio		**17.5dB**	Btw consecutive bursts
Ton	512ns	**250ns**	Gap time between bursts
Treceiver - settling	400ns	**50ns**	After reset off
Output level		**LVPECL compliant**	Matched to LVPECL interface
Power consumption		**160mA from 3.3V source**	

Figure 26.3.5: Summary of receiver performance.

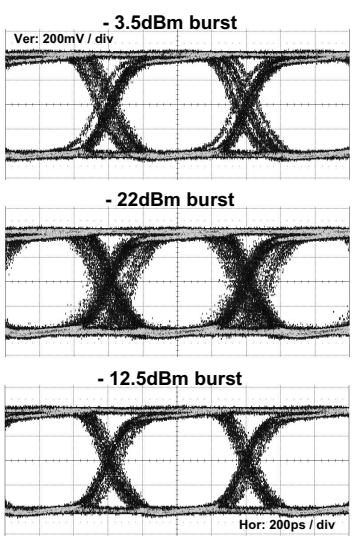

Figure 26.3.6: Eye diagram of 2^{23}-1 random data at different optical signal level.

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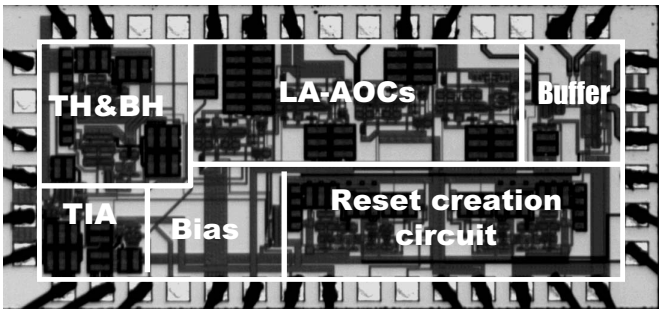
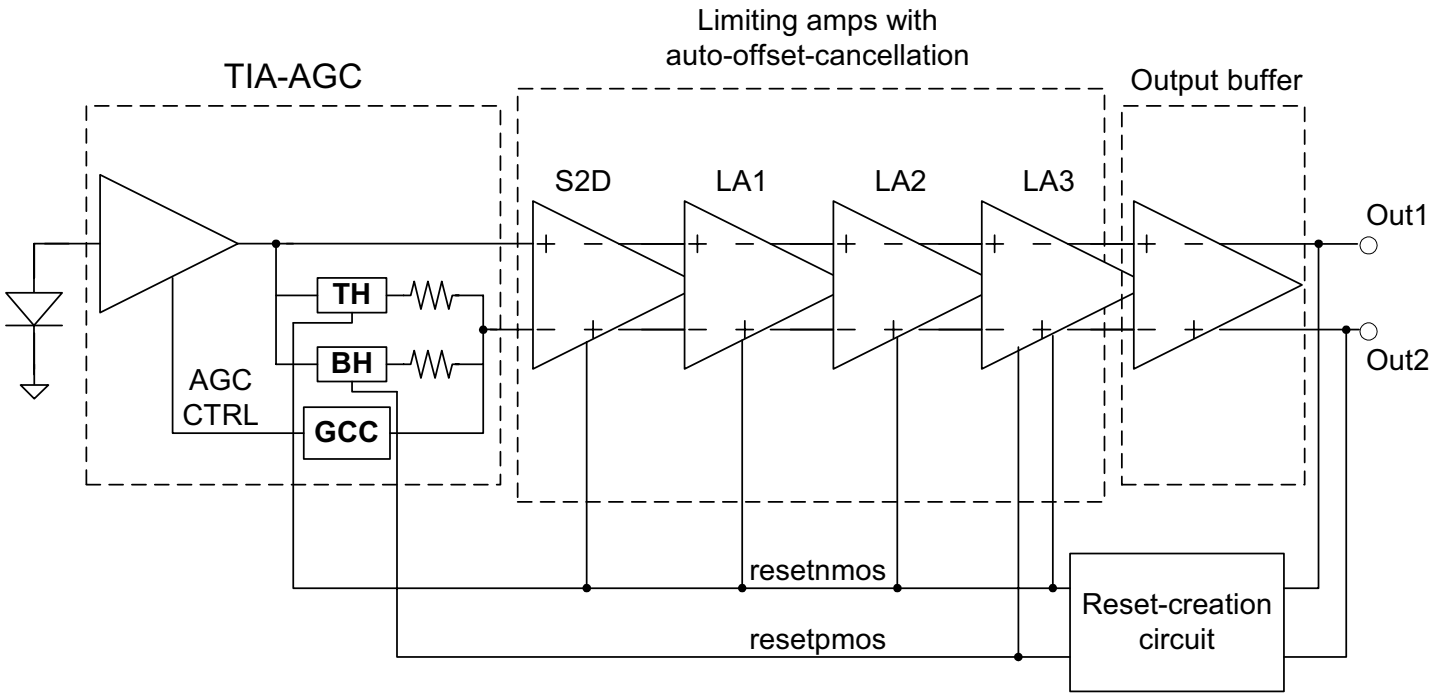


Figure 26.3.7: Die photo of receiver IC.



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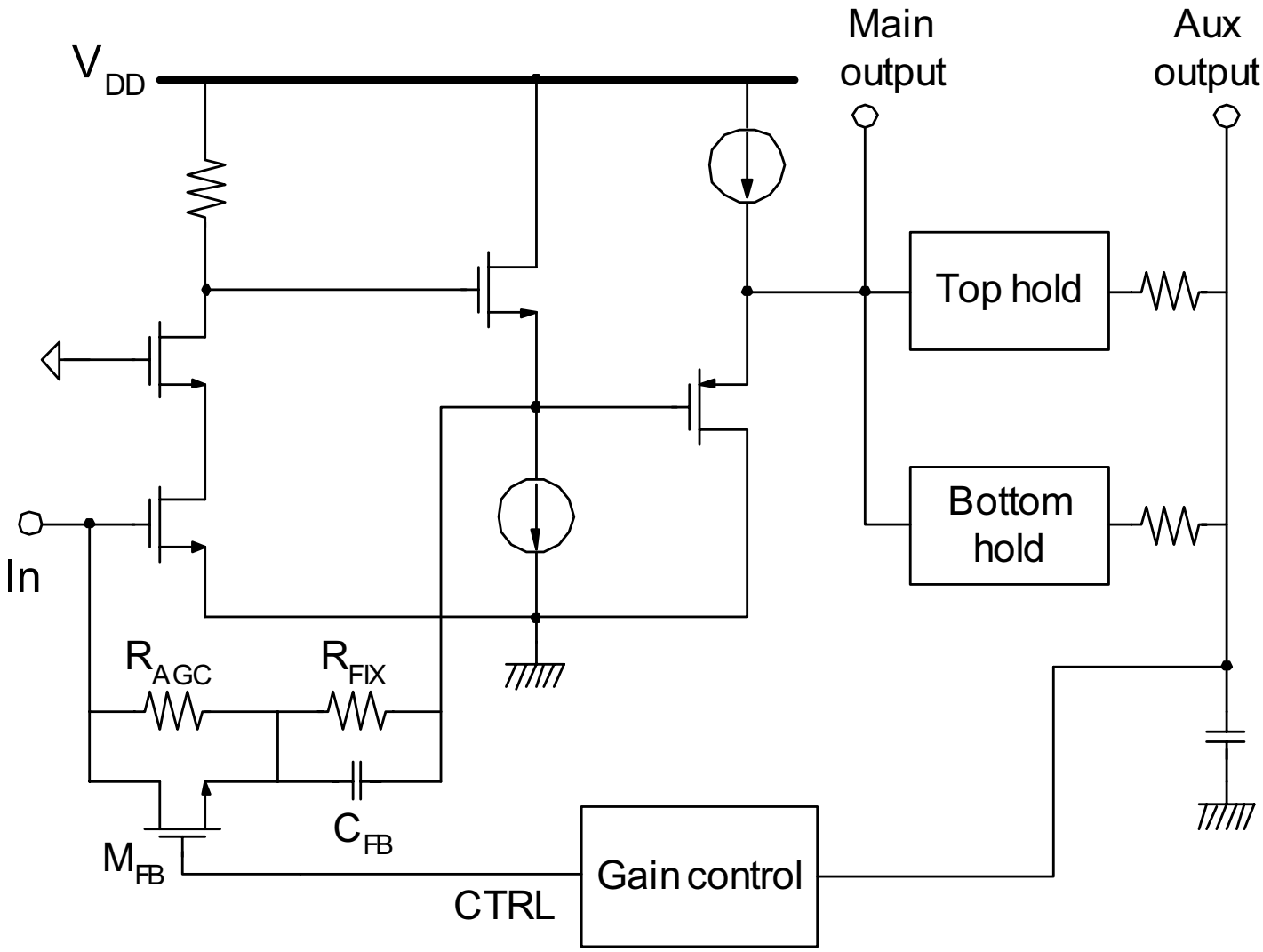


Figure 26.3.2: TIA-AGC circuit.

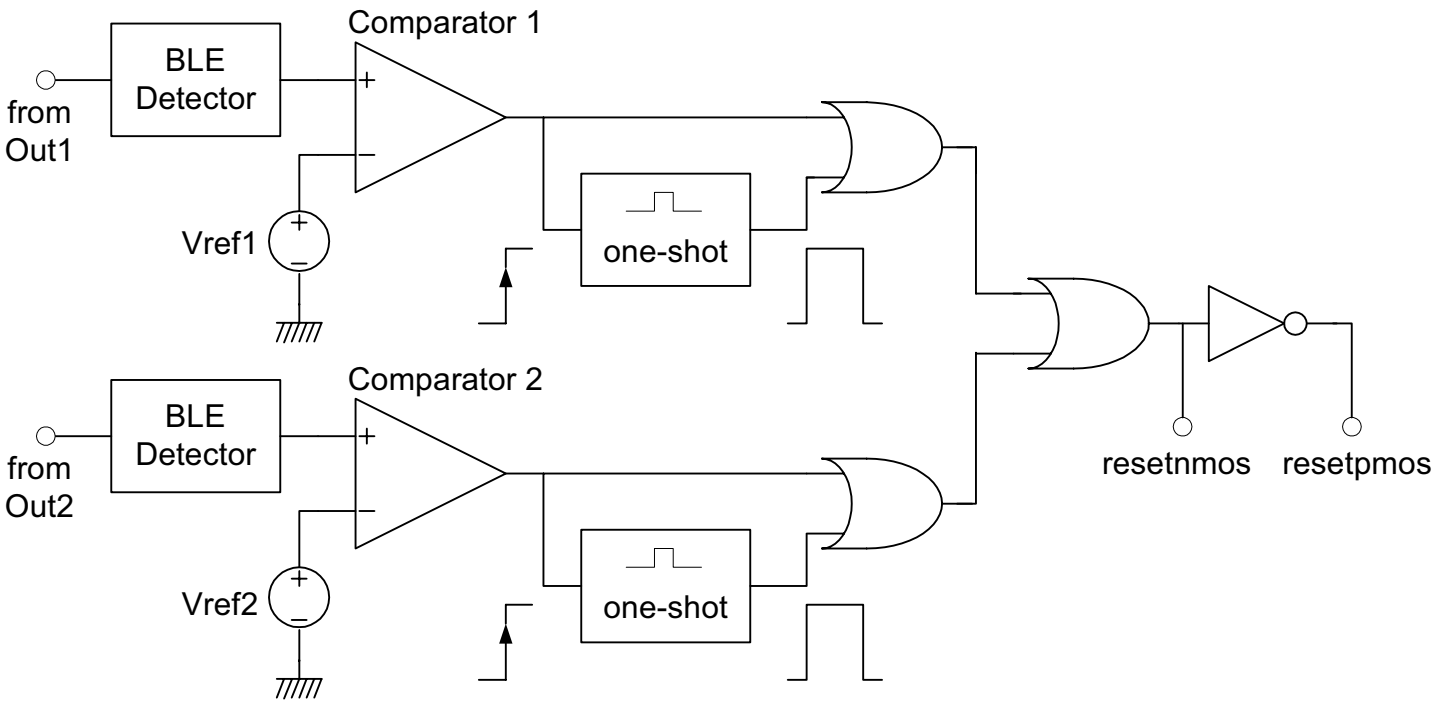
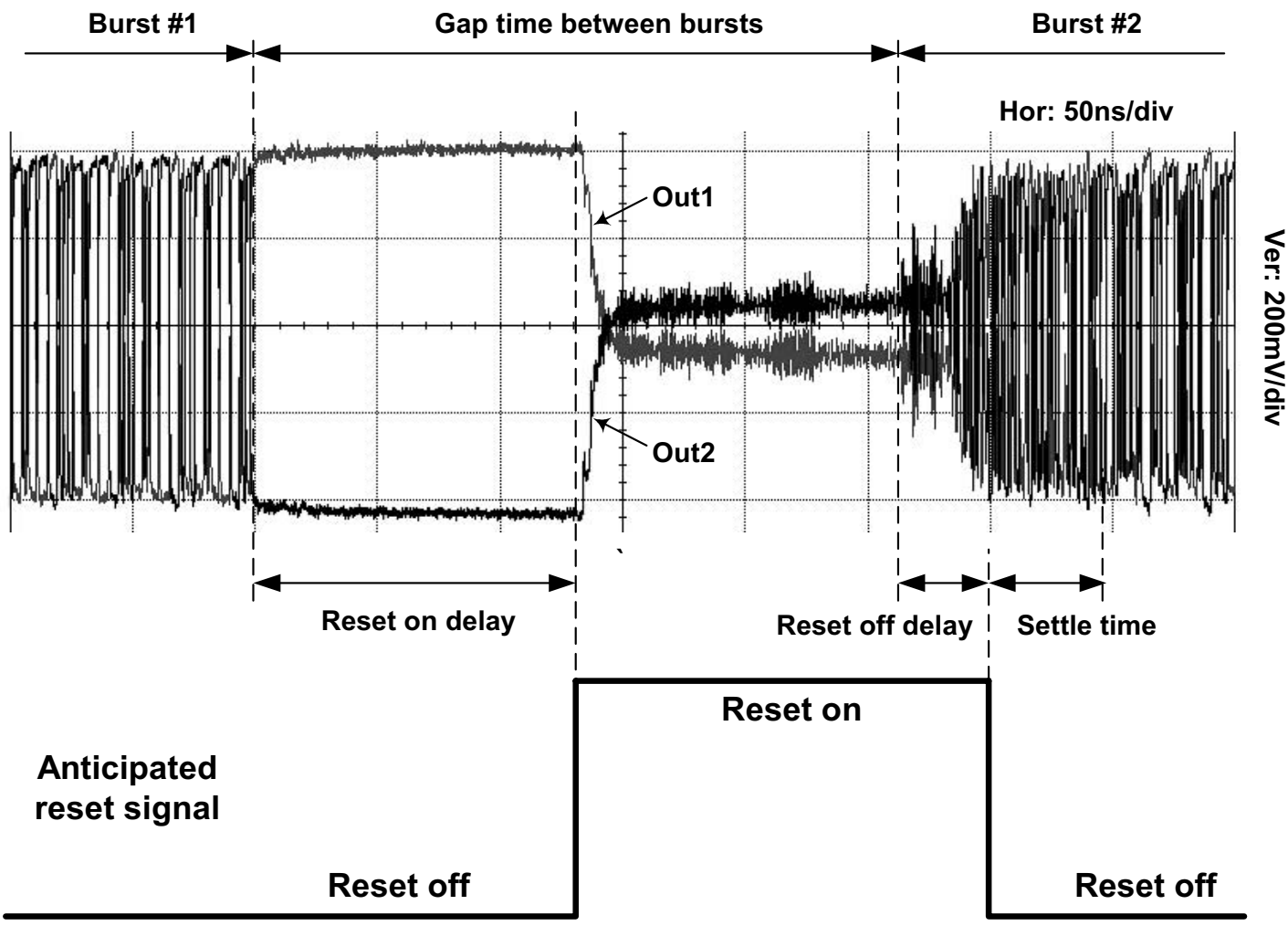


Figure 26.3.3: Reset creation circuit.



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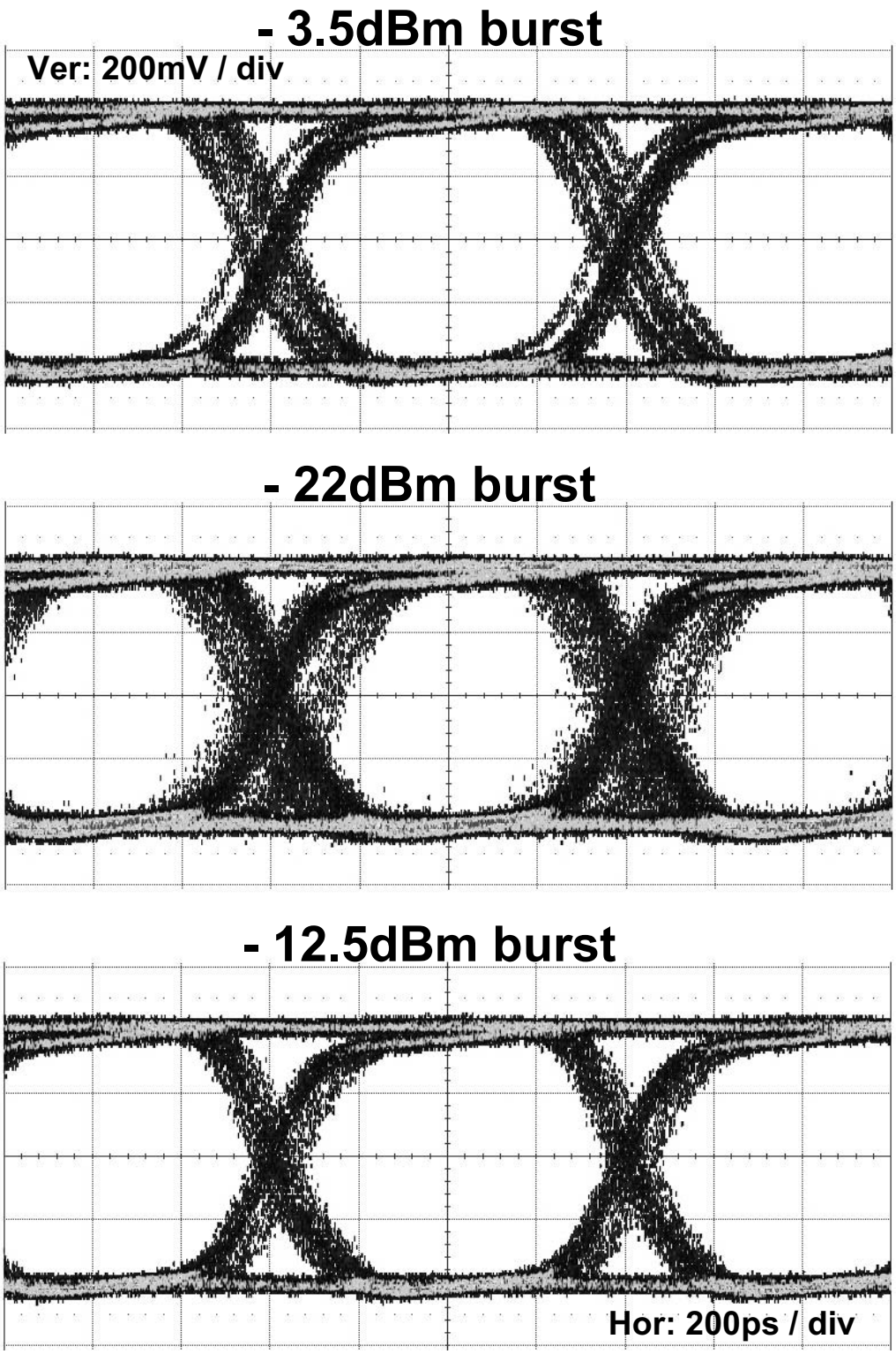

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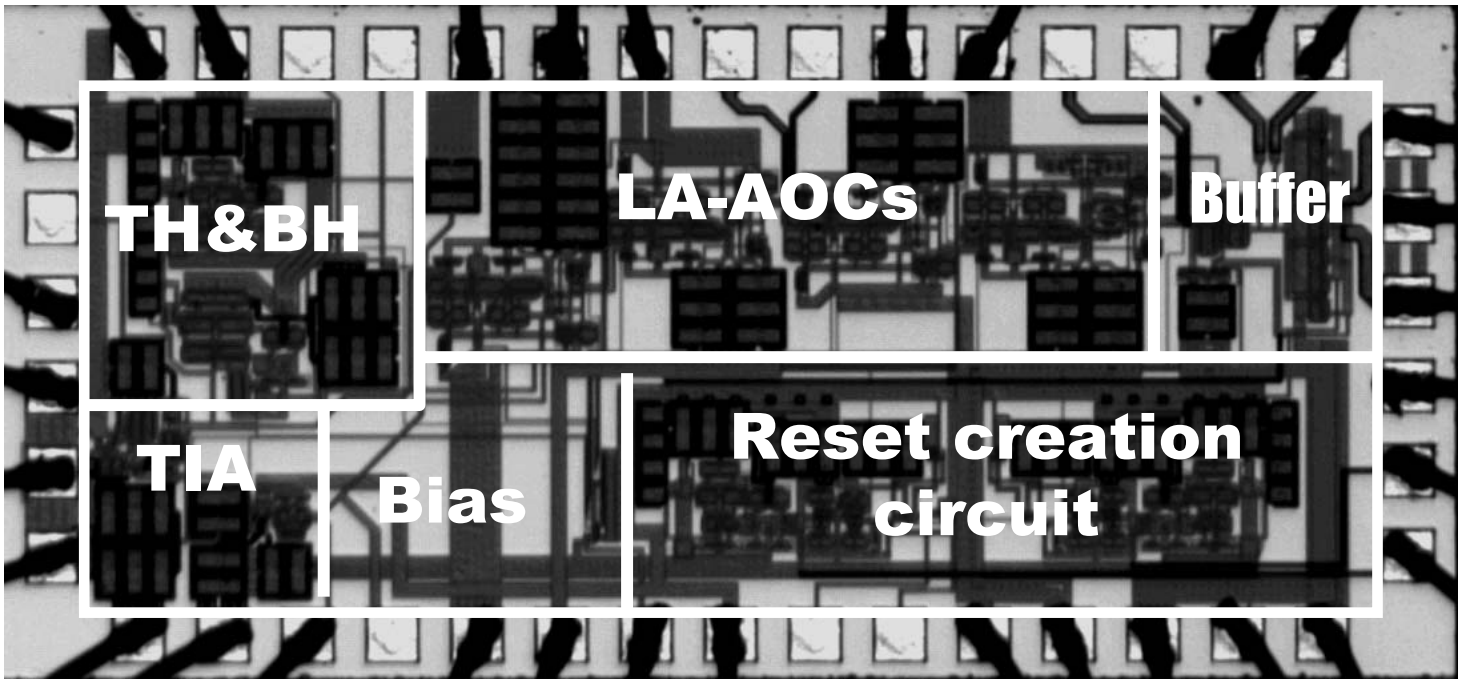

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