Low Noise And High Gain CMOS Down Conversion Mixer

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Abstract — **This paper represents a lowest noise ever high gain CMOS direct down-conversion mixer for 1.8 GHz applications like GSM, PCS... based on 0.18 μm CMOS technology. The designed mixer uses the current bleeding technique and an extra inductor to improve the conversion gain, noise figure (NF). Also, with an extra inductor and the careful choosing of transistor sizes, the mixer has a lowest - ever reported flicker noise. The simulation results show the voltage conversion gain of 28.2 dB, the single-side band (SSB) NF of 4.09 dB. Flicker noise cut-off frequency is just a few kHz. SSB NF at 50 Hz reaches 16.8 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 11.34 mW.**

Keywords: CMOS design, down-conversion, noise, mixers, flicker noise, transceivers.

I. INTRODUCTION

In the past few years, mobile phone market has seen a significant growth. As the industry transit from 2G to 3 G, a number of applications and features are introduced. The size of cellular phone is smaller with higher speed data, multimedia applications and longer battery. That is due to the emerge of direct conversion architecture.

Direct down conversion architecture allow the reduction of number of off-chip components allowing higher integration level, minimizing power consumption. Beside the advantages, it suffers from number of challenges, like DC offset, second order distortion, self mixing and flicker noise in base band [1].

In direct conversion receiver (DCR), flicker noise is a critical issue. For CMOS the flicker noise is high, around 1 MHz of cut-off frequency [1] and 1/f noise tends to corrupt the output base-band signal by degrading the system Noise Figure. Therefore the lower the bandwidth, the higher the degradation is likely to be. Such that, for the narrow band applications like GSM, PCS...the 1/f noise corner frequency needs to be as small as possible since the signal exists at DC after the frequency translation.

In a receiver system, the down-conversion mixer is the key building block since it dominates the system linearity, noise figure, and determines the performance requirements of its adjacent blocks. Among many proposed active mixers, the Gilbert-cell mixer has been widely used so far, and the double-balanced mixer topology has been preferred since it can suppress (LO) leakage signals at the output (Fig. 1). The down-conversion mixer is required to provide a low noise figure and high conversion gain. The simultaneous achievement on these requirements is a very challenging task in the mixer design

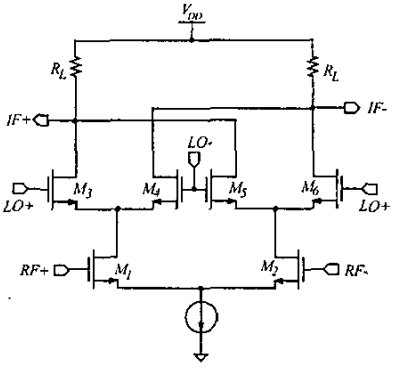

Figure 1. Double-balanced Gilbert-type mixer topology

NF is an important factor limiting the sensitivity of system in the receiver. It can be reduced by increasing the drain current but it will lead to high power consumption. Also, higher gain and better linearity can be achieved by increasing the bias current through the transconductance stage [2], but the power consumption can be excessive. Better techniques to improve conversion gain with the constrained power have been introduced, where some sort of current bleeding techniques are utilized [3,4].

Furthermore, in the mixer, the switching transistors primarily determine the flicker noise performance. There are two dominant mechanisms that the flicker noise of the switching transistors appears at the mixer output, they are direct and indirect mechanisms [5]. The first mechanism is that, the contribution of 1/f noise is from the finite slope of switching pairs [6]. In the indirect mechanism, output flicker noise depends on the frequency and circuit capacitance at the common source node of the switching stage. Our approach is to reduce the flicker noise. By adding an extra inductor, mentioned in [7], the capacitances are reduced leading to reduction in 1/f noise and improve the gain.

In this paper, a 1/f noise reduction down conversion mixer applied for narrow band applications in DCR is designed. The conversion gain is improved by applying the

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current-reuse bleeding technique in [4]. A critical improvement in flicker noise can be achieved by using an extra inductor. The designed direct-converted mixer achieves a very good performance with the voltage conversion gain of 28.2 dB, SSB NF of 4.09 dB at 5 MHz and 16.8 dB at 50 Hz. 1/f noise cut off frequency is only a few kHz. The proposed mixer is implemented based on 0.18 μm CMOS technology under a supply voltage of 1.8V supply, and dissipates dc current of 6.3 m A.

II. PROPOSED MIXER TOPOLOGY AND DESIGNED

The double-balanced Gilbert-type mixer topology shown in Fig. 1 is preferred in CMOS mixer design since it suppresses the LO signal and the even order distortion products at the output.

In overall mixer design, higher gain, higher linearity, lower noise and low power consumption are required. However, these parameters are difficult to achieve simultaneously. Higher gain and better linearity can be achieved by increasing the drive current through the transconductance stage [2], but power consumption will be increased. Furthermore the larger current through the switching quads causes voltage headroom problems especially if resistive loads are used. The larger amount of current through the switching quads mandates the larger LO drive voltage, which is troublesome in the CMOS technology, since it is not easy to get the large enough voltage swing at high LO frequency.

In this design, current bleeding technique is utilized, PMOS transistors M_7 and M_8 create the bleeding currents under the gate bias voltage as shown in Fig. 3

With the bleeding technique, the current through switching transistor is reduced, such that the 1/f noise is improved and the output load resistance is increased leading to a higher gain [4].

Also, the bias current through the transconductance stage can be increased without increasing the current through the switching transistors. The bleeding technique relaxes the voltage headroom problem, and allows smaller LO drive voltage applied to the switching transistors for switching efficiency.

With the bleeding current, the gain is high, that contributes to lower the NF at the output.

However, the mixer topology shown in Fig. 1 has some drawbacks due to the parasitic capacitance at the drain nodes of the transistors pair M_1-M_7 and M_2-M_8. Those parasitic capacitances lead to the reduction of the transconductance and cause the flicker noise such that the conversion gain and NF of mixer are degraded. The designed circuit added an inductor that can be used as the solution to overcome the drawback caused by those parasitic capacitances. This inductor was mentioned in [7]. The mixer topology in [7] is used for Ultra Wide Band (UWB) system, which has a very large bandwidth. In UWB, the flicker noise affects negligibly to the system because of its large bandwidth. But in narrow band application like GSM, PCS which are based on direct conversion architecture, 1/f noise has a vital role. So significant 1/f noise reduction achieved in this design is a progress in CMOS circuit design, particularly in DCR for narrow band applications. This technique can be illustrated briefly by using the simplified single balance mixer in Fig. 2.

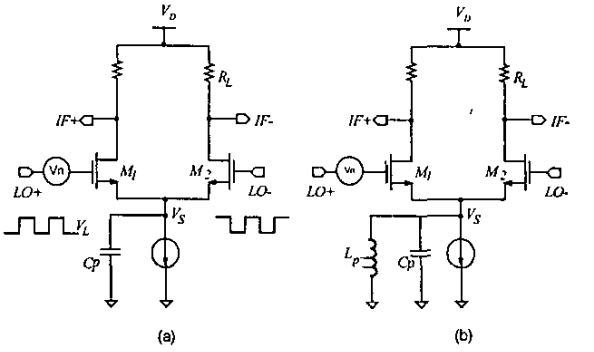

Figure 2. Indirect mechanism for 1/f noise

As mentioned above, in indirect mechanism, output flicker noise depends on the capacitance at the common source node of the switching stage C_p. In order to reduce flicker noise we have to reduce C_p. In Fig. 3, L_p is added in parallel with C_p, by resonating, C_p is suppressed.

The proposed mixer topology is shown in Fig. 3. In this topology, the inductor L_1 is added, the value of L_1 is twice the value of L_p. By parallel resonating with the inductor L_1 at LO frequency, C_p is reduced as well as the effects of current through it. The flicker noise caused by this effect is suppressed. Under resonant conditions, the conversion gain and NF of the mixer are improved.

From [5] we have the input referred flicker-noise voltage (V_n) is:

$$V_n = \sqrt{2x\frac{K}{W_{eff}.L_{eff}.C_{ox}.f}} \qquad (1)$$

Where K is technological parameter, W_{eff}, L_{eff} are effective width and length. C_{ox} is the oxide capacitance with frequency f.

V_n is inversely proportional to gate area. To minimize the flicker noise caused by direct mechanism, large switching transistor sizes are used. So the switching transistors of the designed mixer have the length of 0.35um and width of 280um.

Also, low bias current and overdrive voltage to minimize the switching time are applied. These design is to lower the cut off frequency of switching devices [6].

The gates of switching transistors are biased near threshold in order to minimize the switching time, this factor permits the reduction of LO power and makes the switching more ideal. Non-ideal switching, such as when the switch is not completely turn on and off, will reduce the conversion gain and increase the noise figure [2, 3].

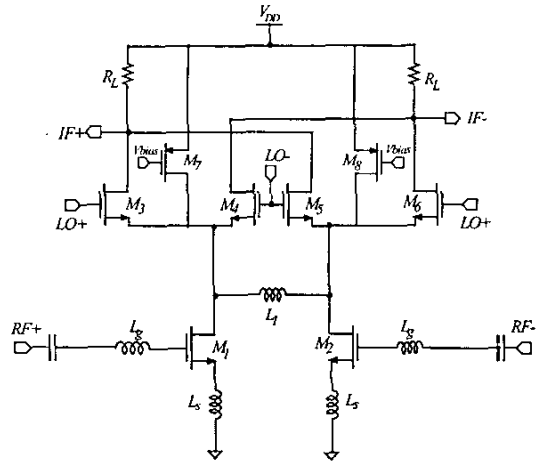

Figure 3. The proposed down-conversion mixer topology

The resistive load is used because it is free of flicker noise. To restrict the power consumption, the size and V_{GS} of transistor M_1 and M_2 are chosen carefully. But if V_{GS} is too low, the gain and linearity will be degraded.

However, by adding L_1, the proposed mixer has very good performances compared to previously reported designs in terms of noise and conversion gain, shown in Table. 1.

Lg and Ls are for input impedance matching at 50 Ohm, Ls inductor is the bonding wire, it helps decrease the noise figure and increase the third order input intercept point (IIP3) [2].

The LO to RF isolation is 57.3 dB, this isolation helps to reduce the DC offset in the down mixer. The LO to IF isolation is 115 dB, the high isolation is to prevent the saturation of signal at output stage that degrades P1dB.

III. SIMULATION RESULTS AND DISCUSSION

The proposed mixer in Fig. 3 is simulated in a TSMC 0.18 μm CMOS process by Cadence. The results are shown below.

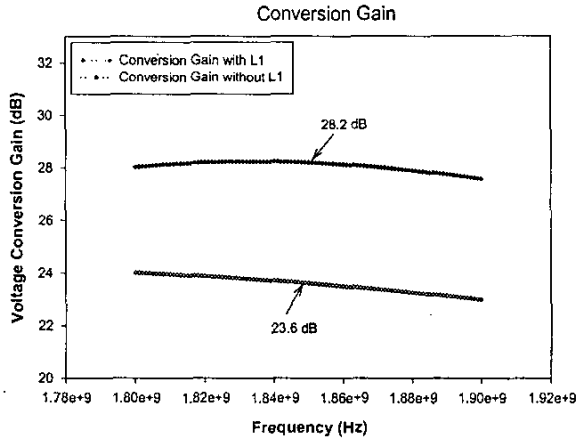

Figure. 4. Conversion Gain

In Fig. 4, the simulation shows the conversion gain increases by 4.6 dB when L_1 is added in the circuit, 28.2 dB at center frequency band. In the circuit, L_1 is an on chip inductor with the optimum value of 3.4 nH.

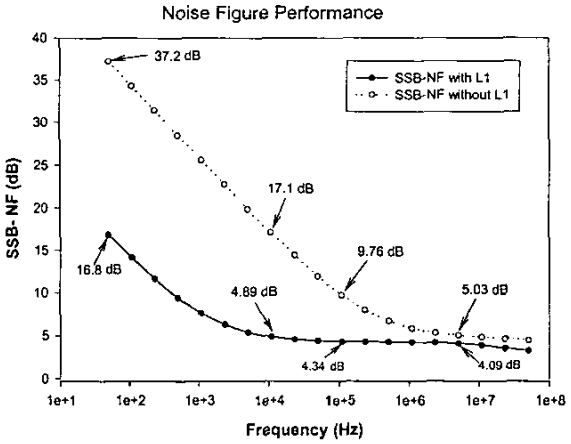

Figure 5. SSB Noise Figure

The most effective improvement in the designed mixer when applying the technique mentioned in [7] is on flicker noise.

The flicker noise is very low, at the frequency of 10 kHz the noise is only 4.89 dB, the corner frequency is reduced from nearly 1MHz to a less than 10 kHz. With an extra inductor L_1, the overall thermal noise or NF is improved by 0.94 dB, SSB NF simulated at 5MHz is 4.09 dB. The 1/f noise at 10 kHz is improved by 12.21 dB, at 100 kHz is by 5.42 dB and much more near DC, about 20 dB. SSB NF simulation is shown in Fig. 5, at 50 Hz, SSB NF is only 16.8 dB.

With the great improvement of the flicker noise, this mixer topology is really suitable for narrow band applications based on direct conversion architecture, which often suffers from 1/f noise. For GSM, the channel bandwidth is 200kHz, but the 1/f noise corner frequency occupies only about 10kHz around DC so the attenuation of signal caused by flicker noise is negligible.

Also, the 4.09 dB of SSB NF achieved from simulation is the lowest ever published value to date for CMOS mixer circuits. Of course, when measuring the real chip circuit, unexpected parasitic components will cause the variations. But the measured results will not be much different from the simulations since the simulations were done with the real model, and post simulations were also carried out.

In Table.1, important parameters like NF, conversion gain and linearity of the proposed mixer are compared with those in [2,3,6,8,9]. The table shows that the performance is much better than previous works however power consumption is still at a reasonable level, 11.34 mW.

Table. 1. Performance Comparison

Parameters	This Work	[2]	[3]	[6]	[8]	[9]
Frequency (GHz)	*1.85*	2.45	2	0.9	0.92	1.8
Supply Voltage (V)	*1.8*	1.8	1.8	2.7	1.8	2.2
Power Consumption (mW)	*11.34*	-	12.06	16.2	16	10.34
(1) Input IP3 (dBm)	*0*	-3.7	10	-4	-5	6.7
(2) Voltage Conversion Gain (dB)	*28.2*	27	14	18	20	10.6
(3) SSB NF (dB)	*4.89*	12.5	9.5 (DSB)	18	4.3 (DSB)	10.3 (DSB)
(1) + (2) - (3)	*23.31*	13.8	13.5	-4	10.7	7

From the above table, the designed down conversion mixer has an outstanding performance, especially the SSB Noise Figure, compared to other previously reported designs.

IV. CONCLUSION

The new down conversion mixer topology for GSM-1800 was designed and compared its performance to those of previously published papers. The mixer topology, designed and manufactured in 0.18 μm CMOS process, shows an excellent performance, particularly in NF. It is suitable for direct conversion architecture since it provides low NF, low 1/f noise and high conversion gain. To achieve higher conversion gain, the bleeding technique is applied and 1/f noise is improved significantly by using an extra inductor. Its function is to reduce the parasitic capacitance at the source terminal of the switching stage such that the conversion gain and NF are improved furthermore.

Some simulated parameters, like NF is better than reported papers. Predicted mixer's SSB NF as low as 4.09 dB is particularly interesting. Very low 1/f noise corner frequency is really suitable for narrow band, direct-conversion structure for applications like GSM, PCS...

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