CMOS Low Noise Amplifier Design Optimization Technique

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Abstract

In this paper, a set up noise parameter expression and the third order intermodulation product expression (IM3) for a power-constrained simultaneous noise and input matching low noise amplifier design optimization technique are introduced. Based on these expressions, the methodology to design LNA to archive the power-constrained simultaneous noise and input matching as well as satisfy the linearization condition is explained. In additional, the power gain is enhanced by using a very simple positive feedback. The proposed LNA for 5GHz WLAN applications is fabricated based on 0.18 μm CMOS technology. Measured results show 20 dB power gain, 1.5 dB NF and –5 dBm IIP3. The proposed LNA dissipates DC current of 3 mA at supply voltage of 2.5 V.

1. Introduction

With the recent proliferation of wireless transceiver applications, there is an extensive effort to develop low cost, highly integrated RF circuits. CMOS has become a competitive technology for radio transceiver implementa-tion due to the technology scaling, higher level of integrability, lower cost, etc. [1]. In typical receiver architectures, a low noise amplifier (LNA) is the one of the most critical blocks that determines the sensitivity of wireless receiver systems [2-[4]. Normally, LNA design involves the tradeoff between noise figure (NF), gain, linearity and power consumption. Consequently, the goal of LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation as well as satisfy the linearization conditions. The LNA design optimization technique proposed in [4] can be applied for power-constrained simultaneous noise and input matching. However, as discussed in [4], the fully potential of this technique is not provided clearly. This paper attempts to analyze and provide clear and perspe-ctive understanding one of the LNA design optimization techniques, namely power-constrained simultaneous noise and input matching technique. The analyses are based on the noise parameter expressions and the expression for the third order intermodulation product (IM3). By using those expressions, the design principle, advantages and practical limitation for the mentioned LNA technique are explained. In additional, in this paper, the power gain of the LNA is improved by using simple positive feedback technique. The simple positive feedback is implemented by one additional capacitor connected from drain terminal of the cascode transistor to that of common source transistor. The description of the methodology for LNA design optimization and the proposed LNA are discussed in detail in section 2 and 3, respectively. The proposed LNA for 5 GHz WLAN applications is fabricated based on 0.18 μm CMOS technology. Measured results show 20 dB power gain, 1.5 dB NF and –5 dBm IIP3. The proposed LNA dissipates the DC current of 3 mA at supply voltage of 2.5 V.

2. Methodology for Low Noise Amplifier Design

A. Noise Optimization Analysis

Figure 1-a shows the schematic of a cascode LNA topology that is adopted to explain the PCSNIM LNA design technique. The LNA shown in Fig. 1-a differs by one additional capacitor C_{ex} in comparison with the typical cascode LNA.

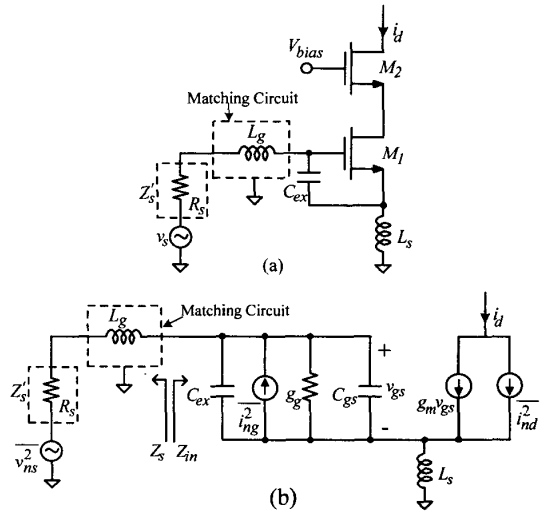

Fig. 1. Simple cascode LNA to adopt the PCSNIM technique (a) and its small-signal equivalent circuit (b)

This LNA topology was first introduced in [3] as a solution to reduce the noise figure of the LNA at low power dissipation, however, the potential and the theoretical analysis as a power-constrained (i.e., low power) simultaneous noise and input matchable LNA topology has not been recognized. Fig. 1-b shows the simplified small-signal equivalent circuit of the cascode amplifier shown in Fig. 1-a for the noise analysis. In Fig. 1-b, the effects of common-gate transistor M_2 on the noise and frequency response are neglected [2]. The noise parameter expressions for a circuit with series

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feedback, shown in Fig. 1-b, can be obtained by applying the Kickoff's law [1]. The results are simple enough to provide useful insights as shown below [5]

$$F = 1 + \frac{1}{g_m^2 R_s} \cdot \left\{ \begin{array}{l} \gamma g_{d0} \cdot \left\{ \begin{array}{l} \left[1 + s^2 C_t^2 \left(L_g + L_s \right) \left(1 + |c| \alpha \sqrt{\frac{\delta_{eff}}{5\gamma}} \right) \right]^2 \\ -\left(sC_t R_s \right)^2 \left(1 + |c| \alpha \sqrt{\frac{\delta_{eff}}{5\gamma}} \right)^2 \end{array} \right\} \\ -\frac{\alpha \delta_{eff}}{5} \left(1 - |c|^2 \right) g_m \left(sC_t \right)^2 \left(R_s^2 - sL_g^2 \right) \end{array} \right\} \quad (1)$$

$$F_{min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2)} \quad (2)$$

$$Z_{opt} = \frac{\alpha \sqrt{\frac{\delta}{5\gamma(1-|c|^2)}} + j\left(\frac{C_t}{C_{gs}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)}{\omega C_{gs} \left\{ \frac{\alpha^2 \delta}{5\gamma(1-|c|^2)} + \left(\frac{C_t}{C_{gs}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\}} - sL_s \quad (3)$$

$$R_n = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \quad (4)$$

where $C_t = C_{gs1} + C_{ex}$

As can be seen from (2) and (4), F_{min} and R_n are not affected by the addition of C_{ex}. In other word, by using C_{ex}, the minimum noise figure and the noise resistance expressions for power-constrained simultaneous noise and input matching technique are the same as those in [3]. From Fig. 1-(b), the input impedance of the LNA is given by

$$Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_m L_s}{C_t} \quad (5)$$

In (5), the source degeneration generates real part at the input impedance. This is important because there is no real part in the input impedance without degeneration while there is in the optimum noise impedance. Therefore, L_s helps to reduce the discrepancy between the real parts of the optimum noise impedance and the LNA input impedance. Furthermore, from (5), the imaginary part of Z_{in} is changed by sL_s, and this is followed by nearly the same change in Z_{opt} in (3), especially with advanced technology considering the value of c is higher than 0.4 (e.g., $c \approx 0.5$ with 0.25 μm technology), and α becomes lower than 1 [6].

Now, for the circuit shown in Fig. 1-(a), the conditions that allow the simultaneous noise and input matching are

$$\frac{\alpha \sqrt{\frac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{gs} \left\{ \frac{\alpha^2 \delta}{5\gamma(1-|c|^2)} + \left(\frac{C_t}{C_{gs}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\}} = \mathrm{Re}[Z_s] \quad (7)$$

$$\frac{j\left(\frac{C_t}{C_{gs}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)}{\omega C_{gs} \left\{ \frac{\alpha^2 \delta}{5\gamma(1-|c|^2)} + \left(\frac{C_t}{C_{gs}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\}} - sL_s = \mathrm{Im}[Z_s] \quad (8)$$

$$\frac{g_m L_s}{C_t} = \mathrm{Re}[Z_s] \quad (9)$$

$$sL_s + \frac{1}{sC_t} = -\mathrm{Im}[Z_s] \quad (10)$$

As mentioned above, for the advanced CMOS technology parameters, (8) is approximately equal to (10). Therefore, (10) can be dropped, which means that for the given value of L_s, the imaginary value of the optimum noise impedance becomes approximately equal to that of the input impedance with opposite sign. Now then, the design parameters that can satisfy (7)-(9) are V_{GS}, W (or C_{gs}), L_s, and C_{ex}. Since there are three equations and four unknowns, (7)-(9) can be solved for an arbitrary value of Z_s, by fixing the value of one of the design parameters that can be the power dissipation or V_{GS}. In other word, this LNA design optimization technique allows to design simultaneous noise and input matching at any given amount of power dissipation.

B Linearity Analysis

In RF circuit design, the linearity is another important aspect to consider. Since LNA is the first block in the typical receiver system, the linearity of the LNA is commonly estimated by the third order intermodulation product. Two signals of adjacent channels $Asin\omega_1$ and $Asin\omega_2$ will generate products *IM3* such as $Asin(2\omega_1-\omega_2)$ and $Asin(2\omega_2-\omega_1)$ at the output of nonlinear circuit. *IM3* usually calculated in the literature as the ratio of intermodulation of the third order and the response magnitude of the fundamental frequency which is given by

$$IM3 = \frac{3}{4} A^2 \left| \frac{A_3(2\omega_1 - \omega_2)}{A_1(\omega)} \right| \quad (11)$$

where A_1, A_3 are the first order and third order coefficient of Volterra series.

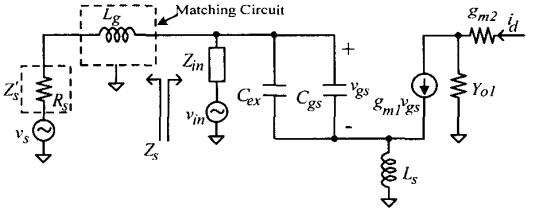

Fig. 2 Circuit model for nonlinear analysis

For linearity analysis purpose, the equivalent small signal circuit of LNA in Fig. 1 is depicted in Fig. 2. Now, M_2 can be considered and modeled by the series trans-conductance g_{m2}, assuming $r_{ds2} >> R_{out}$. In this case, the effects of the C_{gs2} and C_{gd1} have been neglected. The output admittance seen at the drain of M_1, Y_{o1}, is added in the model with the purpose to identify the output contribution. Using the Kickoff's law in the model of Fig. 6 the input signal can be written as

$$v_{in}(s) = v_{gs} a_1(s) + i_d a_2(s) \quad (12)$$

Where

$$a_1(s) = sC_t \left(Z_{in} + sL_s \right) + 1 \quad (13)$$

$$a_2(s) = sL_s \left(1 + \frac{Y_{o1}}{g_{m2}} \right) \quad (14)$$

When the effective mobility reduction is taken into account, the current between the source and drain terminals of the transistor M_1 is given as

$$I_{ds} = \frac{W v_{sat} C_{ox} \left(V_{gs} - V_t\right)^2 \mu_o}{\left(V_{gs} - V_t\right)\mu_1 + 2L v_{sat}} \quad (15)$$

where $\mu_1 \cong \mu_o + 2L v_{sat}\theta$ and $V_{gs} = V_{GS} + v_{gs}$

Here, V_{GS} is the DC bias voltage of the transistor, v_{gs} is the small signal between gate and source, and v_{sat} is the carrier velocity saturation. Using (12), the Volterra series expression of i_d is derived as

$$i_d = A_1(s)v_{in} + A_2(s_1,s_2)v_{in}^2 + A_3(s_1,s_2,s_3)v_{in}^3 \quad (16)$$

Here the coefficients of order higher than three are ignored. Usually, the adjacent channel frequencies ω_1 and ω_2 providing the intermodulation products are very close to the fundamental frequency ωtherefore $s \approx s_1 \approx s_2$ can be assumed. The $|IM3|$ at $(2\omega_1 - \omega_2)$ is

$$|IM_3| = \frac{A^2}{2}\left|\frac{A_1^3(s)}{g_{m1}^3}\right|\left|a_1(s)\right|\left|3g_3 - 2g_2^2 B\right| \quad (17)$$

$$B = 2\Delta s L_s(\Delta s)a_2(\Delta_s)A_1(\Delta s) + 2sL_s(2s)a_2(2s)A_1(2s) \quad (18)$$

$$A_1(s) = \frac{g_{m1}}{a_1(s) + g_{m1}a_2(s)} \quad (19)$$

$$g_2 = \frac{4K\mu_0 L^2 v_{sat}^2}{\left[\left(V_{gs} - V_t\right)\mu_1 + 2L v_{sat}\right]^3},\ g_3 = \frac{4K\mu_0 L^2 v_{sat}^2}{\left[\left(V_{gs} - V_t\right)\mu_1 + 2L v_{sat}\right]^4} \quad (20)$$

$$\Delta s = s_1 - s_2$$

where g_2 and g_3 are the second and third degree coefficients of the transistor nonlinear Taylor expansion. The B coefficient is the second-order interaction of the products 2ω, ω_1-ω_2, and ω_2-ω_1. $A_1(s)$ is the transconductance of the circuit. Substituting (19) into (17), it shows the dependence of $|IM3|$ with inverse of the term

$$\left[sC_t R_{in} + sL_s g_{m1}\left(1 + \frac{Y_{o1}}{g_{m2}}\right)\right]^3 \quad (21)$$

As can be seen in (17), the linearity can be improved by using different ways. Revising (17), the $|IM3|$ can be lowered with the reduction of $a_1(s)$, g_3, or with the increase (21). As shown in (13), with inductive degeneration the $s^2C_tL_s$ term will cancel the "1" term, and as a result $a_1(s)$ is reduced. This indicates that the selected topology is more adequate to keep the $|IM3|$ small in comparison with resistive and capacitive degeneration topology, where such cancellation does not exist. The joint effect of g_3 and g_2 coefficients in $|IM3|$ is inversely dependent on the bias $(V_{gs}$-$V_t)$, indicating that the linearity can be improved by increasing gate source voltage. However, increasing the gate source voltage will increase the power dissipation. With large Y_{o1} and g_{m1} values and small g_{m2} value (21) is increased such that the linearity will be increased. For the same reason, any increase in C_t, preserving the matching condition in the input circuit, also improves the linearity.

C. Design Consideration

In this section, the overall consideration for LNA design to obtain power-constrained simultaneous noise and input matching as well as linearization is described. The qualitative description of the proposed design process would be as follows. First, choose the DC bias, V_{GS}, for example the bias point that provides minimum F_{min}. Second, choose the transistor size, W, based on the power constraint, P_D. Third, choose the additional capacitance, C_{ex}, as well as the degeneration inductance, L_s, to satisfy (7), (9), and $s^2C_tL_s$ = -1 conditions (as mentioned, to improve the linearity of circuit the condition $s^2C_tL_s$ = -1 need to be satisfied). With the given L_s the condition Im[Z_{in}^*] = Im [Z_{opt}] is automatically satisfied. At this point, the simultaneous noise and input matching is achieved. As the last step, if there exists any mismatch between Z_{in} and Z_s^*, as shown in Fig. 1 (b), an impedance matching circuit can be added.

This design optimization technique suggest that, by using an additional capacitor, Cex, the LNA can be designed to archive power-constrained simultaneous noise and input matching as well as satisfy the linearization condition. The limitations of the PCSNIM technique are high Rn and low effective cut-off frequency. High Rn can be a serious limitation for the practical high yield LNA design.

3. Gain Enhancement Technique and Proposed LNA

One of the simple ways to improve the power gain of LNA is using positive feedback. In this paper, the positive feedback is realized by C_f shown in Fig. 3-a. This phenomenon can be understood by another point of view as the form of oscillator. In Fig. 3-a, C_{gs1}, C_f, and M_2 constitutes an oscillator topology with inductive termination at the output [1]. The effect of the positive feedback will increase maximum available gain of the cascode amplifier at high frequencies. Note that no additional active device is used therefore no more DC power is dissipated and no noise is contributed. The limit to amount of feedback is governed by stability consideration. To ensure the stability condition, G_{to1} must always positive. This technique is first introduced in [7]; however, the reported results are simulation-based only. This paper tries to realize this idea in term of measured results. The simplified proposed LNA is shown in Fig. 3-b. The proposed LNA is implemented by combining the PCSNIM design technique described in previous section and the gain enhancement technique shown in Fig. 3-a. In the Fig. 3-b, the simple L_o-C_o network represents the output-matching network and L_o is implemented by off chip inductor.

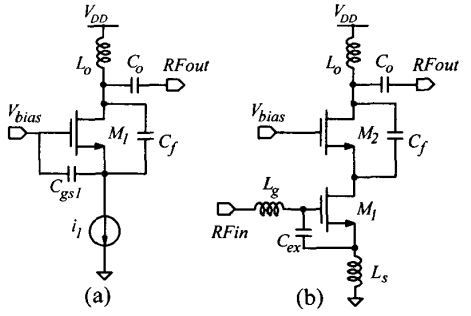

Fig. 3 Gain enhancement technique and the proposed LNA

4. Measurement Results

To demonstrate the potential of power-constrained simultaneous noise and input matching optimization technique and the gain enhancement technique, the current dissipation of the proposed LNA is fixed at 3 mA. Three LNA versions are fabricated based on 0.18 μm CMOS technology, the first circuit is simple cascode inductive degeneration topology, the second one simple cascode with C_{ex} and the third one is the proposed LNA shown in Fig. 3. Note that, all the circuits are designed at the same power dissipation. A Comparison of measured NF results are shown in Fig. 4. As can be shown in Fig. 4, by using the power-constrained simultaneous noise and input matching technique, the obtained *NF* is lower than that for the case of simple cascode inductive degeneration. The main reason of the improvement in *NF* can be understood as the discrepancy between real parts of input and noise matching conditions

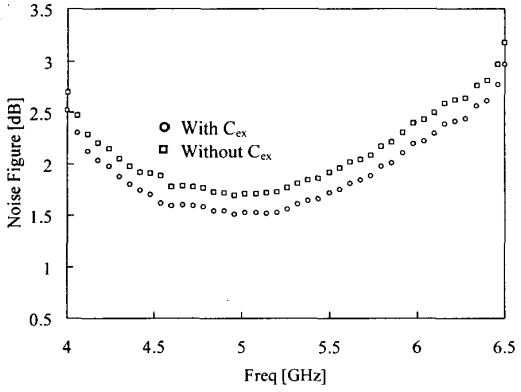

Fig. 4 Measured NF of LNAs

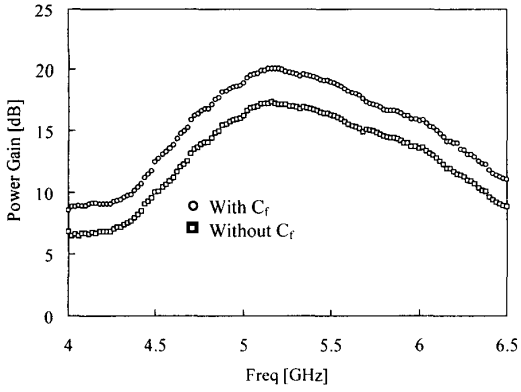

Fig. 5 Measured power gain of LNAs

Fig. 5 shows the measured results comparison of two LNAs simple cascode and proposed LNA shown in Fig. 3-b. As can be seen from Fig. 5, the power gain is improved by 3 dB compare to that of simple cascode topology. Fig. 6 shows the measured result of input third order intermodulation product of the proposed LNA. The proposed LNA has power gain of 20 dB, NF of 1.5 dB at 5.25 GHz and IIP3 of −5 dBm. The microphotograph of the three circuits is shown in Fig. 7.

5. Conclusion

In this paper, a very simple and insightful set of noise parameter expressions and the third order intermodulation product for the power-constrained simultaneous noise and input matching LNA design optimization technique is newly introduced. Based on those expressions, the design principle, advantage, and the limitation for the power-constrained simultaneous noise and input matched technique are explained. To demonstrate the potential of this design technique, the proposed LNA is designed and optimized for 5 GHz WLAN applications. The measured results show good agreement with theoretical analysis.

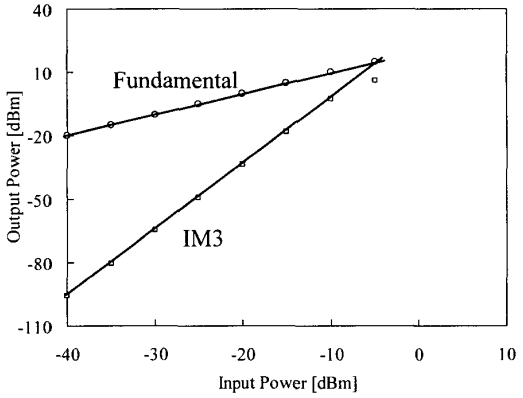

Fig. 6 IIP3 of the proposed folded cascode LNA

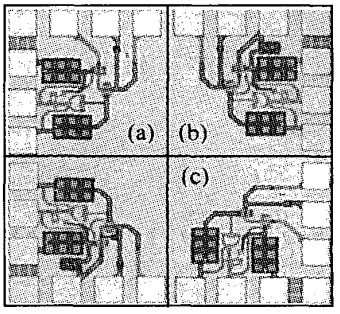

Fig. 7 Microphotograph of the three LNA: (a) simple cascode, (b) simple cascode includes C_{ex}, and (c) proposed LNA

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