# A Low Noise Image Rejection Down CMOS Mixer

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*Abstract* — **This paper represents a low noise image rejection mixer in heterodyne architecture for 2 GHz applications based on 0.18 μm CMOS technology. The designed mixer uses series inductor and capacitors as a notch filter to suppress the image signal and parasitic capacitance to improve the noise figure (NF) and conversion gain. An image rejection of 20-60 dB is obtained in a 200 MHz of bandwidth around 2 GHz with IF varying from 100 to 300 MHz The simulation results show single-side band (SSB) NF improved 4 dB, the voltage conversion gain of 14.4 dB, improved by more than 4 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 11.34 mW.**

## I. INTRODUCTION

The growing demands for low cost, low power, highly integrated circuit levels for wireless transceiver have motivated researcher to present number of monolithic solutions for CMOS technology.

Low cost, low power can be achieved by integrating all the required blocks as much as possible, thus minimizing the number of off-chip components.

There have been several researches for higher integration level for wireless transceivers such as direct-convesion [1] and quasi-IF architectures [2].

Direct conversion architecture eliminate the IF filtering problem by directly converting the RF signal to baseband. Band-pass RF filtering requirements are relaxed and IF filtering is unnecessary. The direct conversion architecture improves the integration level of RF receiver but it suffers from number of disadvantages, such as DC offset, second order distortion, self mixing and flicker noise in base band [1]. For quasi-IF architecture in [2], RF and IF filtering are relaxed, but there still remain the image rejection problem, DC offset and 1/f noise problems.

The heterodyne architecture, shown in Fig. 1, is widely used for the receivers in wireless system since the architecture has the high and stable performance [3,4]. In the heterodyne architecture, the image signal is 2IFs away from the RF signal. After the frequency translation from the down-conversion mixer, the image and signal both lie in the IF band and cannot be distinguished. The image signal appear to be noise or interference, it maybe much larger than the desired signal and therefore significantly degrade the system sensitivity. The way to deal with image problem is to suppress the image signal before down conversion. Currently, off-chip passive filers, such as surface acoustic wave (SAW) filters or ceramic filters, are used for image rejection. These filter cause the integration problem and complexity for the wireless systems, hence increasing the cost.

Image rejection mixer is a way to overcome the problem from those off-chip filters, increasing the integration level. In [5,6], image rejection mixer using phase cancellation is

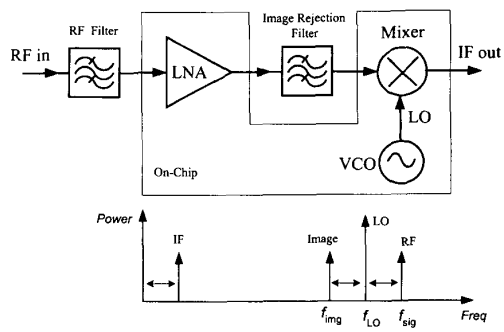


Fig 1. A heterodyne receiver

developed. Those poly phase filters are utilized but they are very sensitive to gain and phase mismatch. The image rejection level is from 25-35 dB, far from the 60-70 dB requirement of image rejection in different wireless standards. Moreover, poly phase filter is often used in cascade structure with the combination of several stages to obtain enough bandwidth, so it is very complex, consuming more power and sensitive for the design.

By utilizing a simple circuitry consisting of an inductor and capacitors in series as a notch filter, the novel image rejection mixer is introduced. It obtains the image rejection level of from 20–60 dB in a 200MHz bandwidth. With the availability of monolithic inductors, it is possible to implement such a simple circuit filter with no additional power consumption.

To meet the specifications of existing wireless systems, additional rejection is achieved by combining an on-chip image filter [3,7] with the integrated image rejection mixer.

Not only suppressing the image signal, the designed mixer also eliminates the parasitic capacitances at the common-source nodes of the mixer's switching stage. That leads to the further improvement in NF, conversion gain and linearity.

In this paper, a low noise image rejection mixer in heterodyne architecture for 2 GHz applications based on 0.18 μm CMOS technology is introduced. The designed mixer uses series inductor and capacitors as a notch filter to suppress the image signal and parasitic capacitance to improve the noise figure (NF) and conversion gain. An image rejection of 20-60 dB is obtained in a 200 MHz of bandwidth, from 1.9- 2.1 GHz with LO of 1.8 GHz, IF varying from 100 to 300 MHz The simulation results show single-side band (SSB) NF is improved about 4 dB, the voltage conversion gain of 14.4 dB, improved by more than 4 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 11.34 mW.

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## II. THE ANALYSIS

For the simplicity, single balanced mixer is used for illustration of the proposed circuit technique. In Fig. 2(a), LC tank circuit is inserted. The series resonant frequency of the LC tank is chosen at the image frequency. The transfer function of the LC circuit is:

$$Z_f(s) = \frac{1}{sC_1} + sL_1 = \frac{s^2 L_1 C_1 + 1}{sC_1} \tag{1}$$

$$f_{img} = \frac{1}{2\pi\sqrt{C_1 L_1}} \tag{2}$$

At the image frequency ($f_{img}$), $Z_f$ is zero, so LC tank steals the current away from showing at the output and reduces the gain at that frequency. Thus, image signal is suppressed.

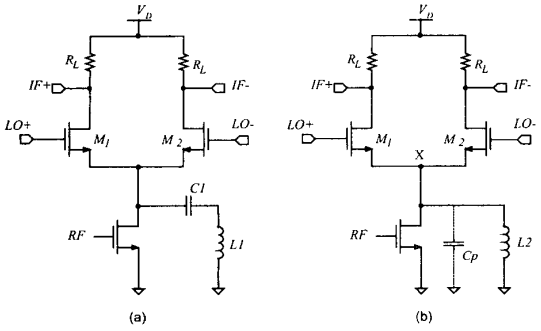


Fig. 2. Illustration of single balanced mixer for (a) image rejection, (b) parasitic capacitance suppression

However, the mixer topology shown in Fig. 2 has some drawbacks due to the parasitic capacitance at the drain node X of the switching transistors pair $M_1$-$M_2$. The parasitic capacitance ($C_p$) lowers the impedance at node X, leading to the reduction of the transconductance, RF signal loss and cause noise such that the conversion gain and NF of mixer are degraded. To restrict the bad effect of $C_p$ on NF and conversion gain, $C_p$ must be nullified. An inductor is inserted in parallel with $C_p$ to overcome the drawback caused by this parasitic capacitance, Fig. 2(b). The parallel resonant frequency of LC is determined equal to the RF signal. At RF signal frequency, node X has the highest impedance, in other words, lowest amount of signal leaks through $C_p$.

$$Z_f(s) = \frac{1}{sC_p} // sL_2 = \frac{sL_2}{s^2 L_2 C_p + 1} \tag{3}$$

$$f_{sgn} = \frac{1}{2\pi\sqrt{C_p L_2}} \tag{4}$$

From the above analysis, a solution circuit showed in Fig. 3 is introduced which can deal with the both two mentioned problems.

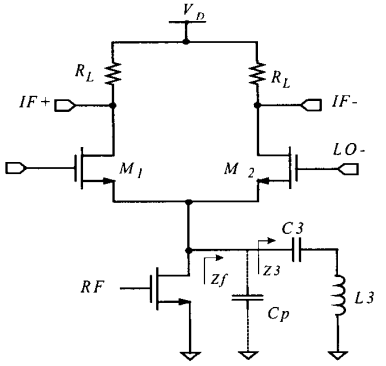


Fig. 3. Image rejection and parasitic capacitance single balanced mixer

The proposed circuit includes a series LC tank, $C_3$ and $L_3$, shown in Fig.3. Its function is similar to a notch filter. This filter will have the low impedance at the image frequency and high impedance at the frequency of signal. The input impedance of the filter can be derived and expressed as follows:

$$Z_f = Z_3 // \frac{1}{sC_p} \tag{5}$$

where $$Z_3 = \frac{1}{sC_3} + sL_3, \text{ and } s = j\omega \tag{6}$$

$$Z_f(s) = \frac{s^2 C_3 L_3 + 1}{s^3 C_3 L_3 C_p + sC_3 + sC_p} \tag{7}$$

$Z_f$ is a function of frequency, near the zero frequency, the filter has low impedance and near the pole high impedance is observed.

From (7), the frequency of the zero is

$$\omega_z = \frac{1}{\sqrt{C_3 L_3}} \tag{8}$$

The zero frequency is understood as the image frequency. The frequency of pole is

$$\omega_p = \sqrt{\frac{C_3 + C_p}{C_p C_3 L_3}} = \sqrt{1 + \frac{C_p}{C_3}} \times \frac{1}{\sqrt{C_3 L_3}} \tag{9}$$

$$\omega_p = \sqrt{1 + \frac{C_p}{C_3}} \times \omega_z \tag{10}$$

The pole frequency corresponds to signal frequency. From (8) and (9), the pole and zero gap is controlled by the ratio of $C_p$ over $C_3$. For correct and effective image rejection, the image frequency or zero must be chosen at the precise frequency. For given, RF signal frequency, we can determine the image frequency, and then using (8) and (10) together with simulation, the values of $L_3$ and $C_3$ are chosen. The higher the Q of an inductor is, the deeper the notch of image rejection filter we will get.

## II. THE PROPOSED MIXER DESIGN

The double-balanced Gilbert-type mixer topology shown in Fig.5 is preferred in CMOS mixer design since it suppresses the LO signal and the even order distortion products at the output.

Double balanced mixer consists of two single balanced mixers. When applying the circuit technique mentioned above for double balanced mixer, two LC tanks are put in series and symmetrically. The two LC tanks like in Fig. 2(a) can be simplified by using only one common inductor $L_i$ with two capacitors $C_i$ at the two ends, shown in Fig. 4. That is because, for double balanced mixer, the input signal is the differential, hence the middle point of $L_i$ is considered as the virtual ground. We have the equivalent circuit transform as follows:

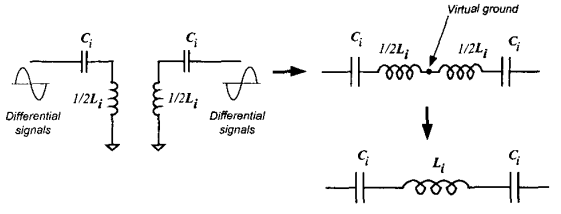


Fig 4. Tranformation of two differential LC tanks

The value of $L_i$ is twice the value of $L_3$. From the simulation, $L_i$ is determined a 8.6 nH on-chip inductor. From the RF signal and image frequencies, $C_i$ is calculated according to equations (9) and (10), it is chosen as 2.2 pF capacitors. This is the optimum value of $L_i$ and $C_i$, since $L_i$ must be small to ensure the high enough Q factor in the real circuit. If $L_i$ is too small, from equation (8), $C_i$ will be large leading to the narrower gap between the zero and pole as expressed in (10). But the zero and pole gap is given since they correspond to the RF and image signals.

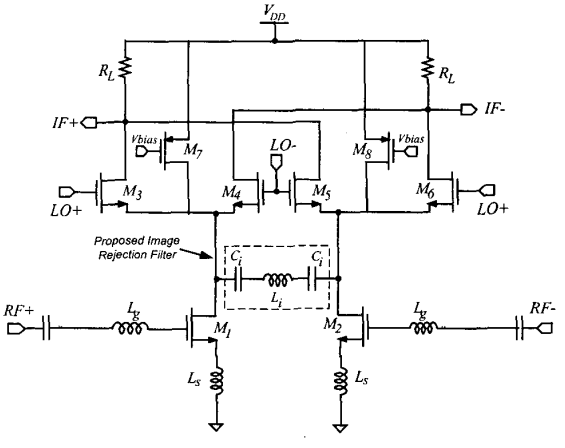


Fig. 5. The down-conversion mixer topology with proposed image rejection filter

In this design, current bleeding technique is utilized, PMOS transistors $M_7$ and $M_8$ create the bleeding currents under the gate bias voltage as shown in Fig. 3.

With the bleeding technique, the current through switching transistor is reduced by steering part of drive stage current from the switching transistors, such that the output load resistance is increased leading to a higher conversion gain. It also improves the switching efficiency that leads to lower NF [8].

The filter not only reject the image signal but also suppressed the parasitic capacitances at the common-source nodes of the switching transistor, as well as the effects of current through it. The conversion gain and NF of the mixer are improved [9,10].

Furthermore, with the image rejection filter, the impedance at twice the signal frequency is lower, in other words the current components at the high order harmonic frequencies, especially second harmonic, and intermodulation products running through common-source nodes of switching transistors are reduced partly, as a result, IIP2 is improved [11].

$L_g$ and $L_s$ are for input impedance matching at 50 Ohm, $L_s$ inductor is the bonding wire, it helps decrease the noise figure and increase the third order input intercept point (IIP3) [12].

## IV. SIMULATION RESULTS AND DISCUSSION

The proposed mixer in Fig. 5 is simulated in a TSMC 0.18 μm CMOS process by Cadence. The results are shown below.

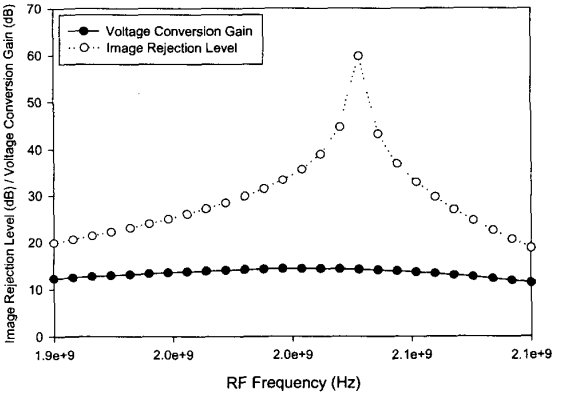


Fig 6. Image Rejection and Conversion gain versus RF frequency

With the presence of the proposed image rejection filter, the parasitic capacitances at the common-source nodes of the switching transistors are eliminated, therefore the RF signal loss through $C_p$ can be avoided, and higher gain can be achieved. Moreover, all the negative effects of $C_p$ on NF, higher intermodulation such as IIP2 are also eliminated [11].

The voltage conversion gain is improved by around 4 dB due to the elimination of $C_p$. In Fig. 6, the simulation shows the conversion gain is 14 dB at center frequency band when image rejection filter is used. Image rejection level is ranging from 20– 60 dB in the wide bandwith of 200 MHz. For narrow bandwidth centered around 2 GHz, the rejection level reaches about 50 dB and the peak reaches 60 dB of image rejection.

The peak of the image rejection characteristic corresponds to the zero frequency as analyzed in equation (1) and (2). Changing the value of $C_i$ will help us choosing the right image frequency.

The most effective and very impressive improvement in the designed mixer when utilizing image rejection filter is on the noise.

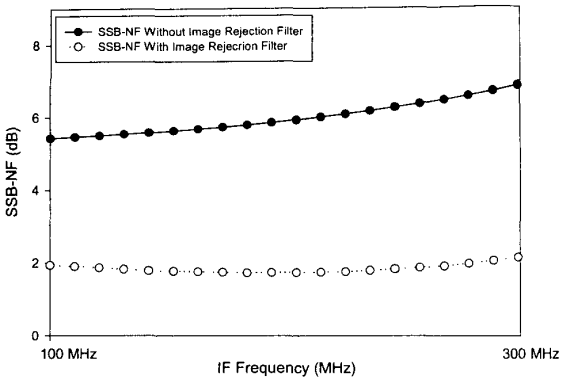


Fig. 7. SSB- NF with and without image rejection filter

For the down mixer in the heterodyne architecture, the main noise contribution come from the side-band noise translation, from RF band and image band to IF. Hence, when the image rejection filter is used, the image band noise is suppressed, the noise performance of the mixer is clearly improved. Figure 7 shows the SSB-NF performance of the mixer with and without using the image rejection. About 4 dB of improvement is obtained. The simulated NF is surprisingly small, probably due to the modeling inaccuracy, but the trend of improvement in NF showed in Fig. 7 is more important, it proved the effect of the filter on image rejection and as a result, NF is improved.

The performances of the proposed mixer are summarized in Table 1.

TABLE. 1
MIXER PERFORMANCE COMPARISION

| Parameters | Without Filter | With Filter |
|---|---|---|
| Input IP3 (dBm) | -9 | -7 |
| Voltage Conversion Gain (dB) | 10 | 14 |
| SSB NF (dB) | 6 | 2 |
| Image Rejection level (dB) | - | 20 - 60 |
| Supply Voltage (V) | 1.8 (TSMC 0.18μ) | |
| RF Frequency/ LO Frequency (GHz) | 1.9 – 2.1/ 1.8 | |
| Image Frequency (GHz) | 1.5 – 1.7 | |
| Power Consumption (mW) | 11.34 | |

## V. CONCLUSION

Image rejection is the main problem in heterodyne architecture. To avoid using off-chip filter to increase the integration level, reduce the cost and complexity of receiver, the image rejection mixer topology was designed. By adding a simple circuitry of inductor and capacitors in series, not only suppressing the image signal, the designed mixer also eliminating the parasitic capacitance at the common-source nodes of the mixer switching stage. The mixer topology, designed and manufactured in 0.18 μm CMOS process, shows an excellent performance, particularly in NF. The image rejection level is from 20–60 dB in a wide bandwidth of 200 MHz around 2 GHz with IF varying from 100 to 300 MHz. The simulation results show single-side band (SSB) NF of 2 dB, improved about 4 dB, the voltage conversion gain of 14.4 dB, improved by more than 4 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 11.34 mW.

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