0.18 μM CMOS SUB-HARMONIC MIXER FOR 2.4 GHZ IEEE802.15.4 TRANSCEIVER

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Abstract – This paper describes sub-harmonic mixer designed in 0.18 μm CMOS process and intended for use in low-power IEEE 802.15.4-compliant 2.4 GHz transceiver. Device addresses the following issues of the direct conversion architecture: flicker-noise, LO leakage and oscillator pulling.

I. Introduction

In the recent years, low-power integrated system design was established as one of the major trends in integrated circuit design industry and research. Requirements of low cost and close integration with digital circuitry dictate the usage of CMOS IC processes for RF and analog parts of transceiver. At the same time, while pursuing toward low-cost low-power receiver, direct conversion architecture is the natural selection.

At a first glance, it looks like low-frequency noise in a down-conversion mixer should be up-converted by LO and should not appear at the output frequency. In reality, not only it does appear at the output, but represents a severe impediment in usage of direct down-conversion architecture in wireless communication systems, especially in ones with narrow channel bandwidth. Two mechanisms responsible for non-complete up-conversion of the flicker noise were identified in literature [1]. One of them, which is the random modulation of the mixer switching instances by the low-frequency noise, is the dominant one in most practical situations. It was also pointed out that this dominant mechanism could be efficiently suppressed by using the passive mixer without DC-current.

Among other issues of Direct Conversion receiver design are self-mixing DC-offset due to LO signal coupling, and VCO pulling due to transmitter output signal and interferer signals coupling to the VCO circuitry [2]. The only feasible approach to deal with this issue is to operate VCO at the frequency not equal to the incoming RF carrier. This can be done by either the VCO frequency transformation [3] (division or multiplication, rational or fractional ones) or by using mixer in which the effective frequency mixing appears between input RF signal and harmonic of applied LO signal. In case of direct-conversion architecture it means that the mixer achieves desired down-conversion by accepting LO signal at sub-harmonic of RF carrier (sub-harmonic mixer) [4, 5].

Sub-harmonic passive mixer in Direct Conversion receiver can provide the advantages described above, as well as flicker noise-free operation.

II. Main part

The schematic of simulation setup is shown in Fig.1. The differential-driven key is used instead of single-MOSFET key in the conventional switching bridge. Accepting multiple-phase quadrature LO signal at half the frequency of RF carrier, the sub-harmonic mixer exhibit time-domain switching function similar to conventional mixer driven by LO signal with double frequency, thus implementing desired direct down-conversion.

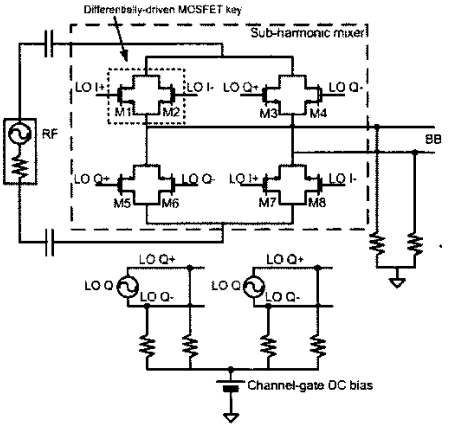

Fig. 1. Mixer schematic and simulation setup

Mixer operation principle under assumption of ideal switching is illustrated in Fig. 2 and Fig. 3.

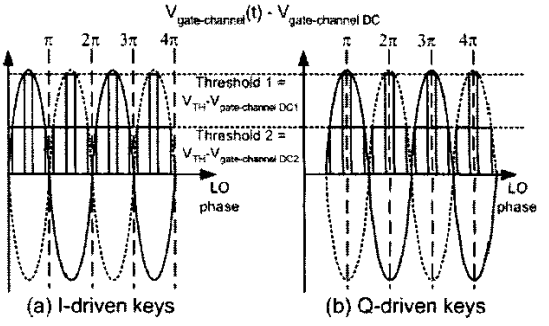

Fig. 2. Gate-channel LO differential waveforms minus their DC levels for MOSFET keys driven by I-LO (M1-M2 and M7-M8 keys) and Q-LO (M3-M4 and M5-M6 keys) signals

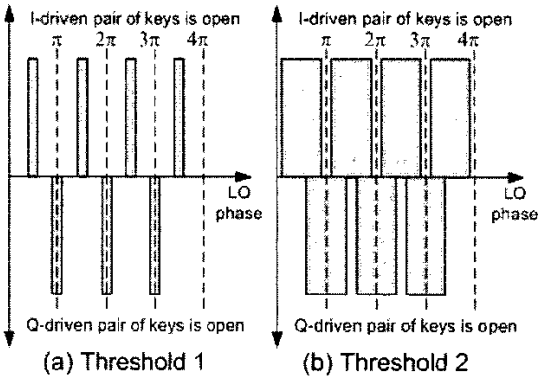

Fig. 3. Two cases of I- and Q-driven keys opening and closing timing resulting from different switching thresholds shown in Fig. 2

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Even though the period of switching function is half of the period of each differential signal for any gate-channel DC voltage bias (as long as the switch operates), opening and closing timing of I- and Q-driven pairs of keys depends on gate-channel bias and in turn affects the linearity and noise performance of the mixer, as it was found through simulation.

One of the design goals was the flicker-noise-free operation, therefore, mixer's Noise Figure for different gate-channel DC biases was simulated, Fig.4. Gate-channel DC bias is swept from 0.2 to 0.4 V. Under assumption of ideal switching, the DC bias of 0.32 V corresponds to switching when only one pair of keys (I-driven or Q-driven) is open at a time.

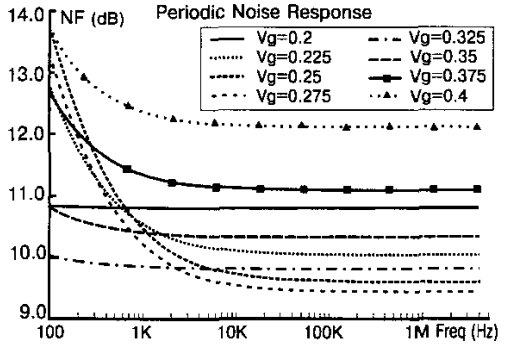

Fig. 4. Single side-band spot NF of the mixer versus output frequency for different gate-channel DC biases

As can be seen from Fig.4, flicker-noise corner frequency does not exceed few kilohertz, meaning that simulation shows flicker-noise-free operation.

The simulated mixer performance after the optimization of transistor sizes and voltage bias is summarized in Table 1.

As a way to provide quadrature LO signal required for the mixer operation, quadrature Voltage Controlled Oscillator (QVCO) was designed and submitted to fabrication at the same chip with mixer.

Table 1

Mixer simulated performance

Voltage gain	-6 dB20
IIP3	+ 5.5 dBm
SSB NF flat-band	10.6 dB
SSB NF @ 100 Hz	11 dB
LO differential amplitude	0.63 V
Current consumption	No current consumption in the mixer core
Intended transceiver supply voltage	1.25 V

III. Conclusion

Simulation results of passive sub-harmonic mixer are presented. Flicker-noise behavior that needs further theoretical explanation is observed. Sub-harmonic mixer with QVCO at sub-harmonic of incoming frequency constitute architecture that addresses the following issues of direct conversion receiver: flicker-noise, LO leakage and oscillator pulling. To the best of authors' knowledge, given mixer topology is first time utilized as a passive mixer. Simulation results of the mixer show flicker-noise-free operation with NF 10.6 dB, voltage gain –6 dB20 and IIP3 +5.5 dBm without DC power consumption. Mixer interconnected with QVCO is submitted for fabrication using 0.18 μm CMOS process and is intended for use in IEEE 802.15.4-compiant 2.4 GHz low-power transceiver.

IV. References

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0.18 мкм КМОП СУБГАРМОНИЧЕСКИЙ СМЕСИТЕЛЬ ДЛЯ ТРАНСИВЕРА IEEE802.15.4 НА 2,4 ГГц

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Аннотация – Описан субгармонический смеситель, спроектированный для 0.18 мкм КМОП процесса и предназначенный для маломощного приемопередатчика на частоту 2.4 ГГц, удовлетворяющие стандарту IEEE 802.15.4. Устройство ориентировано на разрешение следующих проблем архитектуры с прямым преобразованием: фликкер-шум, смещение выходного сигнала по постоянному току и затягивание частоты гетеродина.

I. Введение

Фликкер-шум смесителя является одной из проблем в архитектуре приемников прямого преобразования. В литературе [1] подчеркивается, что он может быть уменьшен использованием пассивных смесителей. Среди других проблем приемников прямого преобразования – постоянное напряжение на выходе смесителя вследствие наводок и самосмешения сигнала гетеродина, и затягивание частоты ГУН вследствие проникновения выходного сигнала передатчика на ГУН [2]. Как метод устранения указанных явлений предлагается схемное решение, описанное в докладе.

II. Основная часть

На рис. 2 показаны промоделированные частотные зависимости коэффициента шума предлагаемого смесителя (Рис. 1) при различном смещении на затворе. Продемонстрирована работа смесителя без фликкер-шума, но ход зависимостей нуждается в дополнительном теоретическом исследовании.

Для создания квадратурного сигнала гетеродина, необходимого для работы смесителя, последний был изготовлен на одном кристалле с квадратурным ГУН.

III. Заключение

Топология смесителя впервые используется в пассивном варианте. Моделирование показывает режим работы без фликкер-шума. Ожидаемые параметры смесителя: коэффициент шума 10.6 дБ, коэффициент усиления по напряжению –6 дБ и условная граница динамического диапазона по интермодуляционным искажениям третьего порядка +5.5 дБм. Схема была разработана для использования в маломощных приемопередатчиках диапазона 2.4 ГГц по стандарту IEEE 802.15.4.

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