A Novel Image Rejection CMOS Mixer Using T-Structure Filter

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***Abstract* - In this paper, a new image rejection mixer in heterodyne architecture for 2 GHz band applications based on 0.18 µm CMOS technology is presented. The designed mixer uses a T-structure filter to suppress the image signal, leading to the improvements in the noise figure (NF) and conversion gain. An image rejection of 25-85 dB is obtained in a 150 MHz of bandwidth from 1.95 to 2.1GHz with IF varying from 200 to 350MHz. The simulation results show single-side band (SSB) NF of 5 dB improved by 3.4 dB, the conversion gain of 10.5 dB, improved by more than 3 dB. The circuit operates at the supply voltage of 1.8 V, and dissipates 12 mW.**

I. INTRODUCTION

The heterodyne architecture, shown in Fig. 1, is widely used in wireless receivers since this architecture has the high and stable performance [1,2]. In the heterodyne architecture, the major problem is suppressing the interfering image frequency component, which is 2IF away from the RF signal. After the frequency translation from the down-conversion mixer, the unwanted image signal and wanted RF signal both lie in the IF band and cannot be distinguished. The image signal appears to be noise or interference, it may be much larger than the desired signal and therefore significantly degrades the system sensitivity. The way to deal with image problem is to suppress the image signal before down conversion. Currently, off-chip passive filers, such as surface acoustic wave (SAW) filters or ceramic filters, are used for image rejection. These filters cause the integration problems, increased weight and complexity for the wireless systems, hence increase the cost.

Image rejection mixer is a way to overcome the problem from those off-chip filters, increasing the integration level. In [3,4], image rejection mixer using phase cancellation is developed. Those polyphase filters are utilized but they are very sensitive to gain and phase mismatch. The image rejection level is from 25-35 dB, far from the 60-80 dB requirement of image rejection in different wireless standards. Moreover, poly phase filter is often used in cascade structure with the combination of several stages to obtain enough bandwidth, so it is very complex, consuming more power and sensitive for design.

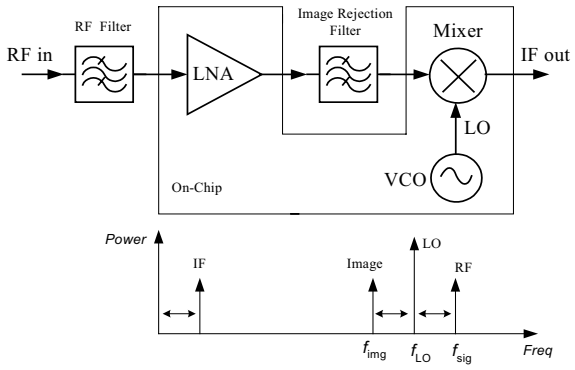

Fig. 1. A heterodyne receiver

A new image rejection mixer is introduced, by integrating a simple circuitry, a T-structure filter [5], the image rejection function is added to the mixer. With the availability of monolithic inductors, it is possible to implement such a simple circuit filter with no additional power consumption.

For further requirements on image rejection level of existing wireless systems, additional rejection can be achieved by combining an on-chip image filter [1,6] with this image rejection mixer.

In this paper, a simple image rejection (IR) mixer with controllable frequency of image rejection in heterodyne architecture for 2GHz applications based on 0.18 µm CMOS technology is introduced. The designed mixer uses a T-structure filter to suppress the image signal to improve the noise figure (NF) and conversion gain. An image rejection of 25-85 dB is obtained in a 150MHz of bandwidth from 1.95 to 2.1GHz, with local oscillator (LO) frequency of 1.75GHz. The simulation results show single-side band (SSB) NF is improved about 3.4 dB, the voltage conversion gain of 10.5 dB, improved by more than 3 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 12 mW.

II. THE T-STRUCTURE FILTER

T-structure is a popular circuitry and is often mentioned in the textbooks. In [5], T-structure consists of R, C and it is the 2nd order filter. By replacing R with L like in [7], we have a modified T-structure filter circuit with the 4th order transfer function as follows:

$$\frac{I_{out}}{I_{in}} = T(s) = \frac{s^4 + s^2\left(\frac{1}{C_1 + C_2}\right)\frac{1}{L_1} + \frac{1}{C_1 C_2 L_1 L_2}}{s^4 + s^2\left(\frac{1}{C_1 L_1} + \frac{1}{C_1 L_2} + \frac{1}{C_2 L_2}\right) + \frac{1}{C_1 C_2 L_1 L_2}} \quad (1)$$

The modified T-structure filter consists of L and C is shown in Fig. 2.

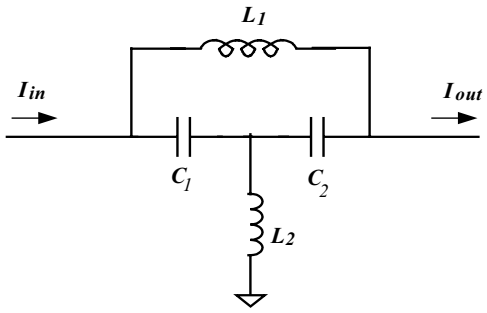

Fig. 2. T-structure filter

The above filter is added between the drive and switching stage of the mixer. At the drive stage of the mixer, the voltage is converted to current. The current is flowing through the switching stage to the load when the switch is ON. At the load, the current is turned to the voltage. So at the position the filter is added in the mixer, shown in Fig. 3, the current is of the interest.

From the transfer function of current derived for the filter, equation (1), we have the zero as follows:

$$f_{zero} = \frac{1}{\sqrt[4]{L_1 L_2 C_1 C_2}} \quad (2)$$

The zero frequency is designed at the image frequency. At this frequency, *T(s)* is zero, so the filter steals the current away from showing up at the output. As a result, the gain is reduced and image signal is suppressed. The pole frequency corresponds to signal frequency.

From [5], the Q of the filter is:

$$Q = \left[\frac{\sqrt{C_1 C_2 L_1 L_2}}{L_1}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\right]^{-1} \quad (3)$$

For correct and effective image rejection, the image frequency or zero must be chosen at the precise frequency. For given RF signal frequency, we can determine the image frequency by choosing the LO frequency. For given Q, from (2) and (3) we can roughly determine the values of capacitors and inductors by arbitrarily choosing the value for one of the two for each type, as long as they are suitable to practical values. Finally, by the simulation, the optimum values are found.

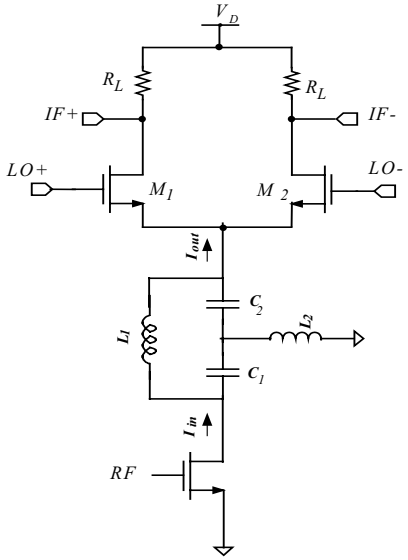

Fig. 3. Single balanced mixer integrated with T-structure filter for image rejection

III. THE PROPOSED MIXER DESIGN

The double-balanced Gilbert-type mixer topology shown in Fig.5 is preferred in CMOS mixer design since it suppresses the LO signal and the even order distortion products at the output.

Double balanced mixer consists of two single balanced mixers. When applying the circuit technique mentioned above for double balanced mixer, two T-structure filter circuits are put in the symmetric position. The two filters like in Fig. 2 can be simplified by using only one common inductor $2L_2$ instead of two L_2 at the two ends, shown in Fig. 4. That is because, for double balanced mixer, the input signal is the differential, hence the middle point of L_2 is considered as the virtual ground. We have the equivalent circuit transform as follows:

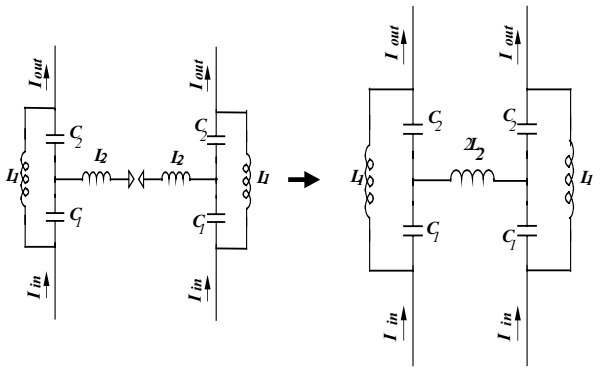

Fig. 4. Simplification of two differential T-structure filter circuits

Fig. 5 introduces a new image rejection mixer with the T-structure image rejection filter. The value of $2L_2$ is twice the value of L_2. From the simulation, $2L_2$ is determined a 8.9 nH on-chip inductor, L_1 is 4.9 nH. From the RF signal and image frequencies, equation (2), (3), C_1 is is chosen as a 6.3 pF capacitor, C_2 is 2.2 pF.

In this design, current bleeding technique is utilized, PMOS transistors M_7 and M_8 create the bleeding currents under the gate bias voltage as shown in Fig. 3. With the bleeding technique, the current through switching transistor is reduced by steering part of drive stage current from the switching transistors, such that the output load resistance is increased leading to a higher conversion gain. It also improves the switching efficiency that leads to lower NF [8].

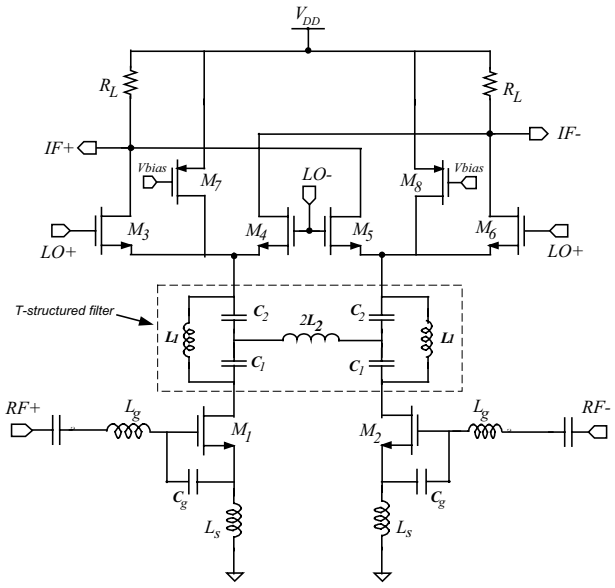

Fig. 5. The down-conversion mixer topology with proposed image rejection filter

L_1 not only acts as part of the T-structure filter, it also has the role of the inter-stage matching inductor. From [9], according to the Miller theory of capacitance, L_1 will introduce a negative resistance at the input port, which can improve the noise figure and gain.

C_g is added between the gate and source of the drive transistors making the input impedance matching easier [10]. Without C_g, the circuit is unstable with negative input impedance is observed during simulation, which is caused by L_1.

L_g and L_s are used for input impedance matching at 50 Ohm. L_s inductor is the bonding wire, it helps decrease the noise figure and increase the third order input intercept point (IIP3) [11]. L_g is an off-chip component, a large gate inductor L_g is normally used to tune out the gate-source of transistor M_1, M_2 for input matching purpose. So with the presence of C_g, the value of L_g is reduced.

IV. SIMALATION RESULTS AND DISCUSSION

The proposed mixer in Fig. 5 is simulated in a TSMC 0.18 μm CMOS process by Cadence. The results are shown below.

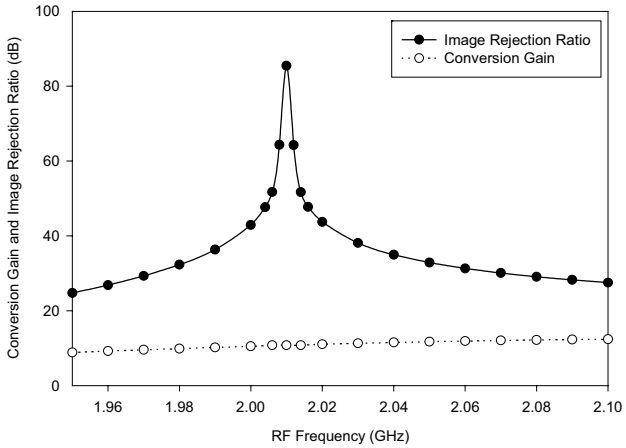

Fig. 6. Image Rejection Ratio and Conversion gain versus RF frequency

In Fig. 6, the simulation shows the conversion gain is 10.5 dB at center frequency band when image rejection filter is used. Image rejection level is ranging from 25 to 85 dB in the wide band-with of 150MHz. For narrow bandwidth centered around 2GHz, the rejection level reaches about 50 dB. At the peak, the attenuation in the image band is 74 dB, while the band pass signal gain is 11 dB, thus the peak reaches 85 dB of image rejection.

The peak of the image rejection characteristic corresponds to the zero frequency as analyzed in equation (2). The simulations show a very high image rejection ratio, however, the practical inductors have the restricted Q factor. The restricted Q factor due to parasitic resistance, substrate losses will partly degrades the image rejection ratio. However, the clear effect of the image rejection by applying the T-structure filter in Fig. 6 is more important.

The most effective and very impressive improvement in the designed mixer when utilizing image rejection filter is on the noise.

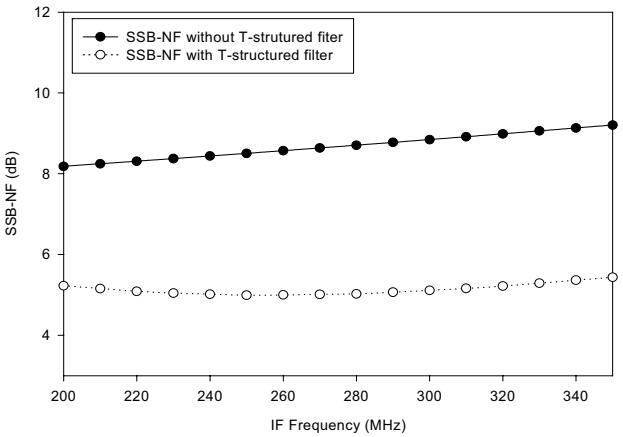

Fig. 7. SSB-NF with and without image rejection filter

For the down mixer in the heterodyne architecture, the main noise contribution come from the side-band noise translation, from RF band and image band to IF. Hence, when the image rejection filter is used, the image band noise is suppressed, the noise performance of the mixer is clearly improved. Figure 7 shows the SSB-NF performance of the mixer with and without using the image rejection. About 3.4 dB of improvement is obtained.

The simulated NF is quite small, probably due to the modeling inaccuracy, but the trend of improvement in NF showed in Fig. 7 is more important, it proved the effect of the filter on the image rejection and as a result, NF is improved.

The performances of the proposed mixer are summarized in Table 1.

TABLE I
MIXER PERFORMANCE COMPARISION

Parameters	Without Filter	With Filter
Input IP3 (dBm)	-6.2	-4.3
Voltage Conversion Gain (dB)	7.5	10.5
SSB NF (dB)	8.6	5.2
Image Rejection level (dB)	-	25 - 85
Image/Signal Frequency (GHz)	1.4 – 1.55 / 1.95 –2.1	
Supply Voltage (V)	1.8 (TSMC 0.18μ)	
Power Consumption (mW)	12	

V. CONCLUSION

Image rejection is the main problem in heterodyne architecture. To avoid using off-chip filter to increase the integration level, reduce the cost and complexity of receiver, the new image rejection mixer topology was designed. By adding a simple T-structure filter circuitry, the designed mixer can suppress the image signal. The mixer topology, designed in 0.18 μm CMOS process, shows an excellent performance, particularly in image rejection ratio and NF. The image rejection level is from 25–85 dB in a wide bandwidth of 150MHz around 2GHz with LO frequency of 1.75GHz. The proposed IR-mixer is suitable for wireless applications where high degree of integration is desirable.

The simulation results show single-side band (SSB) NF of 5.2 dB, improved about 3.4 dB, the voltage conversion gain of 10.5 dB, improved by more than 3 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 12 mW.

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