A Novel LC T-Structure Filter Integrated With CMOS Mixer For Image Rejection

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Abstract - **In this paper, a new image rejection mixer in heterodyne architecture for 2 GHz band applications based on 0.18 μm CMOS technology is presented. The designed mixer uses a LC T-structure filter to suppress the image signal, leading to the improvements in the noise figure (NF) and conversion gain. An image rejection ratio of 25-52 dB is obtained in a 150 MHz of bandwidth from 1.95 to 2.1GHz with IF varying from 200 to 350MHz. The simulation results show single-side band (SSB) NF of 3.2 dB improved by 2.4 dB, the conversion gain of 13.4 dB, improved by more than 1.4 dB. The circuit operates at the supply voltage of 1.8 V, and dissipates 12 mW.**

I. INTRODUCTION

The heterodyne architecture is widely used in wireless receivers since this architecture has the high and stable performance [1,2]. The heterodyne architecture front-end consists of band pass filter, low noise amplifier, image rejection filter and the mixer. The major problem in heterodyne receiver is the rejection of unwanted image signal. After the frequency translation from the down-conversion mixer, the unwanted image signal and desired RF signal both lie in the IF band and cannot be distinguished. The image signal appears to be noise or interference, it may be much larger than the desired signal and therefore significantly degrades the system sensitivity. Therefore, suppressing the interfering image frequency component, which is 2IF away from the RF signal is big challenge in heterodyne receivers. The way to deal with image problem is to suppress the image signal before down conversion. Currently, off-chip passive filers, such as surface acoustic wave (SAW) filters or ceramic filters, are used for image rejection. These filters cause the integration problem, increased weight and complexity for the wireless systems, hence increase the cost.

Some other image rejection filter, which are integrated on chip were proposed but they are complicated to design and consume additional power as in [3].

Image rejection mixer is a way to overcome the problem from those off-chip filters, increasing the integration level. In [4,5], image rejection mixer using phase cancellation is developed. Those poly-phase filters are utilized but they are very sensitive to gain and phase mismatch. The image rejection level is from 25-35 dB, far from the 60-80 dB requirement of image rejection in different wireless standards. Moreover, poly phase filter is often used in cascade structure with the combination of several stages to obtain enough bandwidth, so it is very complex, consuming more power and sensitive for design.

A new image rejection mixer is introduced, by integrating a simple circuitry, a LC T-structure filter [6], the image rejection function is added to the mixer. With the availability of monolithic inductors, it is possible to implement such a simple circuit filter with no additional power consumption.

For further requirements on image rejection level of existing wireless systems, additional rejection can be achieved by combining an on-chip image filter [1,7] with this image rejection mixer.

In this paper, a simple image rejection (IR) mixer with controllable frequency of image rejection in heterodyne architecture for 2GHz applications based on 0.18 μm CMOS technology is introduced. The designed mixer uses a T-structure filter to suppress the image signal to improve the noise figure (NF) and conversion gain. An image rejection of 25-52 dB is obtained in a 150MHz of bandwidth from 1.95 to 2.1GHz, with local oscillator (LO) frequency of 1.75GHz. The simulation results show single-side band (SSB) NF is improved about 2.4 dB, the voltage conversion gain of 13.4 dB, improved by more than 1.4 dB. The circuit operates at the supply voltage of 1.8 V, and dissipates 12 mW.

II. THE T-STRUCTURE FILTER

T-structure is a popular circuitry and is often mentioned in the textbooks. In [6], T-structure consists of R, C like Fig. 2(a) and it is the 2nd order filter. By replacing R with L like, we

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have a modified T-structure filter circuit with the 4th order transfer function as follows:

$$\frac{I_{out}}{I_{in}} = T(s) = \frac{s^4 + s^2(\frac{1}{L_1 + L_2})\frac{1}{C_2} + \frac{1}{C_1 C_2 L_1 L_2}}{s^4 + s^2(\frac{1}{C_2 L_1} + \frac{1}{C_2 L_2} + \frac{1}{C_1 L_2}) + \frac{1}{C_1 C_2 L_1 L_2}} \quad (1)$$

The above transfer function is deduced from [6] and [8]. In [8], we have the T-structure filter incorporated with the LNA with the positions of R and L are different from that in Fig. 2(b). The inductors in [8] cause negative impedance, makes the circuit unstable and difficult for input matching. As a result, C_c is added at the cost of lower gain.

The modified T-structure filter consists of L and C is shown in Fig. 2(b). With this topology, the effect of negative input impedance is cancelled, no C_c is needed, moreover the two series inductors L_1 and L_2 will act as the inter-stage matching inductor leading to the improvement in conversion gain[9].

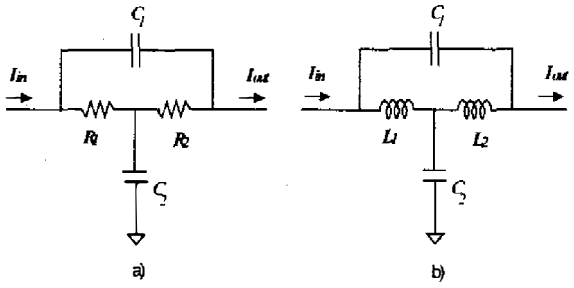

Fig 2. T-structure filter consists of a) RC, b) LC

The filter is added between the drive and switching stage of the mixer. At the drive stage of the mixer, the voltage is converted to current. The current is flowing through the switching stage to the load when the switch is ON. At the load, the current is turned to the voltage. So at the position the filter is added in the mixer, shown in Fig. 2, the current is of the interest. Therefore, the transfer function $T(s)$ is presented as the ration of input and output current of the filter.

From the transfer function of current derived for the filter, equation (1), we have the zero as follows:

$$f_{zero} = \frac{1}{\sqrt[4]{L_1 L_2 C_1 C_2}} \quad (2)$$

The zero frequency is designed at the image frequency. At this frequency, $T(s)$ is zero, so the filter steals the current away from showing up at the output. As a result, the gain is reduced and image signal is suppressed. The pole frequency corresponds to signal frequency.

From [6], the Q of the filter is:

$$Q = \left[\frac{\sqrt{C_1 C_2 L_1 L_2}}{C_2}\left(\frac{1}{L_1} + \frac{1}{L_2}\right)\right]^{-1} \quad (3)$$

For correct and effective image rejection, the image frequency or zero must be chosen at the precise frequency. For given RF signal frequency, we can determine the image frequency by choosing the LO frequency. For simplicity, let the value of two inductors L_1 and L_2 equal. For given Q, from (2) and (3) we can roughly determine the values of capacitors and inductors by arbitrarily choosing the value of the inductors, as long as it is suitable to practical values. Finally, by the simulation, the optimum values are found.

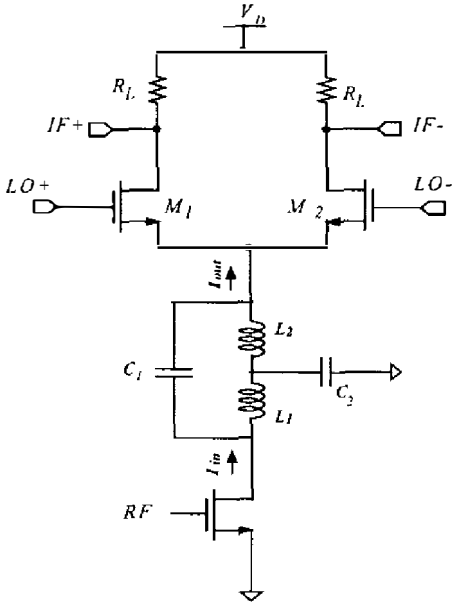

Fig 3. Single balanced mixer integrated with T-structure filter for image rejection

III. The Proposed Mixer Design

The double-balanced Gilbert-type mixer topology shown in Fig. 4 is preferred in CMOS mixer design since it suppresses the LO signal and the even order distortion products at the output.

Double balanced mixer consists of two single balanced mixers shown in Fig. 3. In double balanced mixer, the input signal is differential, hence the middle point of the two C_2 is considered as the virtual ground. So two T-structure filter

circuits are put in the symmetric position like in Fig. 4

Fig. 4 introduces a new image rejection mixer with the T-structure image rejection filter. For simplicity, L_1 and L_2 are supposed to have the same value. From (2), (3) and the simulation, they are determined a 4.6 nH on-chip inductor. From the RF signal and image frequencies and equation (2), (3), C_1 is is determined and chosen as a 6.4 pF capacitor, C_2 is 4 pF.

In this design, current bleeding technique is utilized, PMOS transistors M_7 and M_8 create the bleeding currents under the gate bias voltage as shown in Fig. 3. With the bleeding technique, the current through switching transistor is reduced by steering part of drive stage current from the switching transistors, such that the output load resistance is increased leading to a higher conversion gain. It also improves the switching efficiency that leads to lower NF [10].

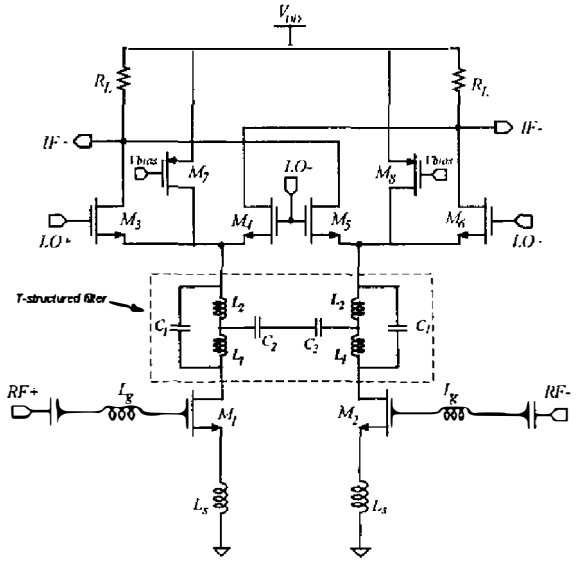

Fig. 4. The down-conversion mixer topology with proposed image rejection filter

L_1 and L_2 not only act as part of the T-structure filter, they also has the role of the inter-stage matching inductors that helps improve the conversion gain [9].

L_g and L_s are used for input impedance matching at 50 Ohm. L_s inductor is the bonding wire, it helps decrease the noise figure and increase the third order input intercept point (IIP3).

IV. Simulation Results And Discussion

The proposed mixer in Fig. 5 is simulated in a TSMC 0.18 μm CMOS process by Cadence. The results are shown below.

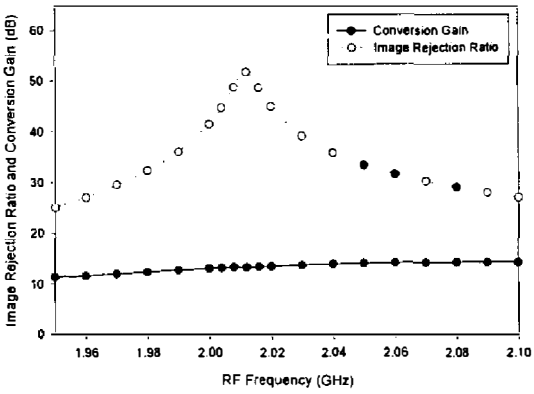

Fig. 5. Image rejection ratio and Conversion gain versus RF frequency

In Fig. 5, the simulation shows the conversion gain is 13.4 dB at center frequency band when image rejection filter is used. Image rejection level is ranging from 25 to 52 dB in the wide band-with of 150MHz. For narrow bandwidth centered around 2GHz, the rejection level reaches about 40 dB. At the peak, the attenuation in the image band is 38.6 dB, while the band pass signal gain is 13.4 dB, thus the peak reaches 52 dB of image rejection.

The peak of the image rejection characteristic corresponds to the zero frequency as analyzed in equation (2). The simulations show a very high image rejection ratio, however, the practical inductors have the restricted Q factor. The restricted Q factor due to parasitic resistance, substrate losses will partly degrades the image rejection ratio. However, the clear effect of the image rejection by applying the T-structure filter shown in Fig. 5 is more important.

The most effective and very impressive improvement in the designed mixer when utilizing image rejection filter is on the noise figure.

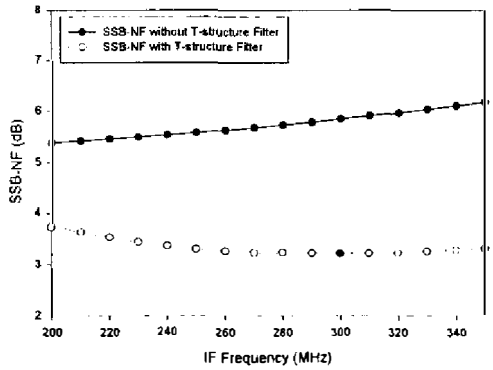

Fig. 6. SSB-NF with and without image rejection filter

For the down mixer in the heterodyne architecture, the main noise contribution come from the side-band noise translation, from RF band and image band to IF. Hence, when the image rejection filter is used, the image band noise is suppressed, the noise performance of the mixer is clearly improved. Figure 6 shows the SSB-NF performance of the mixer with and without using the image rejection. About 2.4 dB of NF improvement is obtained.

The simulated SSB-NF is quite small, probably due to the modeling inaccuracy, but the trend of improvement in NF showed in Fig. 6 is more important, it proved the effect of the filter on the image rejection and as a result, NF is improved.

The performances of the proposed mixer are summarized in Table I.

TABLE I

MIXER PERFORMANCE COMPARISON

Parameters	Without Filter	With Filter
Voltage Conversion Gain (dB)	12	13.4
SSB NF (dB)	5.6	3.2
Image Rejection level (dB)	-	25 - 52
Input IP3 (dBm)	-8.5	-10.2
Image/Signal Frequency (GHz)	1.4 – 1.55 / 1.95 –2.1	
Supply Voltage (V)	1.8 (TSMC 0.18μ)	
Power Consumption (mW)	12	

V. SUMMARY

Image rejection is the main problem and challenge in heterodyne architecture. To avoid using off-chip filter to increase the integration level, reduce the cost and complexity of receiver, the new image rejection mixer topology was designed. A simple LC T-structure filter circuitry is incorporated onto the double balanced mixer, as a result, the designed mixer can suppress the image signal. The mixer topology, designed in 0.18 μm CMOS process, shows an excellent performance, particularly in image rejection ratio and NF. The image rejection level is from 25–52 dB in a wide bandwidth of 150MHz around 2GHz with LO frequency of 1.75GHz. The proposed IR-mixer is suitable for wireless applications where high degree of integration is desirable.

The simulation results show single-side band (SSB) NF of 3.2 dB, improved about 2.4 dB, the voltage conversion gain of 13.4 dB, improved by more than 1.4 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 12 mW.

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