3.7 A Fully Integrated TV Tuner Front-End with 3.1dB NF, >+31dBm OIP3, >83dB HRR3/5 and >68dB HRR7

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In TV tuner systems, the RF front-end design has been a challenging issue since it must simultaneously satisfy over 65dB of harmonic rejection (HR), and have high linearity for high-power input and low noise over wide bandwidth (48-to-870MHz). In terms of harmonic rejection, even though the state-of-the-art work reports over 60dB rejections on the 3rd- and 5th- order harmonics with a single mixer [1], higher-than-5th-order harmonic rejections are still required for the low-band channels in TV tuners and thereby RF filters are indispensable at the RF front-end. However, due to the difficulties of integrating RF filters satisfying low noise and high linearity over wide bandwidth, the previous works inevitably had to use external inductors [2-4]. Although a recent work successfully integrates an RF filter satisfying all the stringent specifications by current-domain signal flow from the LNA output to the baseband stage [5], the transconductance stage at the filter input is not linear enough to drive the high-power input and thus the input signal needs to be attenuated at the RF front-end, which eventually degrades system SNR.

This paper presents a TV tuner front-end that shows exceptional linearity and harmonic-rejection performances over the whole frequency range while sustaining low noise. Figure 3.7.1 shows the block diagram of the TV tuner front-end. As shown in Fig. 3.7.1, the RF front-end consists of a shunt feedback LNA with post-nonlinearity correction scheme, a highly linear 6-b tunable RF filter and a 2-stage baseband HR mixer. In the front-end, a new-topology RF filter shows a cutting-edge linearity performance with low noise while the LNA also shows high linearity performance even in the high-gain mode. In addition, two-stage harmonic rejection in the baseband allows itself more robust performance to the gain mismatch compared to the previous two-stage harmonic rejection in [1].

Figure 3.7.2 shows the schematic of the two-stage resistive-feedback LNA. In Fig. 3.7.2, the LNA is composed of two gain stages (A_1 and A_2) with a resistive feedback (R_F) loop, where A_1 provides sufficiently high loop gain for low noise figure, and A_2 ensures near-ideal feedback operation by removing the loading effects. Basically, each gain stage adopts a common-source amplifier (M_{1N} or M_{3N}) cross-stacked with a source follower (M_{2N} or M_{4N}) considering its stable loop gain over PVT variations (the gain is determined by the transconductance (g_m) ratio of the M_{1N} to M_{2N}) and smaller amount of odd-order harmonic distortion by the post-linearization process [3]. In the first gain stage (A_1) as shown in Fig. 3.7.2, the combination of M_{1N} and M_{1P} configures an inverter-type amplifier, which inherently helps to cancel out the even-order harmonics, thus further improving the post-linearization process. Additionally, the cross-coupling current-bleeding transistors (M_{1P}) helps to boost the loop gain of the LNA by reducing the amount of current in M_{2N} (I_{2N} in Fig. 3.7.2), thus maximizing g_{m1N}/g_{m2N}, which also leads to the additional linearity improvement of the LNA. The LNA is designed to have 23dB of maximum gain, >+27dBm of OIP3 over the whole gain range with 1.4dB of noise figure at maximum gain while consuming 36mA from a 1.5V supply.

Figure 3.7.3 shows the schematic of the 4th-order active-RC low-pass filter. In Fig. 3.7.3, the filter biquad is composed of an RC ladder with a unity-gain buffer feedback. Contrary to the typical Sallen-Key (SK) filter, where the active circuits are placed in the feed-through path, the presented filter places it within the feedback path and thus not only eliminates the inherent stop-band limitation of the SK filter but also architecturally filters out the noise and nonlinear components of the active circuits. Moreover, since C_1 presents an open circuit at frequencies near DC, the filter is also free from the DC-offset problem in the unity-gain buffer. In order to sustain higher filter Q and better linearity, a sub-1-ohm-output-impedance source follower is used as the unity-gain buffer. As can be seen in Fig. 3.7.3, the source follower boosts the loop-gain and thus minimizes its output impedance by adopting common-gate active feedback (M_5, M_6), input cross-coupling through C_x, and source degeneration (R_s) to M_7, M_8. Since the low output impedance of the source follower allows sufficient filter Q at high frequencies even with small value of R in Fig. 3.7.3, the filter noise figure can be substantially reduced. Besides, the boosted loop gain reduces the harmonic distortion in the source follower, thus resulting in additional linearity improvement in the filter. The filter is designed to have <15dB of noise figure and >+25dBm of IIP3 for -9dBm of two-tone inputs with 6b bandwidth control over 40-to-660MHz of frequency range while the sub-1-ohm source follower consumes 8mA from a 1.5V supply and sustains its half-circuit output impedance below 1 ohm up to 900MHz.

The harmonic rejection mixer in Fig. 3.7.1 adopts the current-driven passive mixer topology for its low flicker noise and good linearity performance where the two-stage harmonic-rejection scheme is implemented in the baseband. In the harmonic rejection stage, 1:$\sqrt{2}$:1 gain control and 45° phase shift are implemented by the $\sqrt{2}$:1:$\sqrt{2}$ weighted resistors and divider-by-4 block with phase-trimming circuits. Compared to the transconductance ratio control at high frequency as in [1], the resistor ratio control in baseband is more accurate and less susceptible to the PVT variations, especially the threshold voltage variation. The mixer is designed to have 15dB of gain, 12dB of noise figure, >+33dBm of OIP3, and >60dB of 3rd- and 5th-order harmonic rejections in simulation while consuming 62mA for I/Q generation from a 1.5V supply.

Figure 3.7.4 shows the measured frequency response of the filter and P_{1dB} comparison up to the front-end gain. The bandwidth of the filter ranges from 40MHz to 520MHz sustaining steep roll-off characteristics. The measured output P_{1dB} in the LNA maximum-gain mode sustains the same value of +11dBm as the minimum-gain mode. This indicates that the linearity of the LNA is high enough not to degrade the linearity of the front-end. As seen in Fig. 3.7.4, in the low-gain mode, the front-end can endure up to -4dBm of input power without gain compression. As shown in Fig. 3.7.5, the IMD_3 of the front-end at 300MHz filter cut-off frequency is -68dBc with -12dBm two-tone inputs which corresponds to +37.6dBm of OIP3. Also in Fig. 3.7.4, the front-end OIP3 is >+31dBm over the whole gain and frequency range. The measured harmonic-rejection ratio of the RF front-end shows the 3rd- and 5th-order harmonic rejections of >83dB and >89dB respectively while the 7th and higher order is rejected by >68dB over 40-to-300MHz bandwidth. Figure 3.7.6 shows the summary of the front-end performances in comparison with state-of-the-art works. As can be seen in Fig. 3.7.6, the TV tuner front-end shows robust linearity performance regardless of its gain change. Even in case of 15dB of RF stage gain, the front-end can receive up to -4dBm of input signal. Figure 3.7.7 shows the chip micrograph where the tuner front-end occupies 2.7mm^2.

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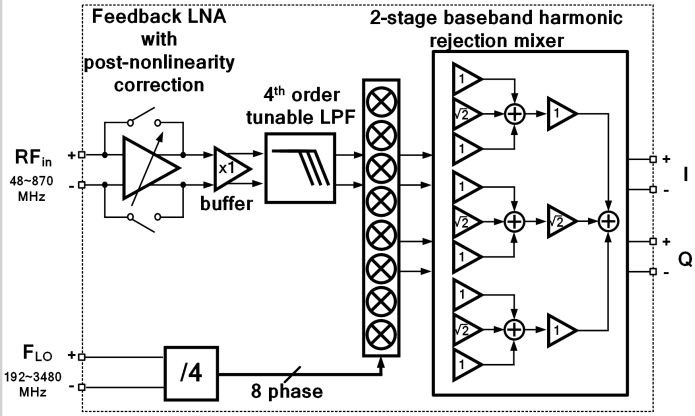

Figure 3.7.1: Block diagram of the TV tuner front-end.

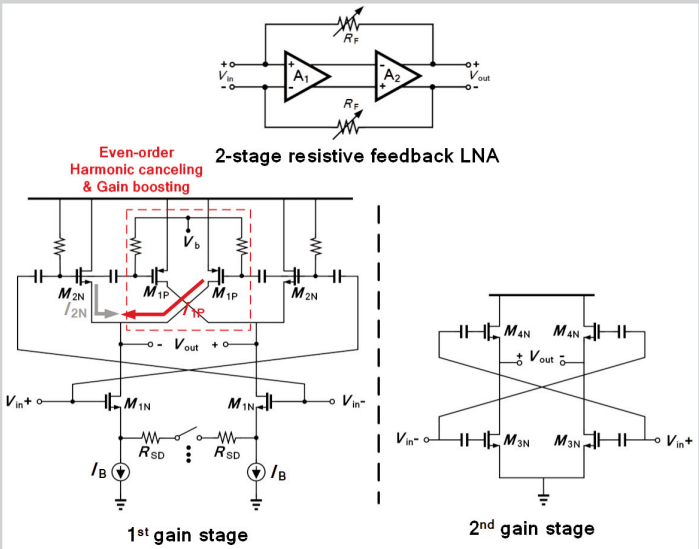

Figure 3.7.2: Schematic of the LNA and gain stages.

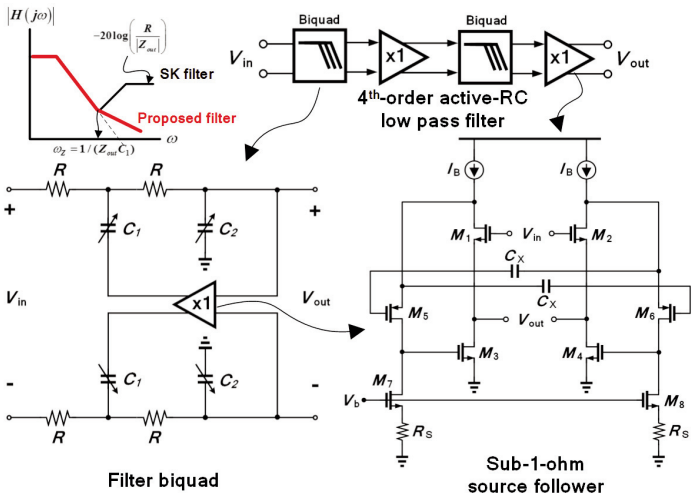

Figure 3.7.3: Schematic of the 4th-order low-pass filter.

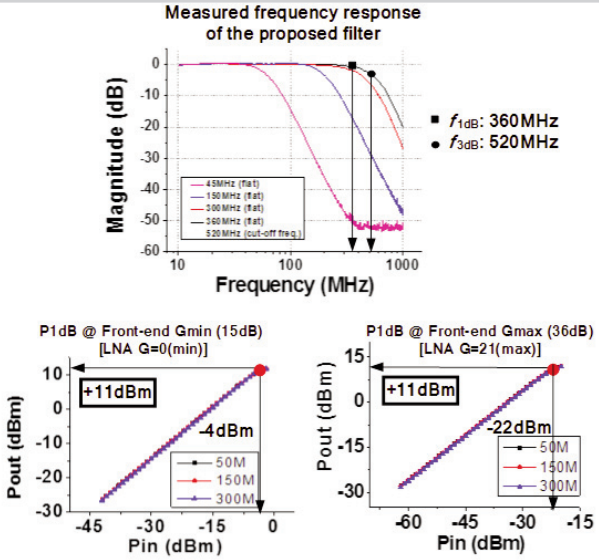

Figure 3.7.4: The measured filter shape and P_{1dB} of the front-end.

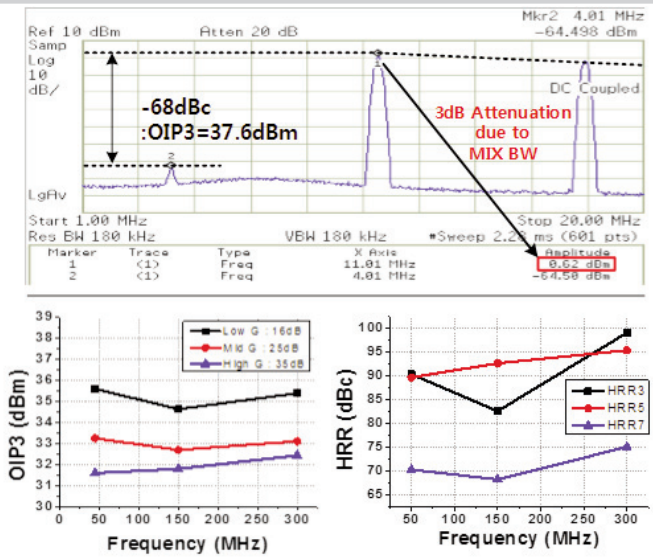

Figure 3.7.5: The measured OIP3 and HRR of the front-end.

Parameter	This work	[5] ISSCC'12	[2] JSSC'13	[3] JSSC'12	[4] T-MTT'10
Front-End Gain max/min [dB]	+36/+15	+36/-19	+42/-36	+42/-16	+40/-22
NF @ Max Gain [dB]	3.1	3	5	6	5.5
OIP3 min/max [dBm]	+31 / +34	+21 / +30	+32.5 / N/A	+29 / N/A	+30 / N/A
OIP2 min/max [dBm]	+59 / +69	+56 / +66	N/A / +62	N/A / +51	N/A
Ext. inductor in filter (#)	N	N	Y(3)	Y(1)	Y(1)
3rd HRR [dB]	>83	>65	>78	>70	>70
5th HRR [dB]	>89	>65	>84	>70	>70
7th HRR [dB]	>68	>65	N/A	>65	>60
Power [mW]	183 @1.5 V	[2]340 @1.8 V	[1]55.5 @1.5 V	[1]115 @1.8 V	[1]140 @1.8 V
Technology	0.13μm CMOS	80nm CMOS	65nm CMOS	0.18μm CMOS	0.18μm CMOS

[1]: the power consumption excluding RF filters.
[2]: the power consumption of all analog parts.

Figure 3.7.6: Performance table and comparison with state-of-the-art.

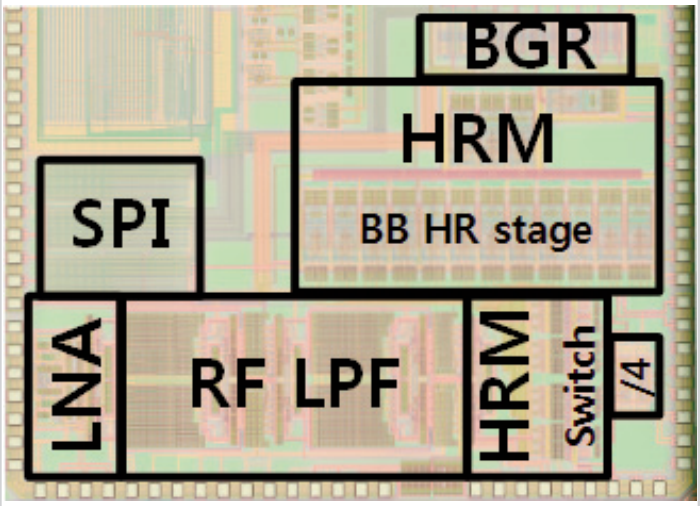

Figure 3.7.7: Chip micrograph in 0.13μm CMOS.

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