A CMOS Direct-Conversion I/Q Up-Mixer Block for Ultra-wideband System

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Abstract **– This paper presents a direct-conversion *I/Q* up-mixer block, which is implemented in 0.18 μm CMOS technology, for the ultra-wideband (UWB) system. To achieve wideband characteristics, a shunt-peaking load is used in the up-mixer. A new wideband amplifier is also proposed, which can suppress unwanted common-mode signals with high linearity. The simulation results show gain flatness of less than 0.5 dB for three channels, a maximum output power level of –4.3 dBm, and a sideband rejection ratio of more than 60 dBc. The current consumption of this design is 27 mA from a 1.8 V power supply.**

Keywords **– Ultra-wideband, CMOS, Transmitter, Mixer, Direct-conversion, Modulator, Wideband, Broadband**

1. Introduction

The Ultra-wideband (UWB) system has emerged as a major technology for high data rate service in wireless communication systems. The unlicensed UWB band allocates between 3.1 and 10.6 GHz, and the spectrum shape of modulated output power and maximum power level are limited (-41.3 dBm/MHz) by the Federal Communications Commission (FCC) [1]. Currently, two UWB system approaches for the Wireless Personal Area Network (WPAN) use carriers similar to conventional wireless systems: MB-OFDM (Multi-Band Orthogonal Frequency Division Multiplexing) and DS-CDMA (Direct-Sequence Code Division Multiple Access) [2]. The MB-OFDM approach has inherent robustness against narrowband interferers and multi-path environments when compared to the DS-CDMA approach. In addition, the MB-OFDM approach divides the UWB band (3.1 ~ 10.6 GHz) into several sub-bands with a bandwidth of 528 MHz, and then once again classifies them into three groups. In this way, the MB-OFDM approach can use its frequency band more flexibly. The lowest group (3168 ~ 4752 MHz) is decided as mandatory mode (Mode 1) in the MB-OFDM system, which can provide a more than 100 Mbps data rate [2]. Mode 1 has three channels, 3168 ~ 3696 MHz (Channel 1), 3696 ~ 4224 MHz (Channel 2), and 4224 ~ 4752 MHz (Channel 3) as shown in Fig. 1. Each channel is hopped within 9.5 nsec to increase data capability. This paper proposes an UWB direct-conversion *I/Q* up-mixer block, which can be adopted for the MB-OFDM transmitter (Mode 1). The proposed *I/Q* up-mixer block adopts a V-I converter to process a large input voltage signal from baseband circuits, like VGA or LPF, and a shunt-peaking load to achieve a flat gain for three channels, respectively.

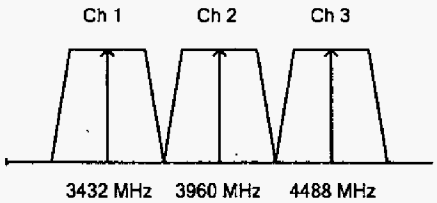

Figure 1. Frequency band for Mode 1 of MB-OFDM: Channel bandwidth = 528 MHz

2. Design of *I/Q* Up-Mixer Block

The transceiver for the MB-OFDM UWB system can be implemented by using heterodyne or direct conversion architecture. Comparing with the heterodyne architecture, the direct conversion architecture has several advantages including high integration, low power, low cost, and so on, despite its inherent drawbacks (*I/Q* mismatch, dc-offset, *1/f* noise, and so on). For low power implementation, the proposed *I/Q* up-mixer block adopts the direct-conversion architecture.

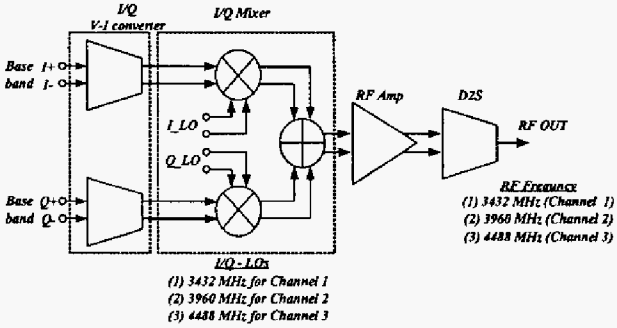

Figure 2. Simplified block diagram of the proposed *I/Q* up-mixer block

Fig. 2 shows a simplified block diagram of the proposed direct-conversion *I/Q* up-mixer block. It consists of an *I/Q*

V-I converter, an *I/Q* double-balanced mixer, a RF amplifier, and a differential-to-single (D2S) converter. In Fig. 2, the *I/Q* baseband voltage signal is first converted into a current signal by the *I/Q* V-I converter, and then modulated and up-converted into RF frequency by the *I/Q*-mixer. Three *I/Q*-LO tones (3432, 3969, and 4488 MHz) are provided from an external multi-LO tone generator for the *I/Q* up-mixer in Fig. 2. The RF amplifier follows the *I/Q*-mixer to provide more power gain and suppress unwanted common-mode signals generated from the output node of the mixer. The D2S converts the differential output signal of the RF amplifier into a single-ended signal, which is also matched to 50 Ω over 3 ~ 5 GHz.

The schematic of the V-I converter in *I*-path is shown in Fig. 3-(a), and the full *I/Q* mixer block in Fig. 3-(b). As shown in Fig. 3, to accommodate a large input voltage signal, the proposed *I/Q* mixer circuit adopts a V-I converter (in Fig. 3-(a)) as its transconductance stage. In Fig. 3-(a), by negative feedback

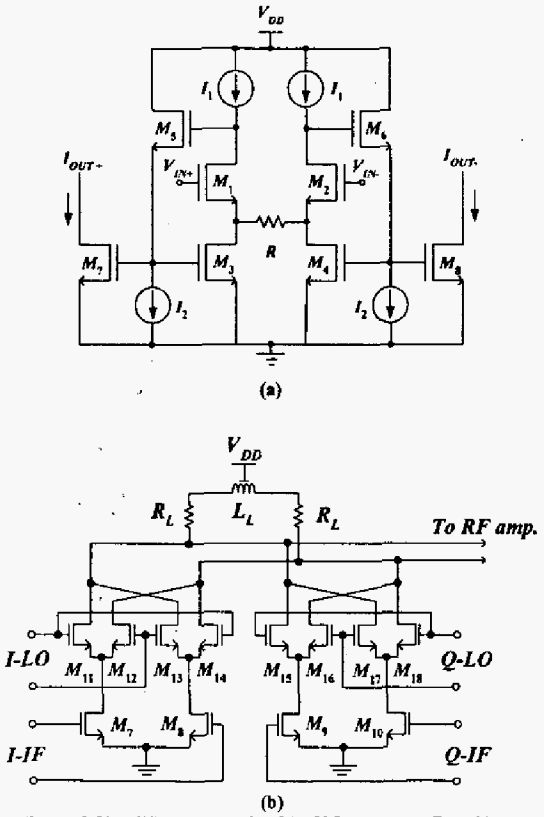

Figure. 3 Simplified schematic of (a) V-I converter (I-path) and (b) *I/Q* double balanced mixer

operation, constant current I_1 flows through the input transistor M_1 and M_2 such that the individual gate-source voltage V_{GS1} and V_{GS2} always remain constant [3]. As a result, input transistor M_1 and M_2 can operate in a saturation region up to a large input voltage swing, leading to high input linearity. The input voltage signal V_{in+} and V_{in-} are converted to the current signal (I) by M_7 and M_8, and the current signal is provided to the common-source node of switching transistors M_{11}-M_{14} in the up-mixer in *I*-path for frequency up-conversion. With the same operation, the converted current signal from the V-I converter in *Q*-path is also provided to the common-source node of M_{15}-M_{18} in the up-mixer in *Q*-path. The overall transconductance of the V-I converter in Fig. 3-(a) is approximately $1/R$ with low dc current consumption. The resistor R is implemented using a NMOS transistor in the triode region, which can be controlled by an external voltage source. In Fig. 3-(b), the *I/Q*-mixer circuit block adopts the widely used double-balanced configuration to suppress the strong LO power spectrum at output nodes, of which the frequency is the same as that of the modulated output RF signal. The modulated output currents from the *I/Q* mixer are summed and converted into a voltage signal at the shunt-peaking load (L_L and R_L) [4], which provides flat gain from 3 to 5 GHz. Because the –3 dB bandwidth of the load stage in the *I/Q* up-mixer by load resistor R_L and the large parasitic capacitances from the switching transistors M_{11}-M_{18} is unable to cover up to 5 GHz, an on-chip center-tap spiral inductor L_L is used to tune out the parasitic capacitances. In Fig. 3-(b), the value of R_L is 50 Ω and L_L 2 nH.

Fig. 4 shows the proposed RF amplifier topology, which combines the common-source (M_1 and M_2) and the common-drain (M_3 and M_4) amplifier. A general differential amplifier with a tail-current source has been among the most widely used circuits in RF and analog circuits, since it can suppress common-mode noise signals. In low power or high linear application, the common-source node of input transistors in the differential amplifier is usually directly connected to the ground to achieve high linearity. However, this configuration degrades its ability to reject common-mode signals.

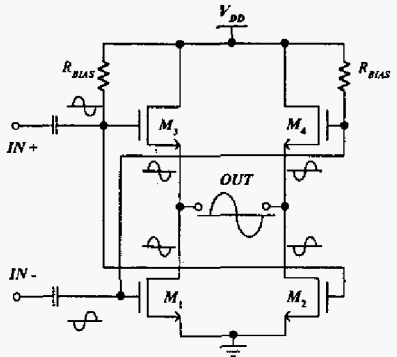

Figure 4. Simplified schematic of RF amplifier

The proposed RF amplifier, as shown in Fig. 4, can suppress unwanted common-mode signals with high linearity. In Fig.4, the common-source node of M_1 and M_2 is directly connected to the ground in order to achieve sufficient linearity. This topology is revised to suppress unwanted strong common-mode signals generated from the mixing operation of the *I/Q*-mixer block, while providing voltage gain for wanted differential signals. The operation of this amplifier can be described as follows: when an incoming

signal is in differential mode, MOS transistors M_1 and M_2 work as the common source amplifier; while M_3 and M_4 work as the source follower. Accordingly, all amplified differential signals are added in the in-phase at output node as shown in Fig. 4. For common-mode input signals, all amplified signals by M_1, M_2, M_3, and M_4 are added in out-of-phase at output node, so that the amplified signals are cancelled out considerably. This topology also shows sufficient the −3 dB bandwidth. In Fig. 4, the common-drain amplifier (M_3 and M_4) inherently shows very wideband characteristics [5]. The common-source amplifier (M_1 and M_2) has low value resistive loads, $1/g_{m3}$ and $1/g_{m4}$, respectively, where g_{m3} and g_{m4} is the transconductance of M_3 and M_4, so that the −3dB cut-off frequency ($\omega_{-3dB} = 1/RC_{para}$, C_{para}= total parasitic capacitances at output node) can extend up to 6 GHz from the simulation result. The differential to single (D2S) converter circuit shown in Fig. 5 is used to convert the differential signal from the output node of the RF amplifier in Fig. 2 to the single-ended signal for direct connection to the off-chip band pass filter (BPF). To completely sum the differential input signal at output node in the in-phase and at the same amplitude, several bonding wires are connected parallel to the source node of NMOS transistor M_1. This configuration also provides wideband characteristics, like the wideband RF amplifier in Fig. 4. The output of the D2S is matched to 50 Ω over 3 ~ 5 GHz with a small value of output impedance $1/g_{m2}$.

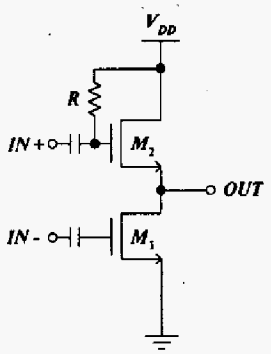

Figure 5. Schematic of D2S

3. SUMMARY

A CMOS direct-conversion *I/Q* up-mixer block for the MB-OFDM UWB system (Mode 1) is presented. The I/Q up-mixer block consists of a V-I converter, a double-balanced mixer, RF amplifier, and a differential-to-single converter circuit. All circuit blocks show excellent broadband characteristics over 3 ~ 5 GHz, respectively. The *I/Q* up-mixer adopts the shunt-peaking load to provide constant conversion gain for three channels with excellent gain flatness. The proposed wideband RF amplifier can suppress unwanted common-mode signals, while maintaining high linearity. The simulation results of this work are summarized in Table 1. The simulated results show gain flatness of less than 0.5 dB for three channels, a maximum output power level of −4.3 dBm, a sideband rejection ratio of more than 60 dBc, and an output return loss larger than −14 dB. Finally, the proposed I/Q up-mixer block shows good performances for the MB-OFDM UWB system (Mode 1). The current consumption of this work is 27 mA from a 1.8 V power supply. The layout is shown in Fig. 6.

Table 1 Summary of simulation results

	Baseband Frequency	RF Power Level (dBm)
Channel 1*	100 MHz	-13.45 @ 3.5 GHz
	300 MHz	-13.47@ 3.7 GHz
Channel 2*	100 MHz	-13.57 @ 4 GHz
	300 MHz	-13.58 @ 4.2 GHz
Channel 3*	100 MHz	-13.7 @ 4.5 GHz
	300 MHz	-13. 7 @ 4.7 GHz
S22	> -14 dB	
Max output power level	- 4.3 dBm	
Sideband Rejection	> 60 dBc	
DC consumption	27 mA from 1.8 V	

* Simulation condition : multi-LO power level = −3 dBm, baseband input power level = −15 dBm for differential 1k ohm loading

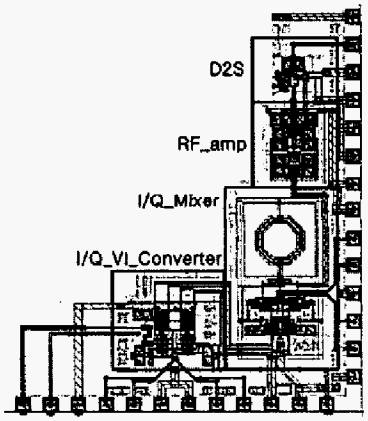

Figure 6. Layout (1.4 mm x 1.7 mm) including PADs

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