A Novel 1.5V DC Offset Cancellation CMOS Down Conversion Mixer

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***Abstract*—This paper presents a novel DC offset cancellation mixer for direct conversion receiver. The proposed mixer is designed in a TSMC 0.18 um CMOS technology with the supply voltage of 1.5V for 2.1 GHz applications. The extra feedback circuitry is used to cancel the DC offset, common mode feedback (CMFB) is used for active load. The design mixer has the conversion gain of 33 dB, NF of 3.9 dB and –13 dBm of IIP3. The DC offset is observed as 2 %. Moreover, the proposed mixer consumes only 5.4 mA of current.**

I. INTRODUCTION

In the past few years, mobile phone market has seen a significant growth. As the industry transits from 2G to 3 G, a number of applications and features are introduced. The size of cellular phone is smaller with higher speed data, multi-media applications and longer battery life. That is due to the emergence of direct conversion architecture.

Direct down conversion architecture makes possible the reduction of number of off-chip components, allowing higher integration level, minimizing power consumption. Beside the advantages, it suffers from number of challenges, like DC offset, second order distortion, self mixing and flicker noise in base band [1].

This work focuses on DC offset correction at the mixer block. In the direct conversion mixer, the down-converted spectrum is centered at DC, the DC offset lies in the middle of the spectrum so that it will degrade the desired signal. Furthermore, the DC offset may be larger than the signal, in the range of millivolts in CMOS devices, consequently, it will saturates the following stages [2].

The main causes of DC offset are component mismatch and self-mixing of the LO signal due to the insufficient on-chip isolation. The LO signal can couple through the substrate and bonding wire to antenna, low noise amplifier and the RF port of the mixer.

Coupling of the LO to the LNA and RF ports causes the static offset. However, when the LO couples to the antenna, radiates and then reflected off the moving objects back to the antenna, a dynamic offset is created [1].

DC offset can also be classified by its characteristics. When the two differential signals with DC offset have the same DC levels, we have “common mode DC offset”. In the case with different DC levels, we call “ differential mode DC offset”. General common mode feed back circuit can be used to adjust the former one, but cannot fix he latter one. Therefore, solving the latter one also means fixing the DC offset issue.

There are several ways to deal with DC offset issue in previously published papers. AC coupling is widely used to correct DC offset for its simplicity, but it will distort the original signal since high pass filter will block the signal around DC, and may degrade signal BER performance. Moreover, since the capacitors are coupling capacitor, metal-to-metal capacitor should be used, it takes a lot of space. Another method that uses DSP is introduced. This method traces the average value of signal [3], however it requires large chip size and complex.

According to [4], conventional offset cancellation technique can be divided into correlated double sampling, chopper stabilizer and auto-zeroing methods. The two first methods require complex design for clock, which may not suitable for RF application. In this paper, a novel circuit technique for offset canceling mixer based on auto-zeroing methods is introduced.

The offset canceling mixer utilizes two extra circuits, the common mode feedback (CMFB) to maintain the DC level at the mixer output and the negative feedback loop to cancel out the offset current.

The proposed mixer is design in standard TSMC 0.18 um CMOS technology. The simulations to verify the offset canceling effect of the proposed mixer show a high performance. The conversion gain is 33 dB, NF of 3.9 dB, IIP3 of –13 dBm. The mixer operates at 2.1 GHz under 1.5 V supply voltage and consumes only 5.4 mA of DC current. The DC offset is observed to remain less than 2 % of uncorrected offset.

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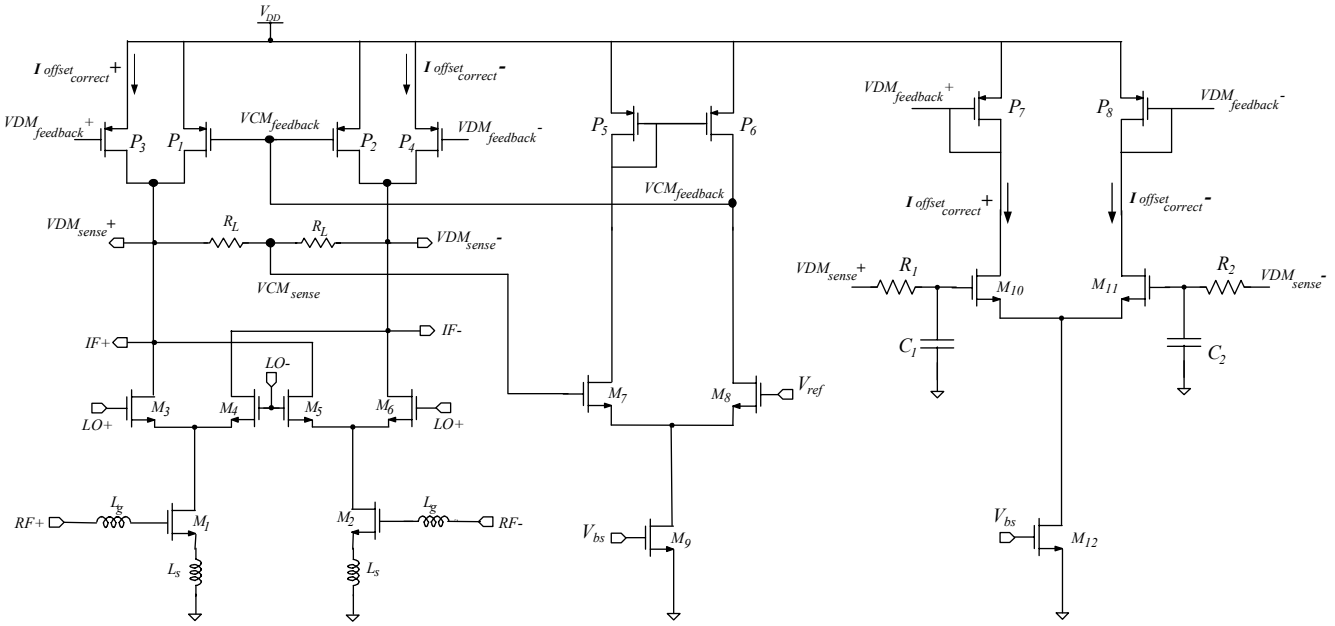

Figure 1. Complete Shemetic of the Proposed Offset Cancellation Mixer

II. PROPOSED MIXER DESIGN

A. Mixer Core

In a receiver system, the down-conversion mixer is the key building block since it dominates the system linearity, noise figure, and determines the performance requirements of its adjacent blocks. Among many proposed active mixers, the Gilbert-cell mixer has been widely used so far, and the double-balanced mixer topology has been preferred since it can suppress (LO) leakage signals at the output [5].

The down-conversion mixer is required to provide a low noise figure and high conversion gain. The simultaneous achievement on these requirements is a very challenging task in the mixer design, especially at low voltage supply.

Schematic of the core mixer is shown in Fig.1. RF signals are fed into the gate of the drive transistors M_1 and M_2. The transistor determined the gain and linearity of the mixer. M_3-M_6 are the switching transistors, careful sizing is done to balance the trade-off between the speed of switch transistors and flicker noise caused by these devices [6].

The output common-mode DC drain voltage is controlled with a feed back loop and the differential mode drain voltage is controlled with a DC offset correction circuitry, shown in Fig. 4.

The load consists of two poly-silicon resistors (R_L) connected differentially and two pair of PMOS transistors $P_{1,2}$. PMOS devices operate in saturation to have large channel resistance, R_d.

The load handles the base-band signal, so long channel PMOS can be used. Their large capacitances benefit in filtering unwanted RF signals and double frequency terms created during mixing.

The differential conversion gain (V_G) of the mixer core:

$$V_G = \frac{2}{\pi}.G_m.(R_d//R_L) \quad (1)$$

where G_m is the transconductance of drive transistors. To obtain high conversion gain, R_L must be large.

B. CMFB Circuit

A schematic of the CMFB circuit is shown in Fig. 2, it controls the common mode level of the output signals. The differential pair compares the reference voltage (V_{ref}) with the common mode drain voltage of the switching quad shown in Fig. 1.

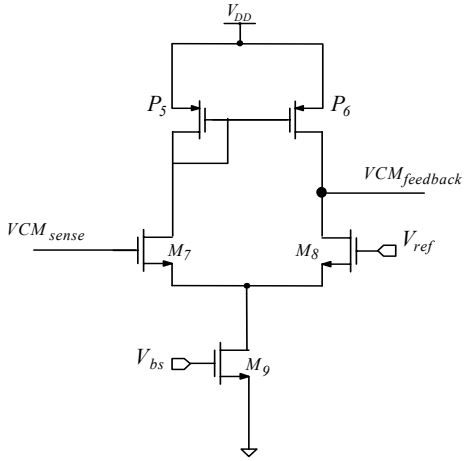

Figure 2. CMFB Circuit

The drain voltage of M_8 is fed to the gate of PMOS load transistors P_3 and P_4. The currents of these PMOS are changed with feedback voltage leading to the adjustable mixer output common mode DC voltage. With high enough loop gain, V_{ref} and common mode voltage are equal. V_{ref} is chosen to maximize output voltage swing.

III. DC OFFSET CANCELLATION

The offset cancellation principle can be modeled like in Fig. 3.

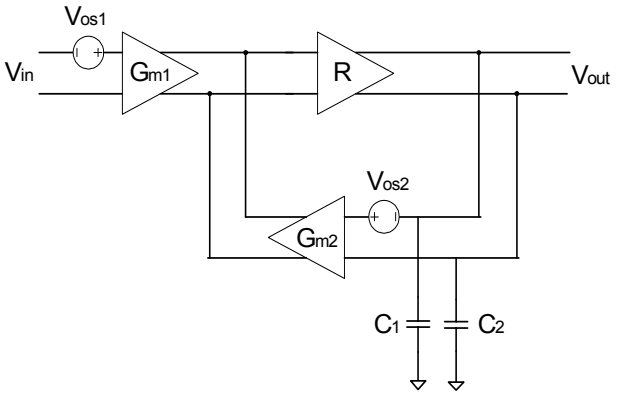

Figure 3. Principle of offset canceling technique

V_{os1} and V_{os2} are the offset voltage of G_{m1} and G_{m2} stages respectively. G_{m1} is the differential pair of the mixer transconductance, G_{m2} is differential pair of the negative feedback loop and R is the transimpedance amplifier.

Mixer output DC offset voltage at low frequency is detected and stored in C_1 and C_2. This voltage induced the offset correction current, which has opposite phase with offset current in the mixer core. G_{m2} injectes this offset correction current back to the mixer core to nullify DC offset current. From [7], we have the input referred offset voltage, V_{os} as follows:

$$V_{os} = \frac{V_{os1}}{G_{m2}R} + \frac{V_{os2}}{G_{m1}R} \qquad (2)$$

where $G_{m2}R >> 1$, if $G_{m1}R$ and $G_{m2}R$ are large, V_{os} will be small.

Fig. 4 shows a proposed offset cancellation circuit, which consists of a negative differential feedback loop with a low pass filter (LPF). This circuit detects the differences of the mixer output signals at DC level and removes the DC offset.

Narrow bandwidth applications of which the bandwidth ranges from few hundreds of KHz to a few of MHz, often have critical problem due to DC offset. Because of that, the LPF is designed with the cut-off frequency of a few tens of KHz. From the cut-off frequency, we can determine the values of C_1, C_2 of 60 pF and R_1, R_2 of 50 K Ohm.

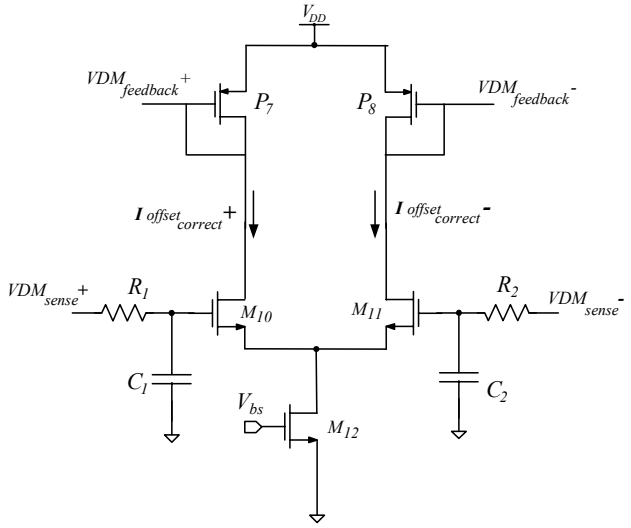

Figure 4. Offset cancellation circuit

In Fig. 4, differential DC offset voltages at the mixer output are sensed and passed through low pass filter (LPF), including resistor $R_{1,2}$ and capacitor $C_{1,2}$, while other higher frequency voltages are blocked. The differential pair M_{10} and M_{11} results differential current signals through P_7 and P_8. The offset correction current through P_7 and P_8 are mirrored with currents through P_3 and P_4. As a result, the offset correction currents are injected back to the mixer core. Therefore, the DC offset current in the mixer core is adjusted differentially leading to the cancellation of offset current in the mixer.

IV. RESULTS AND DISCUSSION

The proposed offset cancellation mixer is designed in TSMC 0.18 um technology. The mixer shows a high performance, especially, the simulation results verify clearly the effect of the DC offset cancellation.

Fig.5 shows the voltage conversion gain simulation result, the average voltage gain is 33 dB.

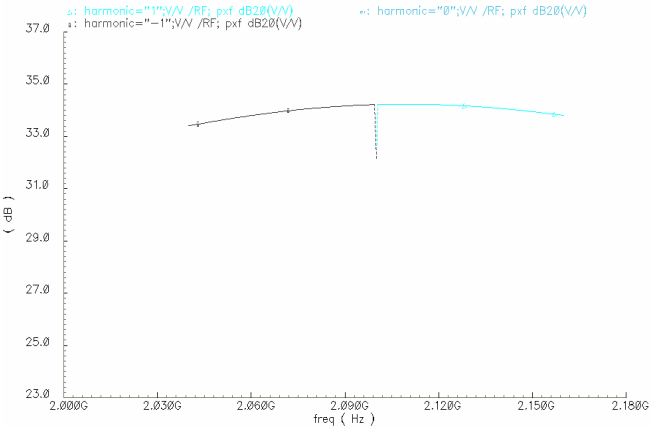

Figure 5. Offset Correction Mixer Conversion Gain

At low frequency, near DC, the conversion gain is attenuated, that means DC offset at low frequency is also suppressed. The input IP3 is simulated with two tones at 2.150 and 2.155 GHz and the results is – 13 dBm.

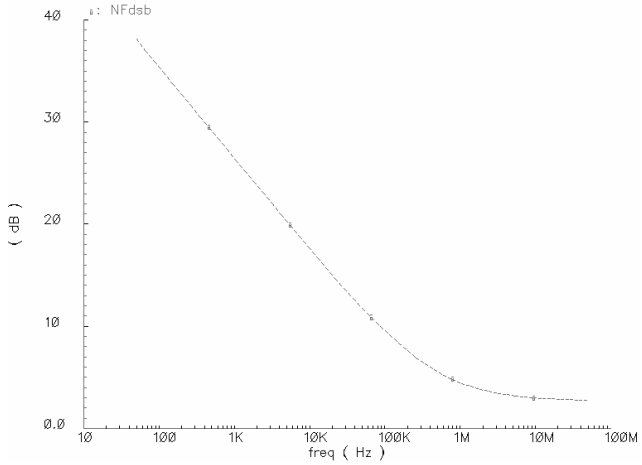

Figure 6. DSB NF of the Mixer

The mixer noise performance is shown in Fig. 6. DSB NF of the proposed mixer with and without using DC offset correction is 3.9 dB and 3.6 dB respectively. S11 and S22 are less than –12 dB.

The designed mixer has a good conversion gain performance but the trade off is the low linearity with IIP3 of –13 dBm.

In Fig. 7, the transient waveform of the proposed mixer at output is shown. The DC offset of the two differential output signals disappears as time passes.

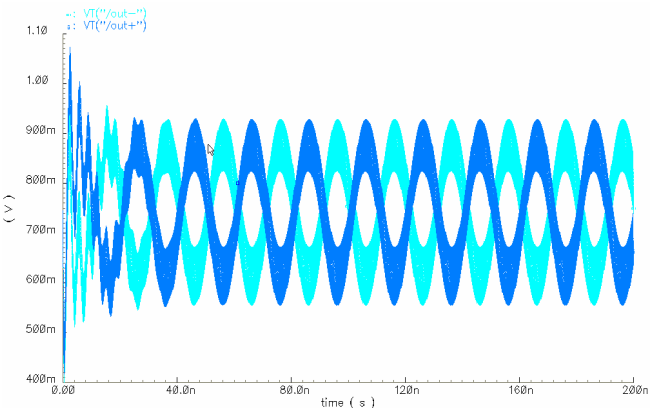

Figure 7. Transient of Output Wave Form

The causes of DC offset in the real circuits are from component mismatch and self-mixing of the LO signal. In order to verify the effect of DC offset canceling mixer, during the simulation, the load transistor is set 10% of mismatch. With the offset correction circuit, the DC offset voltage is 300 uV, while the uncorrected offset is 5 mV.

Summary of the simulation results are shown in Tab. 1. The cost of DC offset cancellation is 0.6 mA of DC current consumption for offset correction loop circuit.

TABLE I. DC OFFSET CANCELING MIXER PARMETERS

Parameters	Without DC Offset Correction	With DC Offset Correction
Input IP3 (dBm)	-12.3	-13
Voltage Conversion Gain (dB)	34	33.2
DSB NF (dB)	3.6	3.9
DC current consumption (mA)	4.9	5.4
LO / RF Frequency (GHz)	2.1 / 2.15	
Supply Voltage (V)	1.5 (TSMC 0.18µ)	

V. CONCLUSION

A novel DC offset canceling mixer is presented. The proposed mixer is design in standard TSMC 0.18 um CMOS technology. The offset canceling mixer utilizes two extra circuits, the common mode feedback (CMFB) to maintain the DC level at the mixer output and the negative feedback loop to cancel out the offset current.

The mixer operates at 2.1 GHz under 1.5 V supply voltage and consumes only 5.4 mA of DC current. The conversion gain is 33 dB, NF of 3.9 dB, IIP3 of –13 dBm. Offset canceling effect of the proposed mixer is observed to reduce to less than 2 % of uncorrected offset.

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