An All CMOS 84dB-Linear Low-Power Variable Gain Amplifier

Quoc-Hoang Duong, *Student member*, *IEEE*, Le-Quan, *Student member*, *IEEE* and Sang-Gug Lee, *Member*, *IEEE*

Information and Communications University
119-Mujro, Daejeon, Republic of Korea, 305-714.
Tel: +82-42-8666293. Fax: +82-42-8666227
Email: hoang@icu.ac.kr

Abstract

A new exponential approximation function is implemented into a variable gain amplifier (VGA). The newly proposed VGA topology provides low-power, small chip size, and wide control gain range. The VGA is fabricated in 0.18μm CMOS technology and measurements show a gain variation of more than 84dB in two cascaded stages, and 80dB-linear range with a linearity error of less than ±1dB. The P1dB varies from -42dBm to -22dBm. The power dissipation is less than 3.6mA from 1.8V supply. The chip excluding bondpads occupies 0.4mm^2.

Keywords: Variable gain amplifier (VGA), automatic gain control (AGC).

Introduction

VGAs play an important role in many applications; such as telecommunication systems, medical equipment, hearing aids, disk drives and others [1-5]. Many applications require highly-linear and wide-gain-range VGAs, and there are two options to realize them. One is the VGA controlled by digital signals, which are composed of a series of switchable gain stages. The other is the VGA controlled by analog signals, which typically adopt variable transconductance or resistance stages for the gain variation. The analog VGA is the preferred choice as it tends to require fewer gain-control signals.

In CMOS technology, the exponential function generators are generally realized by implementing the pseudo-exponential [1-4] or Taylor series approximation functions [5] into circuits. The pseudo-exponential and the Taylor series approximation functions are respectively given by

$$e^{2ax} \cong \frac{(1+ax)}{(1-ax)} \tag{1}$$

$$e^{2ax} \approx 1+\frac{2a}{1!}x+\frac{(2a)^2}{2!}x^2=\frac{1}{2}\left[1+(1+2ax)^2\right] \tag{2}$$

where a is a constant and x the independent variable, respectively. (1) and (2) are valid for $|2ax| << 1$. For a = 0.1, the plots of (1) and (2) in dB-scale are given in Fig. 1 by the dashed- and dotted-lines, respectively. As shown in Fig. 1, (1) and (2) provide less than 15 and 12dB-linear ranges with a linearity error of less than ±0.5dB, respectively. The pseudo-exponential function is of particular interest since it provides a higher dB-linear range compared to that of the Taylor series approximation. In Fig. 1, the increases of $|x|$ lead to critical deviations of (1) and (2) from the ideal line. Therefore, the gain ranges of VGAs that adopt (1) and (2) are limited by the same amounts [1-5], which are very small values. By circuit implementations of (1) and (2), wider gain ranges might be achieved, but the gain errors become significant. There is another type of analog VGA that utilizes the signal-summing technique as reported in [6]. The signal-summing VGA has the advantages of high frequency operation, low-noise, and low-distortion; but the gain control range is limited to less than 20 dB and the linearity error is large [6]. To the authors' knowledge, all CMOS VGAs, based on these techniques, achieve less than 20dB with a linearity error of less than ±0.5dB for one stage VGA, which is an extremely limited number [1-5].

In cellular wireless communication systems, the amplitudes of the receiver and transmitter signals vary by a large amount. Because of that, for example, in CDMA system, the transceiver requires at least 80dB of the dynamic gain range. In the typical receiver, about 20dB is assigned to the RF stage, and 60dB to the IF and/or baseband stages. Therefore, to cover the wide dynamic gain range, the existing CMOS-based VGAs that adopt (1) and (2) require at least 4 or 5 gain-varying stages. The multiple gain varying stages lead to a higher amount of power dissipation, which makes these VGAs un-suitable for the low-power applications. Also, the multiple-stage VGA results in a larger chip area, which leads to higher cost. Another universal solution to achieve such a very wide gain range is using bipolar transistors [6]; but the bipolar techniques are not compatible with standard CMOS-based circuits [6].

To solve the above problems, in this paper, a new exponential approximation method is implemented in the design of the VGA. The new method offers a very wide gain range compared to conventional ones such that a very low-power, small chip size, wide control gain range, and all CMOS VGA can be obtained.

A New Exponential Approximation Equation

The VGA proposed in this paper utilizes a new exponential approximation equation proposed by the authors, which is given by [7]

$$e^{2ax}=\frac{e^{ax}}{e^{-ax}}\cong\frac{\left[k+(1+ax)^2\right]}{\left[k+(1-ax)^2\right]} \tag{3}$$

where k is a constant. For k = 1, the numerator and the denominator of (3) are the second-order Taylor series approximation of the exponential function. For k less than unity, the dB-linear range of (3) can be extended drastically as shown in Fig. 1 by the dash-dot (k = 1), dash-dot-dot (k = 0.25), and solid (k = 0.15) lines. As can be seen in Fig. 1, for k = 0.15 (the solid line), the dB-linear range extends to more

than 60dB with a linearity error of less than ± 0.5dB, which is a serious improvement compared to the Taylor series approximation and pseudo-exponential functions. Moreover, the input range of x for the new approximation equation is much larger than that of the Taylor series approximation and pseudo-exponential functions as depicted in Fig. 1 by the solid line.

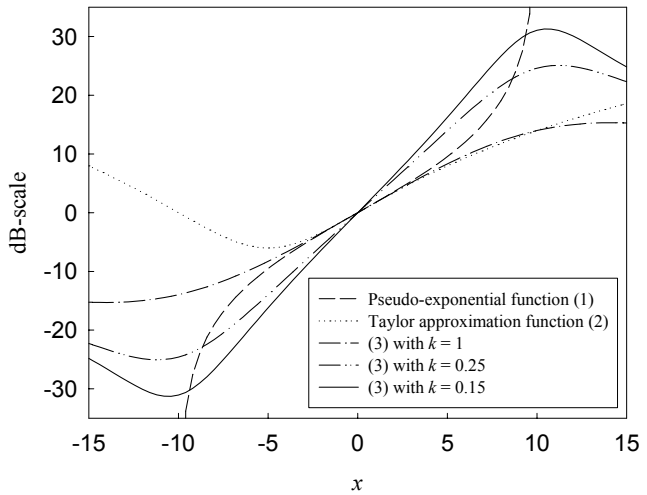

Fig. 1 Plots of various functions on dB-scale

Since long-channel CMOS transistors provide square-law characteristics in saturation region, and the numerator and the denominator of (3) are all second-order functions, the newly proposed exponential approximation function can easily be implemented in CMOS technology. In principle, a VGA that adopts (3) can satisfy 60dB of the required gain range in one stage. Consequently, the power dissipation and the chip area (or the cost) can be reduced drastically.

Circuit Implementation of the New exponential Approximation Equation

A. The control circuit block

The circuit for generating the numerator and the denominator of (3) is given in Fig. 2, where all transistors operate in saturation mode. In Fig. 2, the body terminals of P- and N-MOS transistors are tied to V_{DD} and V_{SS}, respectively, and the lengths of transistors M_1 and M_2 are chosen long enough that the second order effects can be neglected. In Fig. 2, to guarantee the saturation-mode operation of transistors M_1 and M_2, the control voltage V_C must stay within a range of $(V_{SS} + V_{THn}) \sim (V_{DD} - |V_{THp}|)$. The drain currents of transistors M_1 and M_2 in Fig. 2 are given as

$$I_{D1} = K_p\left(V_C - V_{DD} + |V_{THp}|\right)^2 \quad (4)$$

$$I_{D2} = K_n\left(V_C - V_{SS} - V_{THn}\right)^2 \quad (5)$$

where K_p and K_n are constants, and V_{THp} and V_{THn} the threshold voltages of the P- and N-MOS transistors, respectively. In Fig. 2, the currents I_{D1} and I_{D2} are added by a bias current I_0. The resulting currents I_{C1} and I_{C2}, after some mathematical manipulations, can be given by

$$I_{C1} = K_p\left(V_{DD} - |V_{THp}|\right)^2 \times \times\left\{\frac{I_0}{K_p\left(V_{DD} - |V_{THp}|\right)^2} + \left(1 - \frac{V_C}{\left(V_{DD} - |V_{THp}|\right)}\right)^2\right\} \quad (6)$$

$$I_{C2} = K_n\left(V_{SS} + V_{THn}\right)^2 \times \times\left\{\frac{I_0}{K_n\left(V_{SS} + V_{THn}\right)^2} + \left(1 - \frac{V_C}{\left(V_{SS} + V_{THn}\right)}\right)^2\right\} \quad (7)$$

Assuming $K_p = K_n = K$, $V_{DD} = -V_{SS}$, and $|V_{THp}| = V_{THn} = V_{TH}$, from (6) and (7), the ratio I_{C2}/I_{C1}, the relation that is utilized in the amplifying block which will be described later, can be given by

$$\frac{I_{C2}}{I_{C1}} = \frac{\frac{I_0}{K\left(V_{DD} - |V_{TH}|\right)^2} + \left(1 + \frac{V_C}{\left(V_{DD} - |V_{TH}|\right)}\right)^2}{\frac{I_0}{K\left(V_{DD} - |V_{TH}|\right)^2} + \left(1 - \frac{V_C}{\left(V_{DD} - |V_{TH}|\right)}\right)^2} = \frac{\left[k + (1 + ax)^2\right]}{\left[k + (1 - ax)^2\right]} \quad (8)$$

where $k = I_0 \big/ K\left(V_{DD} - |V_{TH}|\right)^2$, $a = 1/\left(V_{DD} - |V_{TH}|\right)$, and $x = V_C$.

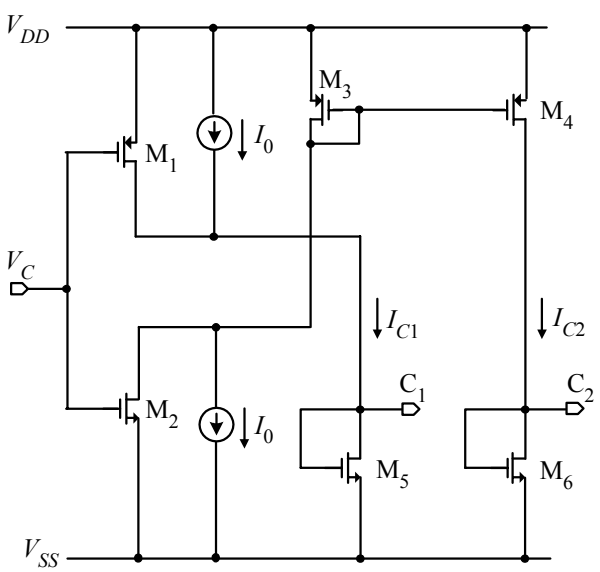

Fig. 2 The proposed circuit schematic of control block.

As can be seen in (8), the current ratio I_{C2}/I_{C1}, which is a function of the control voltage V_C, is equivalent to (3). In (8), adjusting the bias current I_0 can vary the value of the constant k, resulting in different dB-linear ranges.

From (4) and (5), by assuming $V_{DD} = -V_{SS}$, the exponential approximation equation as a function of the control voltage V_c is obtained and shown in (8). Considering the case where $V_{DD} = -V_{SS} = 0.9$V; if we shift all supply voltage nodes by 0.9V, $V_{DD} = 1.8$V, $V_{SS} = 0$V and the input

voltage V_C is from V_{THn} to (1.8 - $|V_{THp}|$). In this case, the exponential relation shown in (8) is still maintained.

B. Variable Gain Amplifier Circuit

Fig. 3 shows the circuit schematic of the amplifying block that is adopted for the proposed VGA, including the common-mode feedback circuit. The variable gain circuit block is composed of an input source-coupled pair (M_9 and M_{12}) and diode-connected loads (M_{10} and M_{11}). The sum of currents through input pair and loads is equal to that of the upper PMOS current sources (M_7 and M_8). The two currents I_{C1} and I_{C2} from the control block in Fig. 2 are mirrored to M_{13} and M_{14} in Fig. 3. The currents in the loads and the input pair are respectively controlled by I_{C1} and I_{C2} as shown in Fig. 3. From (6), (7), and (8) the sum of the currents through M_7 and M_8 is equal to $2(k+1+a^2x^2)$, which is a function of the control voltage V_C ($x = V_C$). Upon the change of currents in M_7 and M_8, the common-mode feedback circuit with a high gain is used to stabilize the output common mode level as shown in Fig. 3.

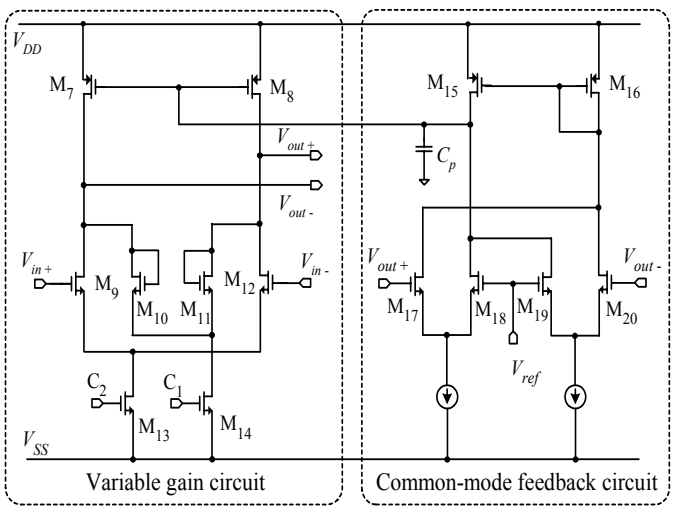

Fig. 3 Circuit schematic of amplifying block.

The differential gain of the amplifier in Fig.3 is expressed as

$$A_v = \frac{g_{m-input}}{g_{m-load}} = \sqrt{\frac{(W/L)_{input} I_{C2}}{(W/L)_{load} I_{C1}}} \qquad (9)$$

where $g_{m\text{-}input}$ is the transconductance of the input transistors (M_9 and M_{12}), $g_{m\text{-}load}$ is the transconductance of the diode connected loads (M_{10} and M_{11}), and I_{C1} and I_{C2} are given in (8). From (8) and (9) the differential gain is calculated as

$$A_v = \frac{g_{m-input}}{g_{m-load}} = \sqrt{\frac{(W/L)_{input}}{(W/L)_{load}} \times \frac{\left[k+\left(1+ax\right)^2\right]}{\left[k+\left(1-ax\right)^2\right]}} \qquad (10),$$

which is the same form of expression as (3). As in (10), the differential gain is a function of the control voltage V_C. By adjusting the bias current I_0 to get $k = 0.15$, the amplifying block in Fig. 3 can provide more than 60dB of the gain variation. Note that the dB-linear characteristic of $(I_{C2}/I_{C1})^{1/2}$ in (9) is equivalent to (I_{C2}/I_{C1}) by the nature of exponential functions.

The bandwidth of the proposed VGA is a function of the output impedance and capacitance. The load is mainly composed of two diode-connected transistors (M_{10} and M_{11}), so that the output impedance is proportional to $g_{m\text{-}load}$, which is determined by the current I_{C1}. Since the I_{C1} varies with the square root of the control voltage V_C, the bandwidth of the proposed VGA has different values between the low- and high-gain modes. The $g_{m\text{-}load}$ increases and decreases at low- and high-gain modes, leading to wide and narrow bandwidths of the VGA, respectively.

Fig. 4 shows the block diagram of the overall VGA. The VGA adopts two amplifying blocks in cascade so that more than 120dB of the gain variation can be obtained. The 1st VGA cell is the same as the 2nd one, which is shown in Fig. 3. The control stage in Fig.4 generates two currents I_{C1} and I_{C2}, which are functions of the control voltage V_C. The bias current, I_0, can be tunable to change the value of k in (10) so that the gain control range of the VGA in Fig. 3 can be adjusted. The buffer circuit shifts the differential gain to positive values, and provides 50Ω output impedance for the conveniences of the measurements.

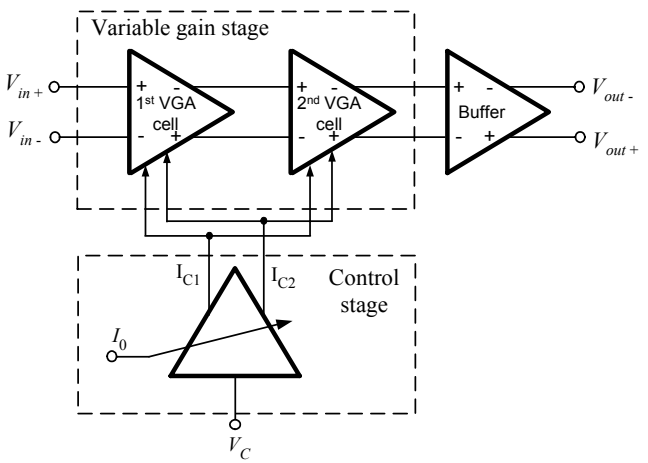

Fig. 4 Block diagram of the proposed 2-stage VGA.

Measurement results

The two-stage VGA is fabricated in 0.18μm CMOS technology with the supply voltages V_{DD} = 1.8V and V_{SS} = 0V. The threshold voltages of NMOS and PMOS transistors in the given technology are about 0.4V, hence the V_C is from 0.4 to 1.4V. Fig. 5 shows the measured gain versus control voltage V_C at 20MHz. In Fig. 5, the VGA shows a total gain range of 84dB and an 80dB of the gain variation with a linearity error of less than ±1dB while dissipating less than 3.6mA. At maximum gain, the $g_{m\text{-}load}$ is minimal so that the bandwidth is smallest; the measured bandwidth at 36dB gain is 40MHz. The bandwidth increases when the gain is reduced. At minimum gain, the $g_{m\text{-}load}$ is maximized and the 3dB-bandwidth is about 1GHz. The P1dB at maximum and minimum gains are measured respectively as -42 and -22dBm. The overall VGA performance is summarized in Table.I. The microphotographs of the chip and layout are shown in Fig. 6. and Fig. 7. The chip area excluding bondpads is less than 0.4mm^2.

The reduction in the gain variation range, about 40dB, compared to the theoretical prediction, is due to the

shortcoming of the amplifier topology: as the currents I_{C1} and I_{C2} become too small or large, the transistors M_9-M_{12} enter subthreshold or linear mode operation, respectively, then (9) becomes invalid. However, the proposed VGA still offers a 50dB gain range improvement compared to the two-stage VGAs which adopt the conventional pseudo-exponential approximation function as in (1). This improvement is significant.

Conclusions

An all-CMOS VGA with a small chip size and low-power consumption is proposed in this paper. The new exponential approximation function with a very wide dB-linear control range is utilized, so that fewer VGA stages are needed to satisfy the required dB gain range. Consequently, the chip size (or the cost) and the power consumption are reduced drastically, while still achieving a very wide gain control range. The VGA topology that implements the new exponential approximation function is newly proposed, implemented, and verified through the measurement. The proposed VGA is implemented in 0.18μm CMOS technology and measurements show the gain variation of more than 84dB in two cascaded stages, and 80dB-linear range with a linearity error of less than ±1dB. The P1dB and 3dB-bandwidth vary from -42dBm (40MHz bandwidth at maximum gain) to -22dBm (1GHz bandwidth at minimum gain). The power dissipation is less than 3.6mA from 1.8V supply.

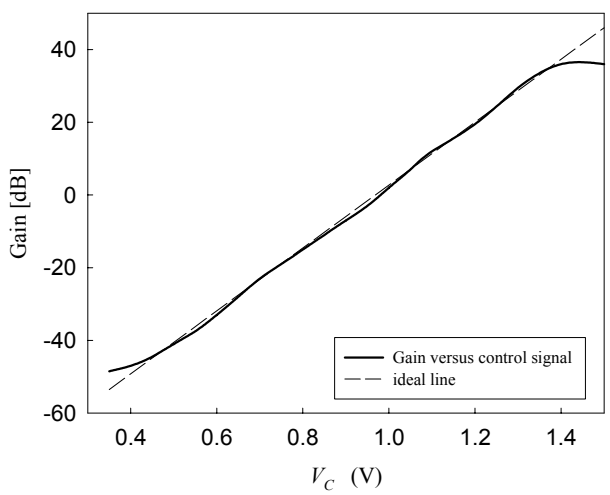

Fig. 5 Measured gain versus control voltage V_C of the proposed circuit shown in Fig. 4.

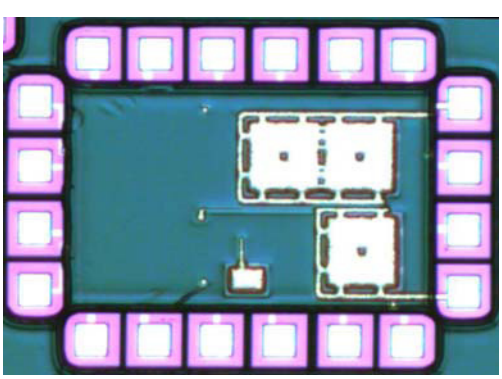

Fig. 6 Microphotograph of the proposed two-stage VGA chip

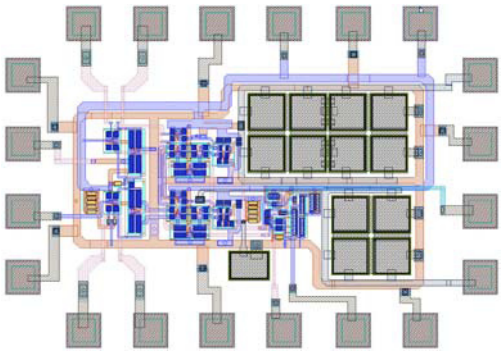

Fig. 7 The layout of the proposed two-stage VGA.

TABLE I
SUMMARY OF MEASUREMENT RESULTS

Technology	0.18μm
Die area	0.4mm^2
Supply Voltage	V_{DD} = 1.8V, V_{SS} = 0V
Current Consumption	3.6mA
Input frequency range	40MHz ~ 1GHz
Gain range	-48dB ~ 36dB
Gain error	±1dB
Input P1dB at maximum gain	-42dBm
Input P1dB at minimum gain	-22dBm

Acknowledgements

The work is supported by the Digital Media Lab which is funded by the Ministry of Information and Communication, Korea.

References

[1] R. Harjani, "A Low-Power CMOS VGA for 50 Mb/s Disk Drive Read Channels," ***Tran. on cir. and syst.-II***, vol. 42, pp 370-376, June 1995.

[2] Christopher W. M, "A Variable Gain CMOS Amplifier with Exponential Gain Control," ***Dig. Symp. VLSI Circuits***, pp. 146-149, 2000.

[3] P. Huang, L.Y. Chiou, and C.K. Wang, "A 3.3-V CMOS Wideband Exponential Control Variable-Gain-Amplifier," ***Inter. Sym. On Cir. and Syst.***, pp. I-285-I-288, May 1998.

[4] M. M. Green and S. Joshi, "A 1.5-V CMOS VGA Based on Pseudo-Differential Structures," ***Inter. Sym. On Cir. and Syst.***, pp. IV-461-IV-464, May 2000.

[5] C.-C Chang, M.-L. Lin, and S.-I. Liu, "CMOS Current-mode Exponential-Control Variable-Gain Amplifier," ***IEE Electronics Letters***, vol. 37, no. 14, pp 868-869, July 2001.

[6] S. Otaka, G. Takemura, and H. Tanimoto, "A Low-Power Low-Noise Accurate Linear-in-dB Variable-Gain Amplifier with 500-MHz Bandwidth," ***J. of Solid-State Circuits***, vol. 35, no. 12, pp1942-1948, Dec. 2000.

[7] Quoc-Hoang Duong and S.-G. Lee, "CMOS Exponential Current-to-Voltage Circuit based on newly Proposed Approximation method," ***Inter. Sym. On Cir. and Syst.***, pp II.866-II.868, May, 2004.