A 2.5Gb/s CMOS Transimpedance Amplifier Using Novel Active Inductor Load

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Abstract

A high-speed and low power transimpedance amplifier for 2.5Gb/s applications has been implemented in 0.35μm CMOS technology. For higher transimpedance gain and wider bandwidth, in this paper, an inductive shunt peaking technique is applied using a novel active inductor load that can be used at 1 ~ 2GHz range. Measured performance shows 1.45GHz bandwidth with 57dBΩ transimpedance gain and the power consumption of about 50mW.

I. Introduction

As motivated by the huge data transmission capacity for multimedia communications, optical communication systems, such as LAN (Local Area Networks) and FTTH (Fiber-To-The-Home), are booming today. The performance of the optical interconnection system depends on the receiver's gain, bandwidth, power consumption, and noise figure. These four parameters tend to trade-off with each other [1].

The front-end component of typical optical receiver generally is an amplifier. The typical amplifier generally requires a low-noise characteristic in order to achieve a good noise performance of overall receiver system. And the amplifier should operate a high of an input signal as possible without being saturated.

To meet the noise requirement, two different types of amplifier architectures are available [2]. One is high input impedance amplifier for low noise, and the other is transimpedance amplifier using resistive shunt-shunt feedback. The high impedance amplifier can provide lower noise, but bandwidth can be reduced significantly due to the longer input RC time constant, and therefore, another circuit like equalizer to compensate the bandwidth reduction. In contrast, the transimpedance amplifier has more noise due to feedback resistance but wide bandwidth and the design is simple. Furthermore, the transimpedance amplifier has wide dynamic range due to the higher saturation limit. Thus, transimpedance amplifier (TIA) architecture is widely used in optical receiver systems.

In designing the TIA, to satisfy the given data rate of an optical receiver, the amplifier should have a proper bandwidth [3]. For example, to support the 2.5Gb/s application, the optimum bandwidth could be approximately 1.3 GHz. Typically for given technology, obtaining wider bandwidth involves higher power consumption. Therefore, designing a circuit with less amount of power consumption is a major design challenge from the reliability and the power saving aspects especially with CMOS technologies.

In this paper a transimpedance amplifier (TIA) is designed for 2.5Gb/s optical communication system based on 0.35μm CMOS technology. Though the traditional TIA is designed using more expensive IC technologies such as silicon bipolar or GaAs MESFET, there has been an increasing interests in CMOS based implementation because of the demand for the lower cost and greater integration with digital circuits. In this paper, the TIA is designed as a part of 12 channel optical interconnection system including VCSEL (Vertical Cavity Surface Emitting Lasers) driving circuits.

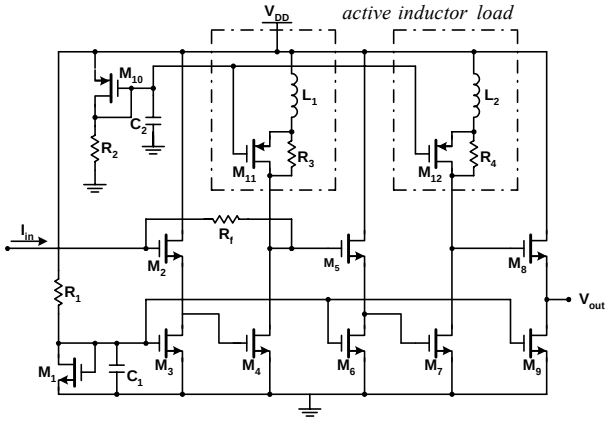

Figure 1. Schematic diagram of TIA

II. Circuit Design and Performances

A. Circuit Design

The schematic diagram of the designed TIA is shown in Fig. 1. As shown in Figure 1, M_2 and M_3, M_5 and M_6, and M_8 and M_9 compose source-follower circuit. In addition, M_4 and M_7 in Fig. 1 construct a common-source

amplifier with an active inductor load that will be introduced later. M_3, M_6, and M_9 are used as current sources of source-follower circuits. As can be seen in Fig. 1, the cascade of M_2 and M_4, and the cascade of M_5 and M_7 are the Common-Drain (CD) and Common-Source (CS) combination (CD-CS). The combination of M_8 and M_9 are used as an output buffer. The R_f is the shunt feedback resistor making TIA. The C_1 and C_2 are used for ac ground. The rests are biasing circuits.

As well known, the combination of CD-CS is widely used for wideband amplifier. As the cascade of these two amplifiers reduce the input capacitance while providing low impedance at the gate node of CS amplifier [5]. For a given total amount of current, the current distribution between CD and CS has the gain versus bandwidth trade-off. If the more current are allocated to the CD stage than to the CS amplifier, this will introduce less amount of resistance at the gate node of CS amplifier while the voltage gain of the CS is being reduced because of lower current. The reduced gain leads to less Miller capacitance at the gate node of CS amplifier. Therefore, the more current allocation to CD stage results in wider bandwidth at the expense of gain. In contrast, if more current are allocated to the CS amplifier, then the gate node of CS will have larger resistance as well as larger amount of parasitic capacitance because of higher gain of CS amplifier stage. Therefore, the overall gain of CD-CS will increase while the bandwidth decreases.

In the design shown in Fig. 1, more current are allocated to the CS stage of the CD-CS cascade in order to obtain higher amount of overall gain. To alleviate the bandwidth reduction by the higher amount of gain inductive shunt-peaking technique has been applied using a novel active inductor load.

B. Bandwidth Enhancement Using Inductive Shunt-Peaking

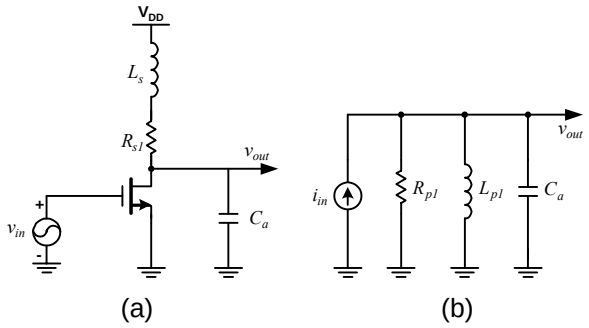

Figure 2. (a) Typical shunt-peaked amplifier (b) the output equivalent circuit

Fig. 2(a) shows a well-known inductive shunt-peaked amplifier [6]. In Fig. 2, the series resistance R_{s1} is used as a load and the capacitance C_a includes all the capacitance at the output node. When this amplifier is used for a wideband application, bandwidth is limited by the time constant $R_{s1} \cdot C_a$. By connecting an inductance L_s in series with R_{s1} the bandwidth of the amplifier can be extended. The bandwidth extension is accomplished by the resonance of L_s with C_a. occurs at the frequency where L_s and C_a resonates. The resonance phenomenon can be better understood by the equivalent representation shown in Fig. 2(b) where L_{p1} and R_{p1} are the parallel representation of L_s and R_{s1}. Here, L_{p1} and R_{p1} can be given by[6]

$$R_{p1} = R_{s1}(Q^2 + 1)$$
$$L_{p1} = L_s\left(\frac{Q^2 + 1}{Q^2}\right) \qquad (1)$$
$$where \quad Q = \frac{R_{p1}}{\omega_0 L_{p1}} = \frac{\omega_0 L_s}{R_{s1}}$$

In order to get the bandwidth extension effect by the peaking phenomenon, the resonance frequency determined parallel-connected L_{p1} and C_a should be near the desired corner frequency (f_{-3dB}).

In many practical situations, the DC voltage drop limits the load resistance R_{s1}. Therefore, from Eq. (1), L_{p1} is not so much greater than L_s as the Q-factor is rather high. For a typical parasitic output capacitance C_a and the reasonable value of on-chip inductor L_s (typically less than 15nH), the resonance frequency of L_{p1} and C_a tends to be higher than 4GHz. However, the 3-dB bandwidth of the given amplifier is usually much less than that. Therefore, the conventional inductive shunt-peaking provide little improvement in bandwidth. In order to bring the resonance frequency close to the bandwidth, the inductance L_s has to be unrealistically high.

To provide a large value inductance to the shunt-peaking amplifier architecture, in this paper, a novel active inductor architecture is proposed. Fig. 3(a) shows the CS amplifier portion of the circuit with the proposed active inductor load. In Fig. 3(a), the PMOSFET M_p is used for the current bleeding purposes in order to reduce the voltage drop across load resistor R_{s2}. For the same available voltage drop, much larger load resistor can be used and the DC voltage can be specified for the direct coupling with next stage. The capacitance C_b includes all the parasitic capacitance that exists at the output node of the amplifier, such as the drain to substrate capacitance of M_p and M_n, the drain to gate capacitance of M_p and M_n, and the load capacitance. Fig. 3(b) shows the small signal equivalent circuit of the active inductive load represented as Z_{out} in Fig. 3(a). From Fig. 3(b) the output load impedance Z_{out} can be drived as

$$Z_{out}(s) = \frac{v_x}{i_x} = R_{s2} + \frac{1 + g_m R_L}{1 - \omega^2 C_{gs} L_s} sL_s \qquad (2)$$
$$where \ R_L = R_{s2} \,//\, r_0$$

As can be seen in Eq. (2), Z_{out} represents a series connection of resistance R_{s2} and an inductor with a multiplication factor. In Eq. (2), as the frequency approaches the resonance frequency of $C_{gs}{\cdot}L_s$, the inductive component of the output impedance approaches infinite. Therefore, at frequencies below the $C_{gs}{\cdot}L_s$ resonance frequency, Z_{out} becomes equivalent to Fig. 4(c). Above the resonance frequency the second term of Eq. (2) becomes a capacitive. Thus, the amplifier of Figure 3 (a) using the proposed novel active inductor load effectively becomes the same architecture like the typical shunt-peaked amplifier shown in Fig. 2(a). The differences are that the inductance L_{eq} can be much larger than L_s, and the resistor R_{s2} can also be larger value than R_{s1}. So, the output part of Fig. 3(a) can be represented as shown in Fig. 3(d). If we compare the schematic of Fig. 3(d) with that of Fig. 2(b), L_{p2} is much larger than L_{p1}, and the capacitance C_b is slightly higher than C_a due to the additional capacitance from M_p. Therefore, the proposed active inductor load can induce inductive shunt-peaking effect using practical inductor size at the frequency of interest, in this case 1 to 2 GHz range.

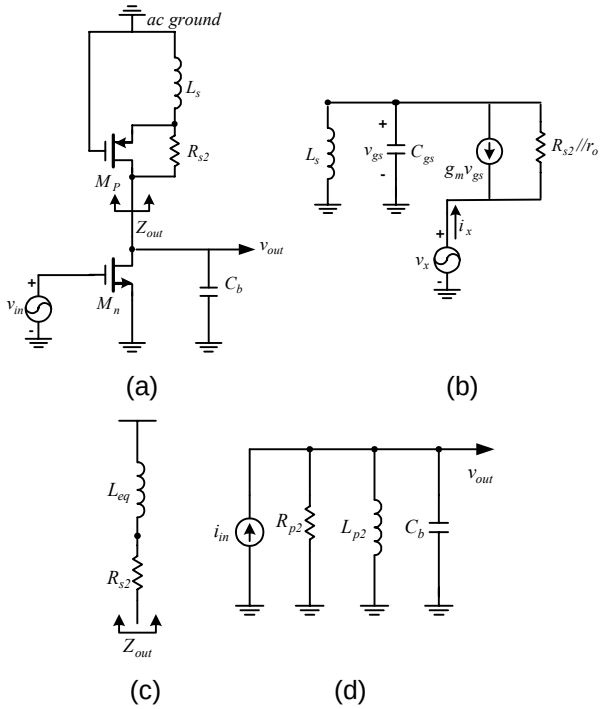

Figure 3. (a) A shunt-peaked amplifier with proposed active inductor load (b) the small-signal equivalent circuit for the active inductor (c) equivalent circuit for Fig. 3(b) (d) the output equivalent circuit for Fig. 3(a)

In order to demonstrate the phenomenon a simulation results is included. Figure 4 compares the simulation results of two different shunt-peaking architectures (Figure 2 (a) and Figure 3 (a)). In the simulation in order to keep the same DC bias, R_{s1} is set to 250Ω while R_{s2} 500Ω. A 15nH inductor is used for L_s. As shown in Fig. 4, the load impedance of the proposed architecture shows inductive peaking at much lower frequency near 2GHz while conventional topology shows inductive peaking near 4GHz. Therefore, by adopting the proposed active inductor load, the bandwidth of the CS amplifier could be improved at the frequency of interest.

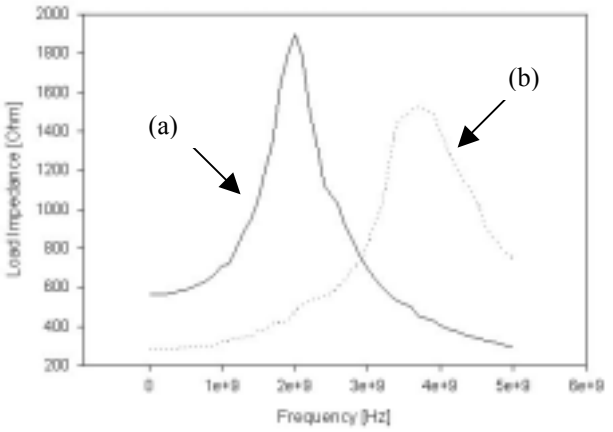

Figure 4. Simulation result of load impedance of two different types of shunt-peaking (a) load impedance with the proposed active inductor (b) load of conventional shunt-peaked output

C. Measurement Results

The TIA shown in Figure 1 is implemented with 0.35μm CMOS technology, and the power dissipation is 50 mW with 3.3V supply voltage. The microphotograph of the chip is shown in Fig. 5 and 6. Fig. 5 represents an array implementation of 6 channel TIA, and Fig. 6 is a single TIA for testing purposes. Fig. 7 shows measurement set-up of the fabricated chip [4].

Fig. 8 shows the measured gain versus frequency response of the TIA. As can be seen Figure 8, the transimpedance gain is a 57dB and the bandwidth is 1.45GHz, which makes the amplifier suitable for 2.5Gb/s application. Fig. 9 shows the output impedance as a function of frequency. In Figure 9, more than 10dB return loss is obtained up to the 3-dB frequency.

The noise measurements are under process and will be included in the final paper. However, some of the preliminary measurement results indicate a good noise performance.

III. Conclusions

A high speed and low power transimpedance amplifier for 2.5Gb/s application is introduced. By adopting novel active inductor architecture, which is composed of an on-chip inductor, a PMOS transistor, and a load resistor, the bandwidth of 1.45 GHz and the transimpedance of 57 dB are successfully demonstrated with 50 mW of power dissipation. The proposed active

inductor can be useful for low-frequency inductive peaking purposes (below 3 GHz). The TIA is implemented on a 0.35 micron CMOS technology.

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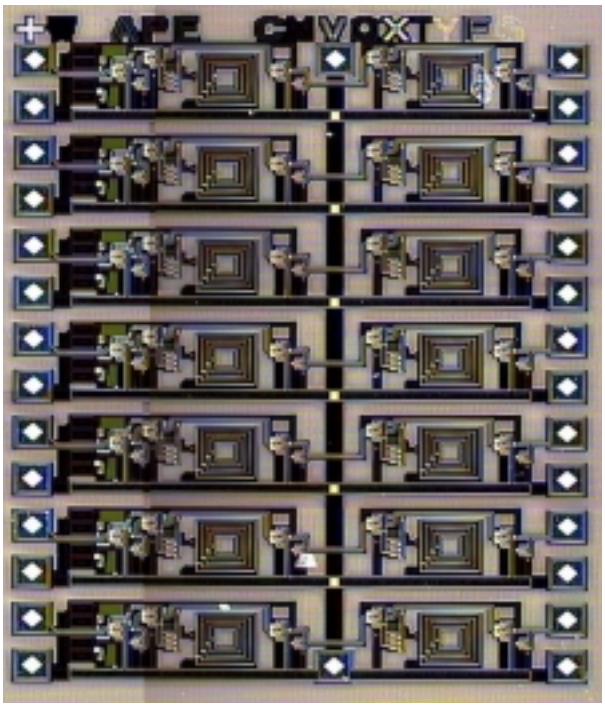

Figure 5. The microphotograph for the 6 channel TIA array

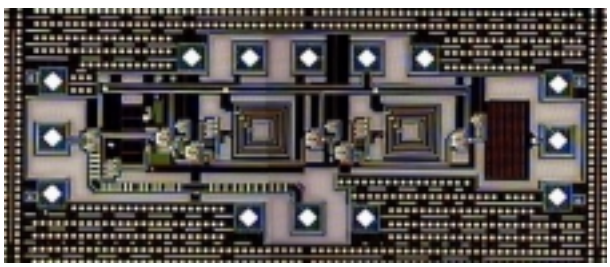

Figure 6. The microphotograph for the single channel TIA for the measurements

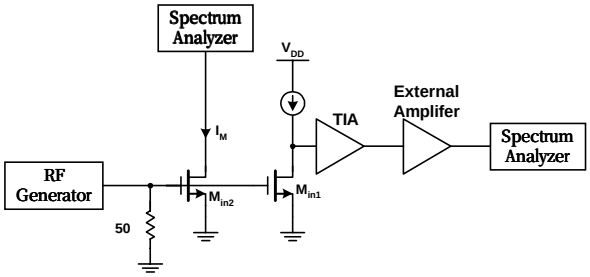

Figure 7. Measurement set-up for TIA including voltage-to-current converter circuit

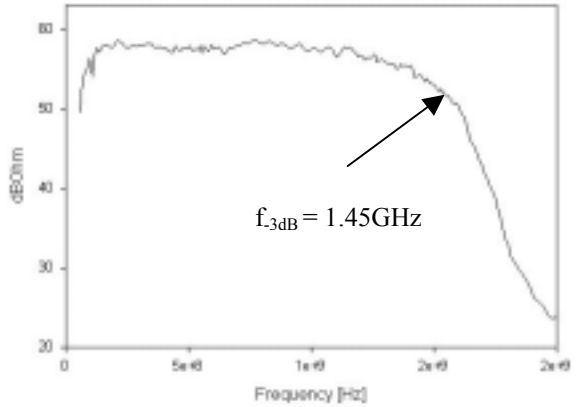

Figure 8. Measurement result of transimpednce gain

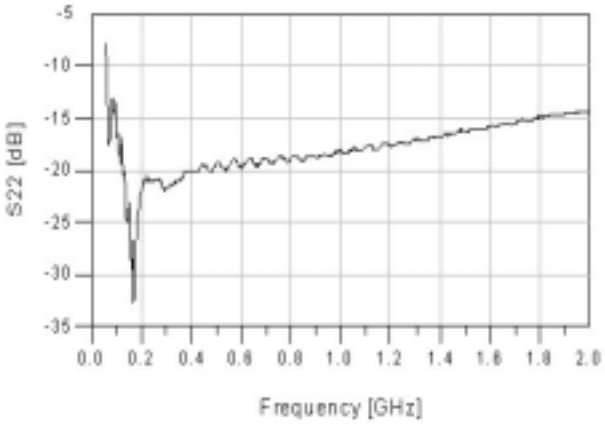

Figure 8. Measurement result of output impedance