RF CMOS Differential Oscillator with Source Damping Resistors

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Abstract — **This paper proposes a new method to suppress 1/f noise contribution of active devices in oscillator using source damping resistors. The operational mechanism of proposed source damping resistor method is analyzed through circuit simulation with complementary LC differential oscillator topology. This analysis shows that the amount of 1/f noise and the mismatch of instant current swing of oscillator's active devices can be substantially reduced with source damping resistors. The reduced 1/f noise and instant current mismatch leads to the phase noise improvement by suppressing 1/f noise up-conversion to phase noise. To prove experimentally the usability of proposed resistor damping technique, two complementary LC differential VCOs with different damping conditions are fabricated using 0.18μm CMOS technology. The measurement result shows that there is about 6.0dBc, 4.0dBc and 1.0dBc of phase noise improvement at 10 kHz, 100kHz and 1MHz offset frequency with source damping resistors, respectively.**

Index Terms — **CMOS, oscillator, 1/f noise, phase noise, damping resistors.**

I. INTRODUCTION

With the improvement of RF CMOS process technology, the active researches to develop very compact and multi-function wireless devices are in process using one-chip CMOS wireless transceivers Recently, Advanced RF silicon CMOS process technologies are solved most problems from conductive substrate, and resistance of interconnection line and operation frequency of active devices. Poly capacitor is replaced by high-Q MIM capacitor and the Q-factor of inductor is improved to more than 10 with thick metal and copper process technology. Unit current gain frequency of N-MOSFET approaches to 100GHz by the scale-down of channel length. But, even though the performance of RF CMOS transistors is improved, the inherent 1/f noise is still an obstacle in the design of integrated low phase noise VCO. The impact of 1/f noise becomes more severe with the decrease in channel length.

In previously reported paper's related with VCO design, there are many different approaches to decrease the phase noise contribution by 1/f noise. The first method is to use PMOS device in VCO design, which is known that PMOS transistor has a decade lower 1/f noise than PMOS [1-2]. The second method is to use capacitive coupling to suppress 1/f noise up-conversion in differential LC oscillator [3]. The third method is to control body node bias in ring oscillator [4]. The fourth method is to replace the current source as LC tank circuit to suppress 1/f noise contribution by tail current [5]. The fifth method is the symmetric VCO design approach [6].

In this paper, a new method using source damping resistor method is introduced and the operational mechanism analyzed. And the new 1/f noise suppression method is proved with experimentally using fully integrated complementary differential oscillator using 0.18μm CMOS process.

II. 1/F NOISE IN CMOS COMMON-SOURCE AMPLIFIER

The low frequency 1/f noise is the inherent property of silicon transistors. Between CMOS and Bipolar transistors, it is known that CMOS transistor has higher 1/f noise spectral density and the corner frequency reaches from several hundred kHz to several MHz. The 1/f noise of CMOS transistor can be modelled as a voltage source in series with the gate and which is inversely proportional to the size of transistor and frequency [7]. Thus, the more CMOS technology is scale-down, the more serious the effect of 1/f noise is. Also in CMOS oscillators, since the low frequency 1/f noise is up-converted to the oscillation frequency, the phase noise performance below several MHz offset frequency is dominated by the 1/f noise of MOS transistors.

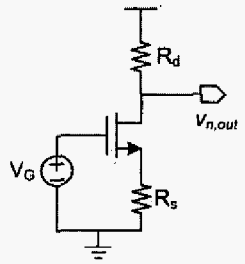

Fig. 1 Common-source amplifier with resistance degeneration

In MOS transistor, the output noise current increases in proportional to the square of the transconductance.

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Conventionally, an oscillator generates large signal swing and the large signal swing leads to large transconductance variation on transistors. Thus, it can be expected that the large signal swing may generate excess 1/f output noise current during oscillation and a cautiously selected degeneration resistance can remove the excess 1/f output noise current.

Fig. 1 is a common-source amplifier with source degeneration resistor. In Fig. 1, R_s and R_d is the degeneration and load resistors, respectively. V_G is gate bias voltage, $v_{n,out}$ output noise voltage. Fig. 2 shows the simulated output noise voltage for the cases with R_s = 0 and 50Ω using 0.18um CMOS, where R_d = 1Ω. From Fig. 2, it is confirmed that the source degeneration resistor suppresses considerably low frequency output noise voltage resulted from 1/f noise, especially with large gate bias voltage (V_G = 1.0V and 1.5V). This mean that if the properly selected degeneration resistors are adopted in CMOS oscillator, the 1/f noise output current of CMOS transistor at oscillation peak can be suppressed considerably and which would be lead to phase noise improvement.

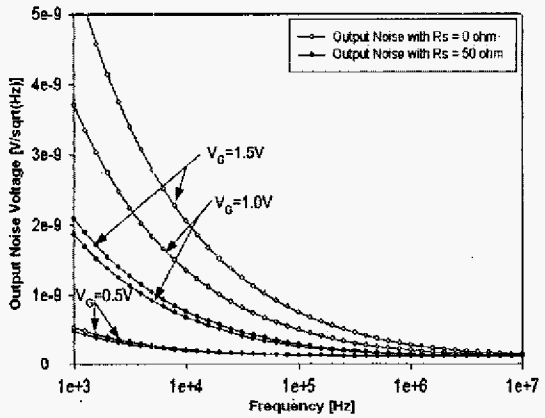

Fig.2 Low frequency output noise voltage ($v_{n,out}$)

III. CMOS DIFFERENTIAL LC OSCILLATORS WITH SOURCE DAMPING RESISTORS

To verify above discussion in Section II, a conventional differential LC oscillator with source damping resistors is configures as shown in Fig. 3. In oscillation, the source degeneration resistors are renamed as "damping resistors" since they work as damping factors during oscillation. As shown in Fig. 3, each N- and PMOS transistor has a damping resistor, R_s, in series with source node. Power is supplied by an ideal current source. C_{by} is a bypass capacitor to ground node. Tank inductance, L_{tank}, and capacitance, C_{tank}, are selected to oscillate at 2.0 GHz. Tank capacitor is an ideal component and the tank inductor is modelled real component provided by foundry and Q-factor ≈ 10.0 at 2 GHz. For simulation, 0.18μm CMOS technology is used, which has embedded 1/f noise model in active device. With 3mA of supply current, the phase noise simulation is performed for the cases of R_s = 0Ω and 40Ω, respectively.

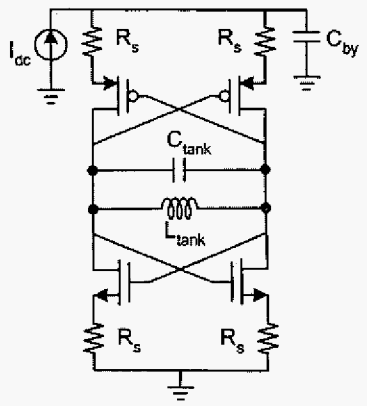

Fig. 3 CMOS complementary differential LC oscillator with damping resistors

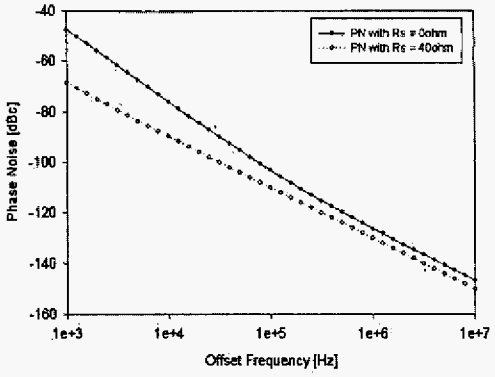

Fig. 4 Phase noise performance in differential LC oscillator

Fig. 4 shows the simulated phase noise performance of complementary differential LC oscillator shown in Fig. 3. As shown in Fig. 4, the phase noise performance with damping resistors (R_s=40Ω) is improved considerably compared to that of R_s=0Ω. In $1/f^3$ phase noise region, the phase noise improvements becomes more as the offset frequency becomes lower. Since the $1/f^3$ region in phase noise is due to 1/f noise, this simulation results confirm well the previous discussions and simulation results in Section II. Damping resistors can suppress effectively the 1/f noise output current of active devices in CMOS oscillator.

Fig. 5 and 6 shows the simulated instant drain current of N- and PMOS transistor and the drain voltage swing of the differential oscillator shown in Fig. 3. In Fig. 5 and Fig. 6, R_s=0Ω and 40Ω, respectively. As shown in Fig. 5 and 6, Fig. 5 shows almost two times more instant drain current swing than that of Fig. 6. Considering that the output 1/f noise current of active device is in proportion to

tranconductance, the output 1/f noise current will also increase in proportion to drain current swing.

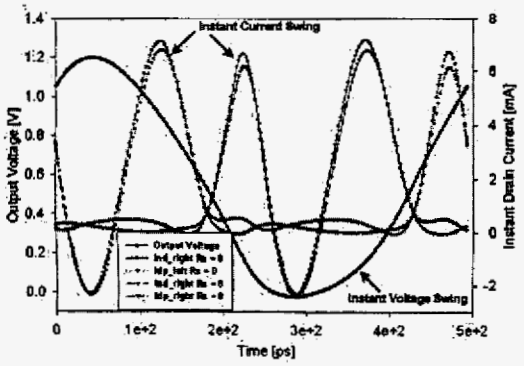

Fig. 5 Instant drain current and voltage with R_s=0ohm

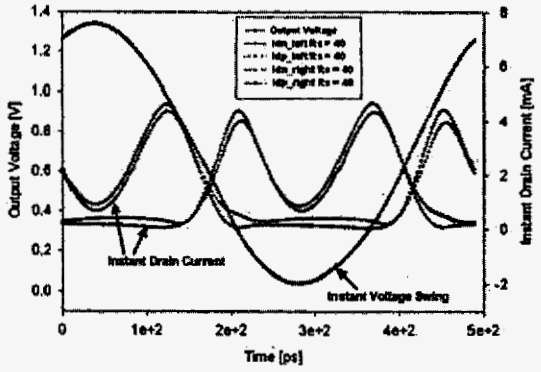

Fig. 6 Instant drain current and voltage with R_s=40ohm

In Fig. 6 and Fig. 5, the waveform of the instant drain current swing is more symmetric in Fig. 6 than that in Fig. 5. Distortion in the sinusoidal instant drain voltage swing is shown in Fig. 5, and which is caused by the asymmetrical drain current swing as shown in Fig. 5. The symmetric current swing waveform of Fig. 6 can be understood as the transconductance of N- and PMOS transistor is equalized as $1/g_m+R_s$ with damping resistance. The g_m symmetry of N- and PMOS transistors of complementary structure is also an important factor in up/down oscillation swing symmetry [6].

Comparing the drain current swing amplitude and symmetry, it can be expected that the phase noise performance is good in Fig. 6 with $R_s = 40\Omega$ as same with the phase noise simulation in Fig. 3. As shown in Fig. 4, the phase noise improvement with $R_s = 40\Omega$ in $1/f^2$ region (note the curve shift) can be understood by the difference of the instant drain current swing amplitude in Fig. 5 and 6. From above simulation results, the phase noise improvement of CMOS differential LC oscillator with source damping resistor is confirmed. But, the source damping resistance value must be cautiously selected since the over-damped resistance value can seriously decrease the oscillation swing amplitude and even prevent the start-up of oscillation.

IV. MEASUREMENT RESULTS

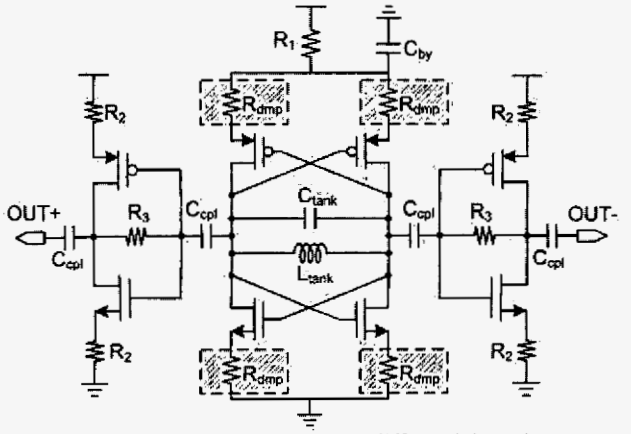

Fig.7 Fabricated complementary differential LC VCO schematic with source damping resistors

To prove experimentally the effectiveness of the proposed source damping resistor method, complementary differential LC VCOs are implemented using 0.18μm CMOS technology. Fig. 7 shows the fabricated complementary differential LC VCO schematic. R_{dmp} is the source damping resistors. Two cases of source damping resistors: (a) $R_{dmp} = 0\Omega$, (b) R_{dmp}=40Ω are used. The inverter amplifiers with feedback resistor R_3 and degeneration resistor R_2 are used for VCO buffer. R_1 is to control DC bias current. C_{cpl} and C_{by} are AC coupling and bypass capacitor, respectively. A spiral inductor L_{tank} has about 10 of Q-factor. C_{tank} is composed as MIM capacitors and MOS variable capacitors. L_{tank} and C_{tank} are chosen as the fabricated VCOs oscillate at 2 GHz band.

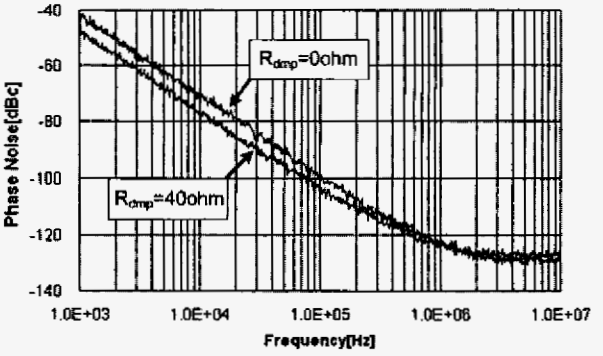

Fig.8 Measured phase noise performance for the cases of R_{dmp} = 0Ω and 40Ω

The phase noise performances of fabricated VCOs are measured using 4352B VCO/PLL signal analyzer. With 1.8V supply voltage, the VCOs with R_{dmp}=40Ω and R_{dmp}=0Ω are oscillated at 2.2 GHz and 2.22 GHz while

flowing 11.3mA and 10.3mA, respectively. DC current includes the current of inverter buffer amplifier. Measured phase noise performances are plotted in Fig. 8. As shown in Fig. 8, the better phase noise performance is achieved with R_{dmp}=40Ω than that with R_{dmp}=0Ω. As the offset frequency becomes lower ($1/f^3$ phase noise region), the phase noise with R_{dmp}=40Ω shows more improvement. The phase noise difference between these two source-damping cases is plotted in Fig. 9. Fig. 9 shows that, with R_{dmp}=40Ω, the phase noise improvement shows linear dependency over the offset frequency region from 20 kHz to 1.1MHz and becomes constant below 20 kHz. Even though the constant phase noise improvement below 20 kHz cannot be explained; the linear dependency of phase noise improvement over the offset frequency coincides exactly with expected simulation result, which proves that source damping resistors can suppress effectively the 1/f noise contribution of active devices in CMOS oscillator. Above 1.1 MHz of offset frequency, the phase noise with R_{dmp}=40Ω is about 1.0dBc worse than that with R_{dmp}=0Ω. This can explained as the VCO noise floor with R_{dmp}=40Ω becomes higher than that with R_{dmp}=0Ω. From Fig. 9, the phase noise improvement with R_{dmp}=40Ω is shown about 6.0dBc, 4.0dBc and 1.0dBc at 10 kHz, 100 kHz and 1 MHz, respectively. Fig. 10 shows the micrograph of the fabricated differential LC VCO. In Table I, measurement results are summarized.

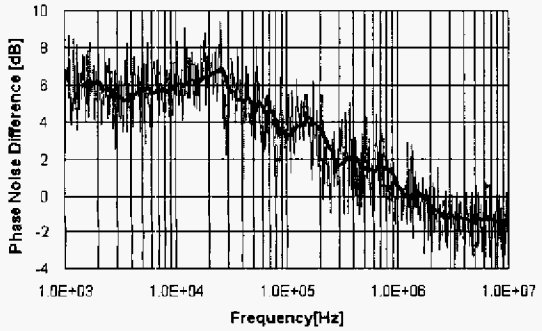

Fig.9 Measured phase noise improvement with R_{dmp} = 40 Ω over R_{dmp} = 0Ω

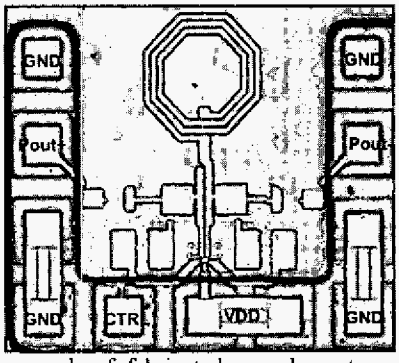

Fig.10 Micrograph of fabricated complementary differential LC oscillator

Table I Measurement results with 1.8V supply voltage

R_{dmp}	I_{DC}* [mA]	Freq. [GHz]	Phase Noise [dBc]		
			10kHz	100kHz	1MHz
0Ω	11.3	2.20G	-81.49	-99.9	-129.32
40Ω	10.3	2.22G	-86.88	-103.5	-131.84

I_{DC}* includes current of inverter buffer amplifier.

IV. CONCLUSION

A new source resistor damping method to suppress 1/f noise up-conversion in CMOS oscillator is proposed. Proposed source resistor damping method is simulated with the common-source amplifier and complementary LC differential oscillator with 0.18μm CMOS technology. The simulation results show that the amount of 1/f noise and the mismatch of instant current swing of oscillator's active devices can be suppressed substantially using source damping (degeneration) resistors, which leads to phase noise improvement in CMOS oscillator.

Two kinds of complementary differential LC CMOS VCOs with different damping condition: (a) R_{dmp} = 0Ω, (b) R_{dmp}=40Ω are fabricated with 0.18μm CMOS technology. Measurement results show that there is about 6.0dBc, 4.0dBc and 1.0dBc of phase noise improvement at 10 kHz, 100kHz and 1MHz offset frequency with source damping resistors, respectively.

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