

A Low-Voltage Low-Power High dB-linear and all CMOS Exponential V-I Conversion Circuit

Quoc-Hoang Duong, *Student Member, IEEE*, and Sang-Gug Lee, *Member, IEEE*

RFME Laboratory, Information and Communications University,
119-Mujro, Daejeon, Republic of Korea, 305-714.
EMAIL: hoang@icu.ac.kr PHONE: 82-42-866-6293

Abstract – A very compact, all CMOS, exponential V-I conversion circuit is proposed for low-voltage and low-power applications. The exponential characteristic is based on the Taylor concept. A new technique to improve the dB-linear output current range of the V-I circuit has been introduced. Based on a 0.18 μm CMOS process, the measured results show 44dB of output current range with a very low current consumption of less than 0.18mA from a 1.2V supply voltage. The chip size, excluding bondpads, is 170x90 μm . The proposed circuit can be used for the design of low-voltage, low-power analog and mixed-mode circuits such as variable gain amplifiers (VGA) and automatic gain control (AGC), and etc.

Index terms – AGC, VGA, V-I converter.

I. INTRODUCTION

The desire for portability of electronic equipment has generated a need for low power systems in battery operated products like hearing aids, cell phones, and hand-held multimedia terminals. Low power consumption is necessary to ensure a reasonable battery lifetime in portable electronics. As well, low-power circuits are expected to reduce thermal dissipation, which is of increasing importance in light of the general trend of miniaturization.

The exponential V-I conversion circuit (EVIC) is the main component for the design of VGAs and AGCs. However, MOS devices that operate in the saturation region provide square-law I-V characteristics, resulting in difficulties in the design of CMOS-based EVICs. Consequently, two exponential approximated methods have been introduced as alternatives. The first method uses the “pseudo-exponential” function [2-4], while the second one expands the exponential relation with the Taylor series and truncates the expansion by the amount of accuracy needed [5-9].

Although the Taylor series expansion, in the author’s opinion, is easily implemented, for example, by implementing only two transistors [6], or by using composite NMOS transistors [7], the previously reported works that adopted this method show a small dB-linear output range (less than 12dB with a linearity error of less

than $\pm 0.5\text{dB}$ [4]-[7]). To increase the dB-linear output range, the “pre-distortion technique” and the “shifted-symmetrical axis technique” were introduced in [8]-[9]. However, the dB-linear ranges are still limited to less than 25dB and the input ranges of these circuits are rather small.

In this paper, we propose a new approach to extend the output dB-linear and input ranges of the Taylor series expansion. Our idea combines the two previously reported techniques used in [8]-[9], and implements into the circuit as an exponential V-I converter. Consequently, a very wide dB-linear range of the output current and a large input range of the EVIC are obtained. We also present ideas to simplify circuit implementations, resulting in a very compact EVIC that offers low-power consumption and small chip size.

II. PROPOSED IDEAS

A. Taylor series expansion

According to the Taylor series expansion, a general exponential function can be expressed as

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \dots + \frac{a^n}{n!}x^n + \dots \quad (1)$$

where a is the coefficient, and x the independent variables, respectively. For $|ax| \ll 1$, (1) can be approximated as

$$f(x) = e^{ax} \cong 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (2).$$

For $|ax| \leq 1$ (2) provides 14dB of amplitude variation, and a linearity error of less than $\pm 0.5\text{dB}$ within 12dB.

B. Pre-distortion technique

The pre-distortion technique is reported in [8]. As in [8], if the variable x in (2) is a linear function of t (let $x = t$ as shown in Fig. 1(b) by the solid line), then the $f(x)$ in (2) as a function of t (*i.e.* $f(x) = f(t)$) shows 12dB with an error of less than $\pm 0.5\text{dB}$ as shown in Fig. 1(a) by the dashed line, which is drawn for the constant $a = 0.1$. The deviation of (2) from the ideal exponential function (1)

increases rapidly as $|x|$ and/or $|t|$ increases, leading to narrow output and input ranges. Now, the variable x is considered as a linear function of t only for $|x| \ll 10$, otherwise, it is a nonlinear function of t as shown in Fig. 1(b) by the dashed line (denoted by $x = f_1(t)$). Intuitively, one can see that (2) as a function of t (i.e. $f(x) = f(f_1(t))$) will be shifted to the ideal exponential function as shown in Fig. 1(a) by the o's symbol line, resulting in the improvement of the dB-linear output range. The nonlinear characteristic of the dashed line in Fig. 1(b) can be easily obtained in MOS transistors in the saturation region, making this method easily implemented. However, this approach has a drawback in that the output dB-linear range is only improved in the positive- t value, leading to a narrow input range of x and/or t as depicted in Fig. 1(a); as well, the dB output range is limited.

C. Shifted symmetric-axis technique

The shifted-symmetrical axis technique was firstly introduced in [9]. This technique implements the exponential approximation as follows:

$$f(x) = e^{ax} \cong 1 + k \left(\frac{a}{1!} x \right) + \frac{a^2}{2!} x^2 \quad (3).$$

If $k = 1$, then (3) becomes (2), which is traditional Taylor approximation function and shows 12dB linear range with ± 0.5 dB linearity error as shown by the solid line in Fig. 2. As reported in [9], for k slightly larger than unity, (3) shows a higher dB output range as shown in Fig. 2. However, this technique extends the dB output range in the negative- x value, resulting in a narrow input range of x as depicted in Fig. 2.

D. Combination of the two techniques

In Fig. 3, the dotted-line shows the traditional Taylor series approximation with 12dB range, a linearity error of less than ± 0.5 dB, and an input x -range from -8 to 12. By using the pre-distortion technique, we get the dashed line which improves the dB range in the positive x -value; and, it is closed to the Taylor series expansion in the negative x -value. If we use (3) with the constant $k = 1.3$, we then get the triangle-line in Fig. 3, which drastically extends the dB output range in the negative x -value. In the positive x -value, a small improvement of the dB range is achieved. By firstly implementing the pre-distortion technique, we get the dashed-line in Fig. 3, we then implement (3) with $k = 1.3$. Consequently, the dashed-line moves to the bold-solid line in the positive x -value, and in the negative x -value, the combination of these two techniques results in the bold-solid line which is closed to the triangle-line. Finally, the combination of these two techniques offers very wide dB output and x -input ranges as shown by the bold-solid line in Fig. 3.

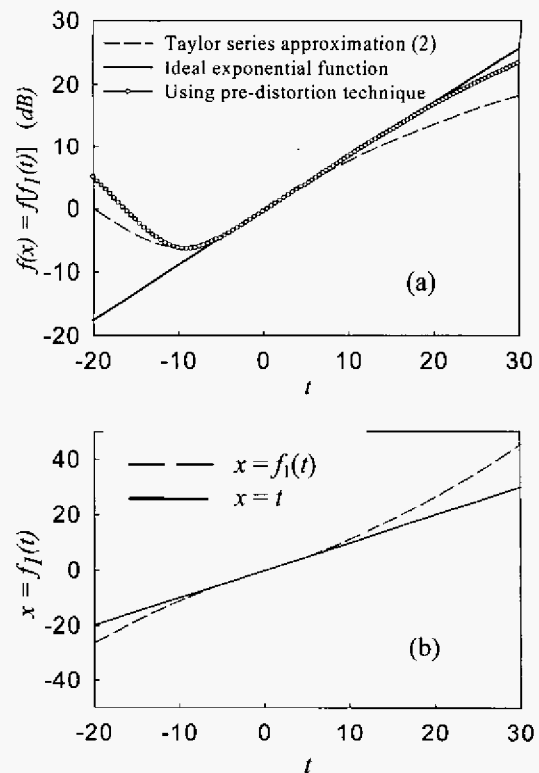


Fig. 1 Plots of various functions on dB-scale

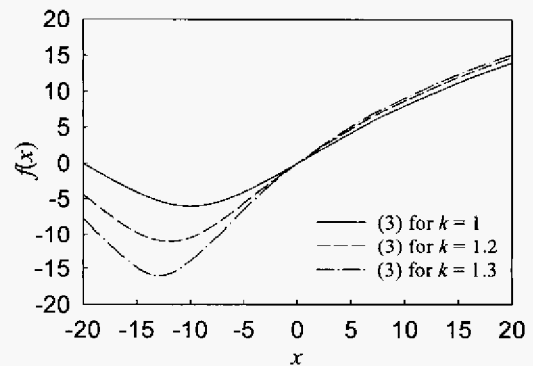


Fig. 2 Plots of (3) on dB-scale for different values of k

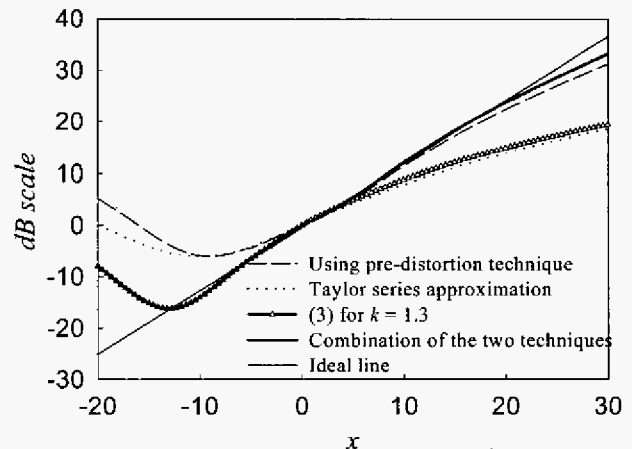


Fig. 3 The combination of the two techniques

III. CIRCUIT IMPLEMENTATIONS

As reported in [8], in order to implement the pre-distortion technique, a nonlinear V-to-I converter is required. Therefore, the proposed EVIC is composed of two circuit blocks: the nonlinear V-to-I converter (NVCC) and the exponential I-to-I converter (ECCC). The ECCC helps to implement the shifted symmetric-axis technique, which will be discussed later. The block diagram of the proposed EVIC is shown in Fig. 4.

Fig. 5 shows the schematic of the proposed EVIC that implements (2) and the combination of the two techniques. The nonlinear V-I converter, reported in [8], is complicated with differential input signals. For the applications of VGAs, a fewer number of control signal lines is preferred. Therefore, this paper proposes a very compact NVCC, which is composed of transistors M1 and M2 as shown in Fig. 5. The NVCC has only one input signal line which is preferred for the implementation of VGAs.

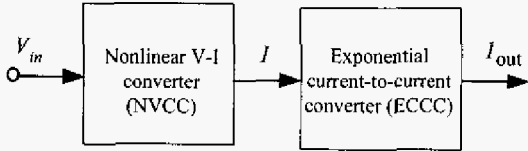


Fig. 4 A block diagram of the proposed EVIC

Neglecting the second order effects and assuming that all transistors are in the saturation region, the drain currents of transistor $M_{1,2}$ are given as:

$$I_1 = (1/2)(\mu_p C_{ox} W/L)(V_{in} - V_{DD} - V_{thp})^2 \quad (4)$$

$$I_2 = (1/2)(\mu_n C_{ox} W/L)(V_{in} - V_{SS} - V_{thn})^2 \quad (5)$$

The threshold voltages and transistor sizes of M_1 and M_2 in (4) and (5) are assumed to be identical ($V_{thn} = V_{thp} = V_{th}$). The currents I_1 and I_2 are depicted in Fig. 6 by the dash-dotted and dashed lines, respectively. If the input voltage, $V_{SS} + V_{thn} < V_{in} < V_{DD} - V_{thp}$, then $M_{1,2}$ in Fig. 5 are in the saturation region, from (4) and (5) the current $I = I_1 - I_2$ as shown in Fig. 4 and Fig. 6 is calculated as

$$I = I_1 - I_2 = M[2V_{in} - (V_{DD} + V_{SS} + 2V_{th})] \quad (6)$$

where $M = (1/2)(\mu C_{ox} W/L)(V_{SS} - V_{DD})$. It is obvious that the current I in (6) is a linear function of the input voltage V_{in} . If V_{in} decreases below $(V_{SS} + V_{thn})$ or V_{in} increases higher than $(V_{DD} - V_{thp})$, one of the transistors M_1 or M_2 approaches the triode region and then is cut-off, while the other is still in the saturation region. Consequently, the $I = (I_1 - I_2)$ is simplified as $I = I_1$ or $I = I_2$, which are nonlinear functions of V_{in} as given in (4) and (5) and shown in Fig. 6. As a result, the output current I of the NVCC is a nonlinear function of V_{in} , which can be used to implement the pre-distortion technique as discussed in the previous section.

A compact ECCC, shown in Fig. 5, adopts the current-squaring block from [10]. Assuming that all transistors of the ECCC are in the saturation region and neglecting the second order effects, the current I_{sq} of the current squaring block [10] as shown in Fig. 5 is given as:

$$I_{sq} = 2I_0 + (I + k_1 I_0)^2 / 8I_0 \quad (7)$$

where $I_0 = (1/2)(\mu_n C_{ox} W/L)(V_2 - 2V_{TH})^2$, and I_0 is also chosen to be the bias current of the ECCC as shown in Fig. 5. The I_{out} of the ECCC can then be calculated as

$$I_{out} = I_{sq} - k_2 I_0 = \frac{I_0}{4} \left[\frac{8(2 - k_2) + k_1^2}{2} + k_1 \frac{1}{I_0} I + \frac{1}{2I_0^2} I^2 \right] \quad (8)$$

where k_1 and k_2 are the current multiplication factors which are shown in Fig. 5. Note that, by letting $k_2 = (14 + k_1^2)/8$, (8) can be simplified as

$$I_{out} = \frac{I_0}{4} \left(1 + k_1 \frac{1}{I_0} I + \frac{1}{2I_0^2} I^2 \right) = (1/4a) (1 + k_1 a x + a^2 x^2 / 2) \quad (9)$$

where $a = 1/I_0$, $x = I$. It is obvious that (9) has the same form of expression as (3), therefore, the shifted-symmetric axis technique can be implemented by adjusting the value of k_1 . And, for $k_1 = 1$, (9) becomes the Taylor series approximation as in (2). The significance of the proposed ECCC is simplicity and, therefore, lower power dissipation.

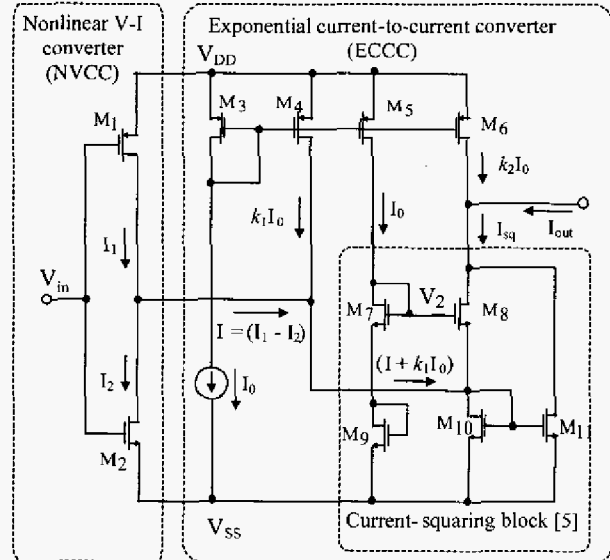


Fig. 5 Proposed exponential V-I converter

IV. MEASUREMENT RESULTS

The proposed EVIC was fabricated in 0.18 μ m CMOS technology with a supply voltage of 1.2V. The measured normalized-dB linear V-I characteristics of the proposed EVIC is depicted in Fig. 7, showing a 44dB range and about a 38dB-linear range with linearity error

of less than ± 1 dB. A very wide input range from 0 to 1.2V is achieved. Fig. 8 shows the die photograph of the EVIC, which is a very small size. The die area, excluding bondpads, is $170 \times 90 \mu\text{m}$. The total current consumption is less than 0.18mA.

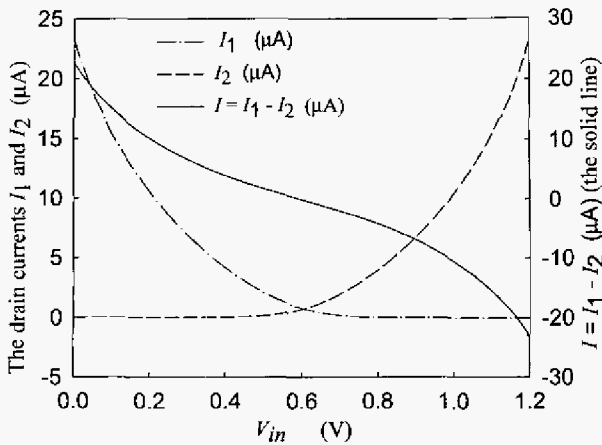


Fig. 6 I-V performance of the NVCC shown in Fig. 5

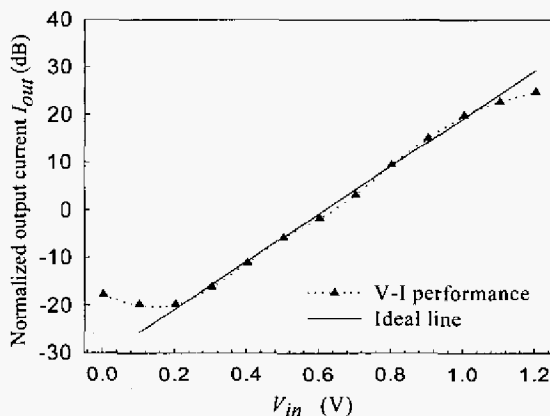


Fig. 7 The measured normalized-dB output current of the proposed EVIC shown in Fig. 5

V. CONCLUSION

This paper proposed a new idea to improve the dB-linear range of the Taylor series approximation method by combining the two previously reported techniques. The proposed idea improves the dB-linear output range of the EVIC drastically. Moreover, the input range of the EVIC is also extended. Compared to previous approaches, only one input control line, V_{in} , is used instead of differential control voltages as in [8]-[9]. Therefore, the implementation of this EVIC in the design of VGAs is simpler. The proposed NVCC and ECCC are rather compact compared to previous designs [5, 8, 9], resulting in very low-power consumption and small chip size. The measured normalized-dB V-I performance of the newly proposed EVIC shows a 44dB output current range and about a 38dB-linear range with a linearity error

of less than ± 1 dB over a large input voltage V_{in} from 0 to 1.2V. An improvement of about 26dB compared to traditional Taylor approximation is obtained. The average current consumption is less than 0.18mA from a 1.2V supply voltage. The chip area, excluding bondpads, is $170 \times 90 \mu\text{m}$.

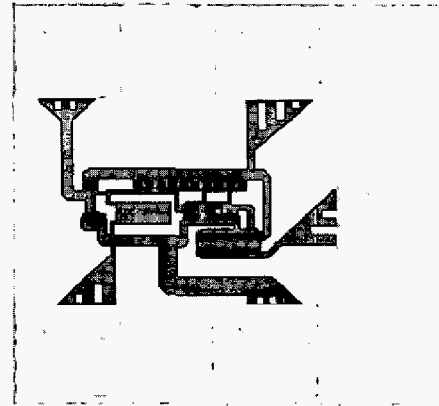


Fig. 8 Die photo of the EVIC shown in Fig. 5

Acknowledgements

This work is supported by the Digital Media Lab which is funded by the Ministry of Information and Communication, Korea.

References

- [1] H. Elwan, A. M. Soliman, and M. Ismail, "A. digitally controlled dB-linear CMOS variable gain amplifier," *Elect. Letters.*, vol. 35, no.20, pp. 1725-1727, 1999.
- [2] R. Harijani, "A Low-power CMOS VGA for 50 Mb/s Disk Drive Read Channels," *IEEE Trans. Circuits and Syst.* vol. 42, No. 6, pp. 370-376, June, 1995.
- [3] A. Motanemd, C. Hwang and M. Ismail, "CMOS exponential current-to-voltage converter," *Elect. Let.*, vol. 33, no. 12, pp. 998-1000, 5th June, 1997.
- [4] K. M. Abdelfattah and A. M. S., "Variable Gain Amplifier Based on a New Approximation Method to Realize the Exponential Function," *IEEE Trans. Circuits Syst.*, vol. 49, No. 9, Sep 2002.
- [5] Cheng-Chieh C. and S.-I. Liu, "Current-mode pseudo-exponential circuit with tunable input range", *IEE Electronics Letters*, vol. 36, no. 16, August 2000.
- [6] Cheng-Chieh C. and S.-I. Liu, "Pseudo-Exponential function for MOSFETs in saturation", *IEEE Transactions on Circuit and Systems-II*, vol. 47, no. 11, Nov 2000.
- [7] W. Liu, C. Chang, and S. Liu, "Realisation of Exponential V-I Converter using composite NMOS transistors," *Elect. Let.*, vol. 36, no. 1, pp. 8-10, 6th Jan, 2000.
- [8] Quoc-Hoang Duong and Sang-Gug Lee, "A low-voltage, low-power, and high db-linear all CMOS exponential function generator for AGC and VGA applications," *AMPC'03 Conference*, pp 409-412 November, 2003.
- [9] Quoc-Hoang Duong and Sang-Gug Lee, "A low-voltage, low-power, and high dB-linear CMOS exponential V-I converter," *AMPC'03 Conference*, pp413-416, Nov, 2003.
- [10] K. Bult and H. W., "A Class of Analog CMOS Circuits Based on the Square-Law Characteristic of an MOS Transistor in Saturation," *IEEE J. of S. State Cir.*, vol. sc-22, no. 3, June 1987.