29.6 A 1mW Current-Reuse CMOS Differential LC-VCO with Low Phase Noise

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An LC-VCO reduces power dissipation to half that of conventional topologies. The new LC-VCO replaces one of the NMOSFETs of a conventional differential LC-VCO with a PMOSFET. The operating principles and design guidelines of the new topology are reported. The 2GHz LC-VCO is implemented in 0.18μm CMOS technology and the measured phase noise is –103dBc/Hz at a 100KHz offset while dissipating 1mW from a 1.25V supply.

Figure 29.6.1 shows schematics of a conventional NMOS-based differential LC-VCO and the proposed current-reuse differential LC-VCO. In Fig. 29.6.1, the negative conductances are provided by the cross-connected pairs of transistors M1, M2 and M3, M4, to compensate the losses in the LC-tanks. The newly proposed VCO in Fig. 29.6.1 uses both NMOS and PMOS transistors in the cross-connected pair as a negative conductance generator. The series stacking of N- and P-MOSFETs allows the supply current to be reduced by half compared to that of the conventional LC-VCO while providing the same negative conductance. It is interesting that, in the proposed VCO, not only are balanced DC conditions maintained in the (N- and PMOS) transistors, as in the the small-signal schematics are equivalent with the exception of the additional resistor R_s.

To explain the operation of the proposed VCO for R_s = 0, Fig. 29.6.2 shows the schematic and corresponding large-signal equivalent circuits during each half period of operation (when the voltage at node X is high and low). In Figure 29.6.2, $C_x = C/2 + C_{px}$ and $C_y = C/2 + C_{py}$, where C_{px} and C_{py} represent the parasitic capacitances at nodes X and Y, respectively. As shown in the figure during the first half-period, the transistors M_1 and M_2 are on and the current flows from V_{DD} to ground through the tuning inductor L. During the second half-period, the transistors are off and the current flows in the opposite direction through the capacitors C_x and C_y. Note that in the conventional differential VCO, the cross-connected transistors switch alternately, while in the proposed VCO, the P- and N-MOSFETs switch at the same time. During the first half-period of oscillation, the P- and N-MOSFETs operate in triode mode near the peak of the voltage swing. In this case, the voltage swing is limited by the supply voltage. Therefore, the oscillator can operate in a voltage-supply-limited mode [1]. However, during the second half-period, the voltage swing across the inductor L is not limited and can lead to a voltage swing greater than the supply voltage.

Figure 29.6.3 shows the voltage swings at node X and Y of the circuit in Fig. 29.6.2 along with the dynamic current through the NMOSFET M_1. The voltage swing during the first half-period, where a large amount of dynamic current flows through transistor M_1, is smaller than that of the second half-period due to the voltage-limited mode of operation. The large drop in dynamic current during the first half-period leads to voltage-waveform distortion. Therefore, the proposed VCO shown in Fig. 29.6.2 is not suitable for generating a balanced differential voltage swing. The resistor R_s in Fig. 29.6.1 solves this problem. R_s controls the DC current as well as the peak dynamic current of the proposed VCO. Therefore, by properly selecting the resistor, the proposed VCO can operate in a current-limited mode, rather than the voltage-limited mode, since the voltage swing is a function of the peak dynamic current. In the current-limited mode, the voltage swing is symmetric during the two half periods. Figure 29.6.3 also shows the output voltage of the proposed VCO when it operates in the current-limited mode. The output voltage swings represent well-balanced behavior and the dynamic current through the resistor R_s also represents undistorted behavior.

Unlike a conventional VCO where the transistors switch alternately, this VCO does not have a common-source node because the transistors switch on and off at the same time. Therefore, the proposed VCO is inherently immune to the phase noise degradation caused by second-harmonic terms at the common-source node. In the conventional N- or P-MOSFET-based differential VCO, the phase noise can be degraded significantly by the noise near the second harmonic [2]. Utilization of PMOS transistors in the cross-connected pair can additionally help to reduce the phase noise due to lower flicker noise and hot carrier effects [3]. As seen in Fig. 29.6.1, the proposed VCO can offer a wide tuning range because the DC levels of the two outputs are approximately half of the supply voltage.

The conventional and newly proposed VCOs, shown in Fig. 29.6.1 are fabricated in a 0.18μm CMOS technology. The two VCOs are biased to draw 2.4 and 0.8mA from 1.25V supply, respectively. Fig. 29.6.4 shows measured phase noise for both the conventional VCO and the new VCO, which operate at 2.04 and 1.97GHz, respectively. The measured values for the conventional and proposed VCOs are –92 and –103dBc/Hz at 100KHz offset, respectively. Although a direct performance comparison may not be appropriate due to different bias levels and Qs for the performance of the proposed VCO is impressive, especially considering the extremely low DC power dissipation.

Figure 29.6.5 shows the measured differential output voltage and the frequency spectrum of the proposed VCO. The output waveforms show only 1.6° phase mismatch and the output power is –7dBm. Figure 29.6.6 presents the figure of merit (FOM) of the proposed VCO in comparison with previously reported low power VCOs, with FOM given by

$$FOM = L\{f_m\} + 10\log\left[\left(\frac{f_m}{f_o}\right)^2 P_{DC}\right] \quad (1)$$

where, L{f_m } is SSB phase noise measured at the offset frequency of f_m from the oscillation frequency of f_o, and P_{DC} represents DC power dissipation in mWs. As can be seen from Fig. 29.6.6, the proposed VCOs FOM of –189.3 is the best number that has been reported at the given amount of power dissipation (1mW). The proposed topology offers low power, small size (low cost), and high performance (low phase noise) solutions for the integrated differential LC-VCO. The micro-photographs of the fabricated VCOs are shown in Fig. 29.6.7.

References:

[1] A. Hajimiri et al., "Design Issues in CMOS Differential LC Oscillators," *IEEE J. Solid-State Circuits,* vol. 34, pp. 717-724, May, 1999.

[2] J. J. Rael and A. A. Abidi, "Physical Processes of Phase Noise in Differential LC Oscillator," *CICC*, pp. 569-572, 2000.

[3] C. Hung, K. K. O, "Fully Integrated 5.35-GHz CMOS VCOs and Prescalers," Trans. *MTT*, vol. 49, no. 1, Jan., 2001.

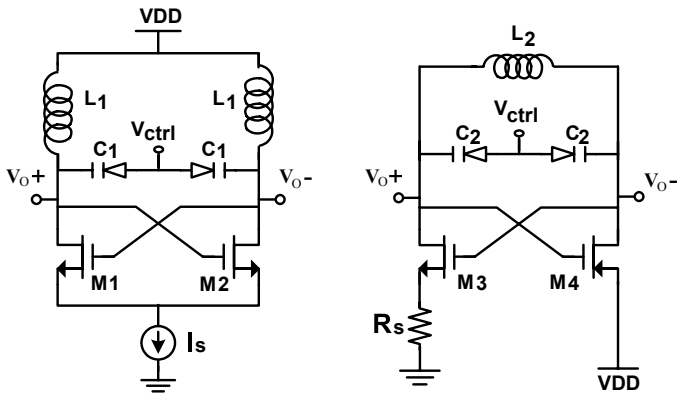

Figure 29.6.1: Differential LC-VCO: conventional and newly proposed.

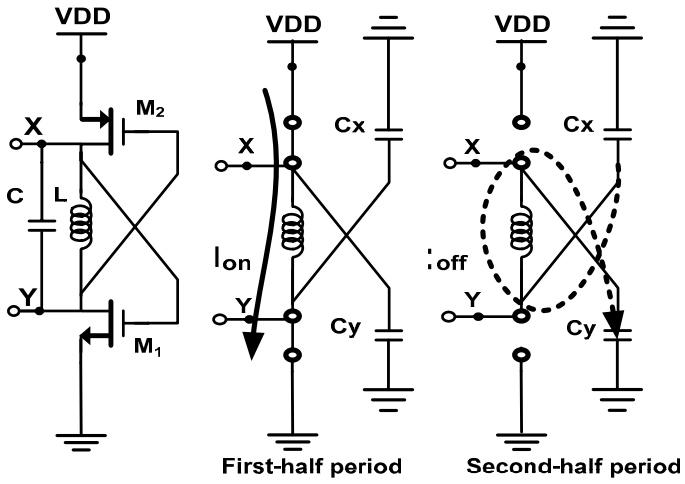

Figure 29.6.2: Proposed VCO operations with Rs = 0 during each half period.

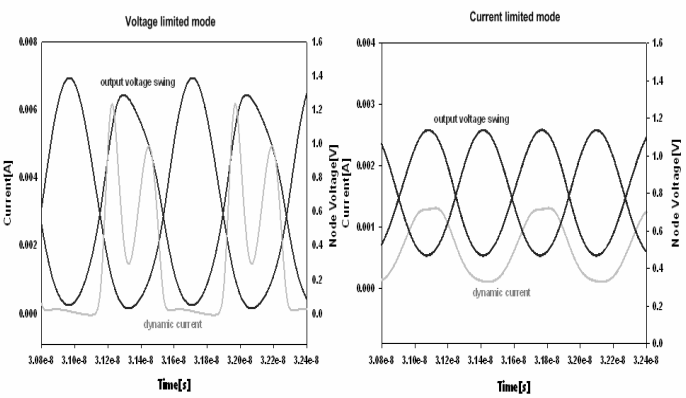

Figure 29.6.3: Differential output voltage and dynamic current waveforms: voltage limited mode (Rs = 0) and current limited mode (Rs ≠ 0).

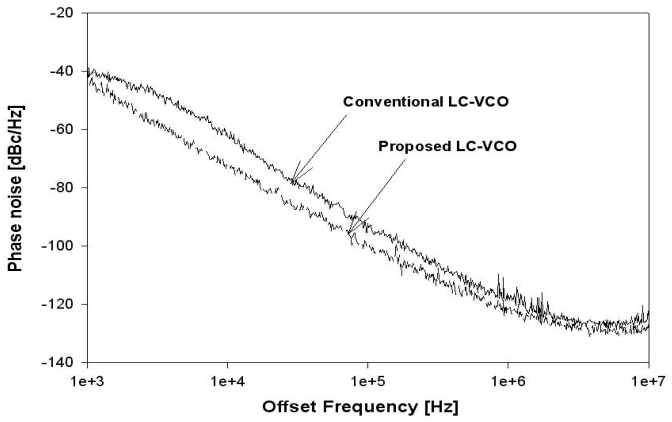

Figure 29.6.4: Measured phase noise of the conventional and proposed LC-VCOs.

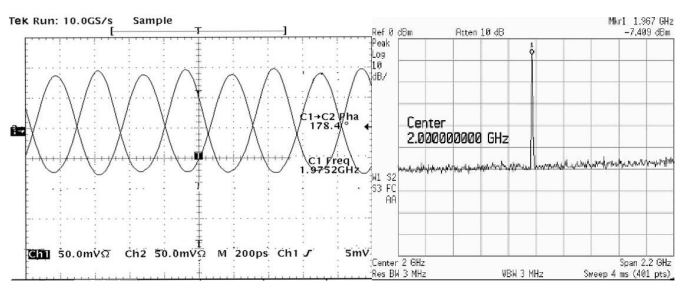

Figure 29.6.5: Measured differential voltage waveforms and output spectrum of the proposed LC-VCO.

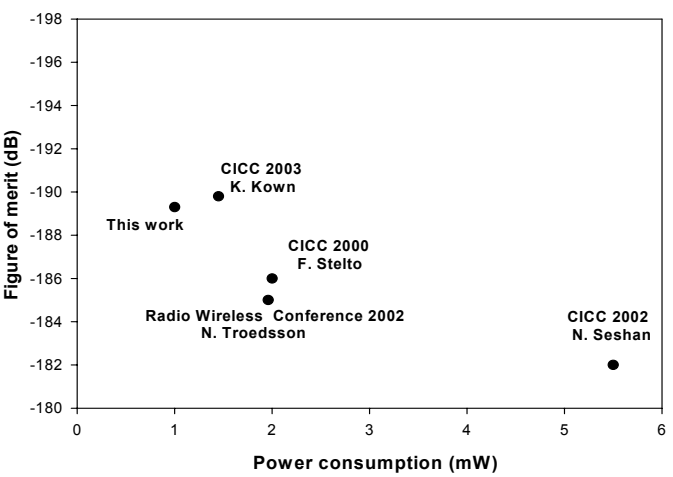

Figure 29.6.6: FOM of the proposed VCO in comparison with previously reported low-power VCOs.

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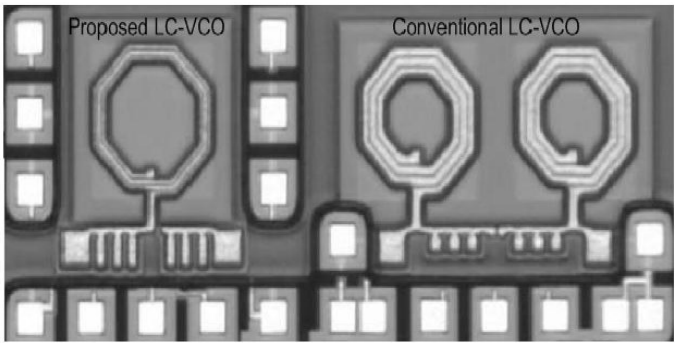

Figure 29.6.7: Micrograph of the proposed and conventional LC-VCOs.

