A 1.25V DIRECT-CONVERSION CMOS TRANSMITTER FRONT-END FOR 900MHz ZIGBEE APPLICATIONS

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ABSTRACT

This paper presents a very low power direct-conversion up-mixer and driver amplifier. The designed mixer is based on the typical Gilbert-cell, and the driver amplifier uses a folded cascode topology to improve the linearity under the low supply voltage. The fabricated up-mixer shows 5.5dB of conversion gain and 7.5dBm of output IP3, and the driver amplifier shows 17dB of power gain and 12dBm of output IP3. The up-mixer and driver amplifier consume 4.5mA and 2mA from 1.25V supply, respectively.

1. INTRODUCTION

In the last few years, the demand for low cost, low power, and small size wireless transceivers has been increasing with the extensive researches on transceiver architecture and RF circuit design utilizing a standard CMOS technology. The ZigBee standard is regarded as one of the most promising standards for low cost, low power wireless transceiver implementation [1]. In addition, the popularity of direct conversion architecture has been dramatically increased because of the possibility for one-chip transceiver solution [2], [3].

This paper describes the direct-conversion transmitter front-end for ZigBee applications, which includes a driver amplifier as well as up-mixer with a frequency doubler. The direct conversion transmitter is attractive for high level integration, but can suffer from the VCO frequency pulling because the RF frequency is equal to the LO frequency. A fully differential frequency doubler is utilized to eliminate VCO frequency pulling, which not only shows good differential outputs but also consumes very small amount of current. The driver amplifier is required to provide very good linearity. The low supply voltage, however, makes the driver amplifier difficult to achieve enough linearity. In this paper, we propose a folded cascode amplifier as one of the solutions to improve the linearity of the driver amplifier under the low supply voltage, 1.25V.

The proposed block diagram of the direct-conversion transmitter front-end is shown in Fig. 1. The external local oscillator provides a differential signal at 450MHz, and the frequency doubler converts them into 900MHz differential LO signals. The frequency doubled LO signals and IF signals are applied to the up-mixer and the RF output signal is applied to the driver amplifier.

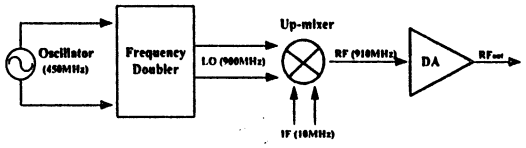

Fig. 1. Proposed Transmitter Front-End

2. TRANSMITTER FRONT-END CIRCUIT DESIGNS

A. Up-Mixer Design

The up-mixer consists of a double balanced mixer core and a LO frequency doubler. Fig. 2 shows the proposed frequency doubler, which is designed with a stacked push-push configuration using N- and P-MOS transistors to generate differential output.

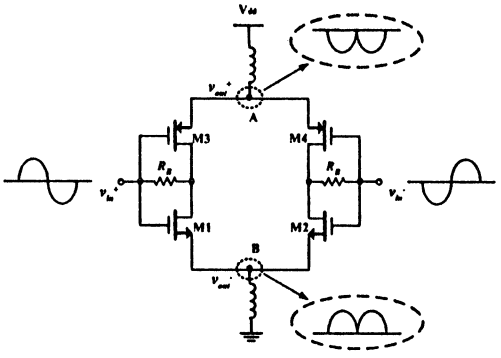

Fig. 2. Proposed LO Frequency Doubler

In Fig. 2, the large resistors R_B are included for the dc biasing which makes no additional dc bias necessary. The output loads at node A and B are implemented with inductors considering the low supply voltage of 1.25V. In Fig. 2, for the large differential input voltage v_{in}^{+} and v_{in}^{-}, the transistor pairs M_1—M_2 and M_3—M_4 operates as switch. As shown in Fig. 2, during the first half cycle of the input signal, the transistors M_1 and M_4 are turned on

and M_2 and M_3 are turned off. The outputs v_{out}^+ and v_{out}^- follow v_{in}^- and v_{in}^+, respectively, as M_1 and M_4 constitutes source follower. Similarly, during the second half cycle of the input signal, the outputs v_{out}^+ and v_{out}^- follow v_{in}^+ and v_{in}^-. As a result, the frequency of the overall output waveforms, v_{out}^+ and v_{out}^-, becomes two times that of the fundamental frequency as shown in Fig. 2. With increase in the frequency of operation, the output waveform of the proposed doubler shapes close to the sinusoidal wave. This is due to the limited cutoff frequency of the source follower transistors, yet it has no deteriorating effects on the frequency of interest. The difference in the transconductance of the N- and P-MOS transistors can lead to a mismatch in the amplitude of the two frequency-doubled output signals. This amplitude mismatch can be alleviated by optimizing the size of the constituting transistors and the inductances at node *A* and *B*.

By utilizing the proposed differential frequency doubler, a direct-conversion up-mixer has been designed as shown in Fig. 3. In Fig. 3, the mixer core is designed based on the Gilbert-cell, and the output load of the mixer is implemented using external LC network that converts differential RF output to a single-ended RF signal [5]. The single-ended mixer output helps to reduce the power dissipation of the overall transmitter as it allows single-ended driver amplifier. In Fig. 3, the output of the frequency doubler is applied directly to the up-mixer core without requiring buffer stages due to the low output impedance of the frequency doubler. The elimination of the buffer stages helps to achieve lower power dissipation.

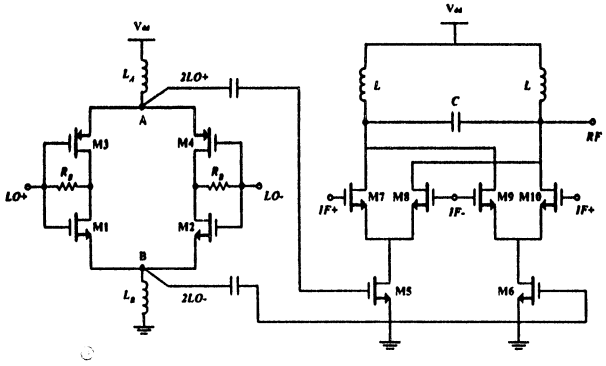

Fig. 3. Schematic of the Up-mixer

B. Driver Amplifier Design

In general, the cascode amplifier can provide high linearity, but it is not suitable for the low voltage low power applications due to the relatively large voltage headroom requirement. The proposed driver amplifier uses a folded cascode topology to achieve high linearity as well as low power consumption and enough power gain. Fig. 4 shows the proposed folded cascode driver amplifier that consists of NMOS and PMOS transistors. The folded cascode structure allows the more voltage headroom than the typical cascode amplifier, thus can provide the better linearity. The first stage is a common-source amplifier with inductive degeneration. The source degeneration L_s is used to match the real part of the input impedance to the output impedance of the up-mixer. And the combination of L_g and L_s are used to cancel out the reactance due to the parasitic capacitance C_{gs} of the input transistor M1 plus an additional MIM capacitor C_{mim}.

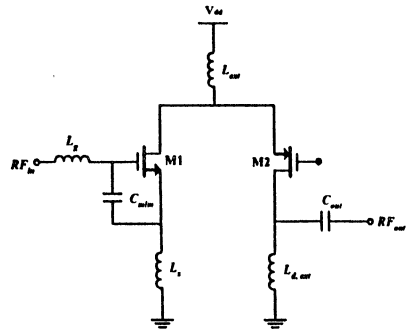

Fig. 4. Schematic of the Driver Amplifier

In Fig. 4, the size of the input transistor M1 is expected to be quite small to lower the current consumption, but the small transistor size can make the gate inductor L_g very large due to the decreased C_{gs} of M1. An MIM capacitor C_{mim} is inserted between the gate and the source of the input transistor M1 to reduce the burden of the gate inductor L_g. The input impedance is then given by

$$Z_{in} = s(L_g + L_s) + \frac{1}{s(C_{gs} + C_{mim})} + \left(\frac{g_m}{C_{gs} + C_{mim}}\right) L_s \qquad (1)$$

And if the resonance occurs at the frequency of interest, the input impedance becomes

$$Z_{in} = \left(\frac{g_m}{C_{gs} + C_{mim}}\right) L_s \quad at \ \varpi = \frac{1}{\sqrt{(L_g + L_s)(C_{gs} + C_{mim})}} \qquad (2)$$

As can be seen from Equation (2), the value of gate inductor L_g can be decreased for the same resonant frequency with the help of the inserted MIM capacitor.

The second stage of the driver amplifier is a common-gate amplifier implemented by PMOS. The second stage plays the more important role than the first stage in linearity. In this paper, two linearization approaches are applied to the second stage of the driver amplifier.

According to [6], the output IP3 of an amplifier can be expressed by

$$OIP3 = 10\log\left\{2\frac{(g_m)^3}{|g_m''|}\mathrm{Re}[Z_x]\right\} + C \qquad (3)$$

where g_m is the transconductance, g_m'' is the third-order intermodulation coefficient, and the $\mathrm{Re}[Z_x]$ is the real value of the output impedance of the amplifier. Two linearization techniques can be obtained from Equation (3). First, the linearity can be increased by raising the

gate overdrive voltage of the transistor because g_m increases but g_m'' decreases as the gate overdrive increases [7]. The folded cascode topology has an advantage in that sense, for it allows the more voltage headroom than the typical cascode amplifier, thus enabling the overdrive voltage of the second stage to have around 0.7V as a maximum under the 1.25V supply. Second, increasing the real value of the output impedance of the amplifier is helpful to increase the linearity. An external inductor is used as an output load to increase the $Re[Z_x]$ in the driver amplifier, which can improve the linearity by 3dB for the same amount of power dissipation [8].

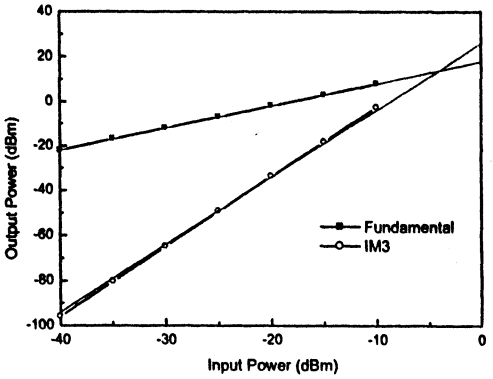

Fig. 6. Linearity of the Driver Amplifier

3. MEASUREMENT RESULTS

The direct conversion transmitter front-end has been fabricated with 0.25μm CMOS technology. In the measurement, 10MHz IF signal and 450MHz differential oscillator signals are applied to the up-mixer and 910MHz RF signal is applied to the driver amplifier. Fig. 5 and Fig. 6 show the linearity of the up-mixer including the frequency doubler and the driver amplifier. The up-mixer shows 7.5dBm of output IP3, 5.5dB of conversion gain, and 40dB rejection to the fundamental LO signal. The driver amplifier shows 12dBm of output IP3 and 17dB of power gain. The up-mixer and driver amplifier consume 4.5mA and 2mA from 1.25V supply, respectively.

4. CONCLUSION

A 900MHz 1.25V direct-conversion CMOS transmitter front-end is presented for ZigBee applications. A low power direct-conversion up-mixer has been designed by utilizing the fully differential frequency doubler. The designed up-mixer shows good conversion gain and linearity, and high rejection to the fundamental LO signal. A folded cascode topology is used for the driver amplifier. The designed driver amplifier shows good linearity while consuming very low current.

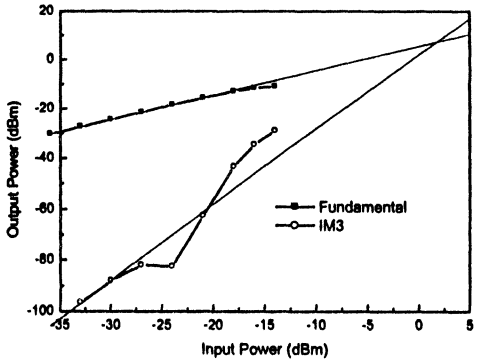

Fig. 5. Linearity of the Up-mixer

5. ACKNOWLEDGEMENT

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