A 5.2 GHz Image Rejection CMOS Low Noise Amplifier Using Notch Filter

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Abstract*-This paper represents a low noise, high gain image rejection low noise amplifier (IR-LNA) used in the superheterodyne architecture. The advantages and disadvantages of two different notch filters are analyzed and discussed. Based on that, the third order active notch filter is proposed. The IR-LNA is implemented by integrated the low noise, high gain LNA with the proposed third order active notch filter. The proposed IR-LNA is optimized for 5.25 GHz WLAN with IF frequency of 500 MHz applications. The measurement results show power gain of 20.5 dB, lower than 1.5 dB NF, and image rejection of 26 dB. Two-tone test results indicate –5 dBm and – 8 dBm of IIP3 for the case of using and not using the notch filter, respectively. The circuit operates at supply voltage of 3 V, and dissipates 4 mA in 0.18 μm CMOS technology.

Index terms — LNA, CMOS, Inter-Stage Resonance, Image Rejection, WLAN.

I. INTRODUCTION

The superheterodyne architecture is the most widely used architecture for the stage-of-the-art receivers in the modern handsets since this architecture is capable of providing high and stable performance in mobile communications [1], [2]. In the superheterodyne receivers, proper filtering of image signals is mandatory, and this filtering is done by external passive components such as SAW filters. These external filters are large and expensive but unavoi-dable in superheterodyne architectures. Consequently, they are the major impediment to increase the level of integration of wireless radio since they cannot be easily implemented monolithically [3]. To overcome the problems from those external filters, the image rejection mixer using the phase cancellation is developed [4], [5]. However, due to the gain and phase mismatch the image rejection ratios for 5 GHz band receivers generally lie within the range of 25-35 dB [2], which is still far from the 60-90dB of image rejection required by the different wireless standards. This implies that, off-chip image reject filters are still needed in conjunction with the above image-reject mixer structures to enhance the image rejection ratio. Therefore, in order to build fully monolithic receivers, on-chip image-reject filters or more advanced image-reject techniques must be developed.

Recently, a novel technique that helps to improve the image rejection ratio of the radio receiver systems is using an integrated notch filters [6]-[10]. In this technique, a notch located at the image frequency is used to reject image signals rather than band-pass filtering. By combining an on-chip image filter with an integrated image reject mixer, the image rejection ratio can be achieved as high as 79 dB [10].

In this paper, an image rejection low noise amplifier (IR-LNA) is implemented by integrated low noise, high gain LNA with the third order active notch filter. The proposed IR-LNA is optimized for 5.25 GHz with IF frequency of 500 MHz superheterodyne applica-tions. The measurement results show the power gain of 20.5 dB, lower than 1.5 dB NF, and image rejection of 26 dB. Two-tone test results show –5 dBm and –8 dB of IIP3 for the cases of using and not using the notch filter, respectively. The circuits dissipate the DC current of 4 mA under supply voltage of 3 V.

II. LNA DESIGN

A. The Third Order Active Notch Filter

An on-chip image rejection filter was first introduced in [6] by using the second order notch filter. The design of this active notch filter is based on a series resonator, whose resonant frequency is tuned to that of the image frequency. The advantage of that design is that the quality factor of the filter does not depend on the quality factor of the on-chip inductor. Therefore, very high quality factor of the filter can be easily achieved. However, such a notch filter can only control the response at the image frequency. The third order notch filter in [2] is used because of its ability of controlling the frequencies at both the image and the desired signals, separately. The disadvantage of this filter is the limitation of the quality factor of the filter due to low quality factor of on-chip inductor. To overcome those limitations, in this design, the third order cascode active notch filter is introduced as shown in Fig. 1. Another world, with the proposed third order notch filter the limitation of the low quality factor of on-chip inductor and the controllability at both image and wanted frequencies are solved.

As can be seen from Fig. 1, the input impedance, Z_{in}, of the proposed active filter can be expressed as

$$Z_{in} = \frac{1}{j\omega C_n} // Z_1 \qquad (1)$$

where

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$$Z_1 = j\omega L_f + \frac{1}{j\omega}\left(\frac{1}{C_{gs1}} + \frac{1}{C_f}\right) - \frac{g_{m1}}{\omega^2 C_{gs1} C_f} + R_{Lf} + r_{g1} \quad (2)$$

and C_{tt} is sum of the parasitic capacitance at node X and C_1

Note that the negative term in the right-hand side of Eq. (2) represents the negative resistance (proportional to g_{m1}) seen at the gate of transistor M_1. Thus, by adjusting g_{m1} by means of the bias current I_1, sufficient negative resistance can be generated to cancel R_{Lf} and r_{g1}. Therefore, the quality factor of this filter is not dominated by the quality factor of an on-chip inductor. Assuming that, all the parasitic components are cancelled the input impedance of the filter is now re-expressed as

$$Z_{in} = \frac{s^2 L_f C_{eq} + 1}{s\left(s^2 C_{tt} L_f C_{eq} + C_{tt} + C_{eq}\right)} \quad (3)$$

where

$$\frac{1}{C_{eq}} = \frac{1}{C_{gs1}} + \frac{1}{C_f} \quad (4)$$

From Eq. (3), the image and wanted signals are located at

$$f_{im} = \frac{1}{2\pi\sqrt{L_f C_{eq}}} \quad (5)$$

$$f_{wanted} = \frac{1}{2\pi\sqrt{\frac{1}{L_f}\left(\frac{1}{C_{tt}} + \frac{1}{C_{eq}}\right)}} \quad (6)$$

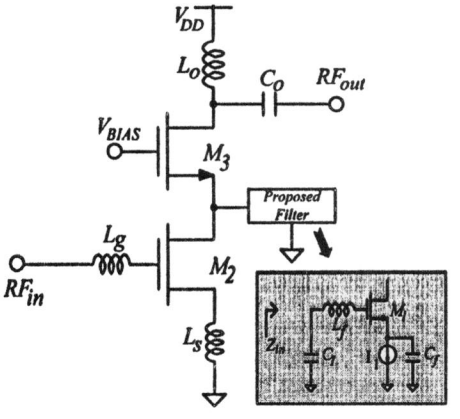

Fig. 1. The schematic of proposed notch filter

At the image frequency, the impedance Z_{in} looking into the filter is minimum such that the entire image signal will be extracted from the original path. While at the wanted frequency, the impedance Z_{in} is maximized such that the wanted signal is not extracted from the original path. The ability of image rejection depends on the difference of impedance between the filter and the original LNA at the image frequency. The larger the difference, the higher the image rejection is. To increase this difference a feedback connection from the drain of transistor to the input of the inductor has been added [6] (see Fig. 3). Now, the input impedance will be decreased by the factor of $1 + (g_m/\omega C_{gs1})$ such that the impedance difference becomes less dependent on the negative term in Eq. (2). This means that with a relatively low Q filter implemented in the signal path of a typical cascode LNA it is possible to realize a very deep notch with very high Q, provided the band-pass filter has large impedance difference.

Fig.2 shows the input impedance of the filter as function of frequency. This design is optimized for 5.25 GHz WLAN and an LO of 4.75-GHz for 500-MHz IF wireless receivers. Hence, the image signal is located at 4.25 GHz. As can be seen from Fig. 2, the impedance at 4.25 GHz is very low while the impedance at the wanted signal has a peak value. However, the impedance at the image signal has a narrow valley, so for correct image cancellation, the zero much be occurred at the correct frequency. On the other hand, the peak is a wider valley and the exact location of the pole is less important [2].

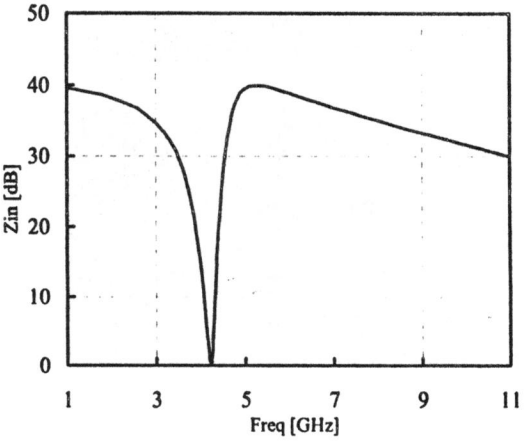

Fig. 2. Input Impedance of the filter at node X

B. The Image-Rejection LNA

In this design, IR-LNA is implemented by integrated low noise, high gain LNA with the proposed third order active notch filter. The complete schematic of IR-LNA is shown in Fig. 3. As can be seen in Fig. 3, the IR-LNA consists of two stages with current reused technique like in [11]. The first stage is a common source (CS) amplifier. In the first stage, an extra capacitor C_{ex} is used to obtain the power-constrained simultaneous noise and input matching. Another word, as described in detail in [12], by using C_{ex} the LNA can be design with any given amount of power dissipation while achieve the simultaneous noise and input matched. As can be seen in Fig. 3, the second stage has the cascode configuration, which consists of transistors M_2, M_3. The capacitor C_c is ac coupling, C_p the bypass capacitor. In this design, an inter-stages inductor L_c is included to resonate with input capacitor of second stage, C_{in2}, (approximately equal to gate-source capacitor of M_2) which can improve the

gain and NF of the amplifier [11]. Under the series resonant condition, the input impedance at node X is low such that the signal loss through substrate is avoided. Besides, the low impedance at node X also reduces voltage gain of the first stage so that the Miller effect on M_1 is reduced. In Fig. 3, the effect of the low and high quality factor of the inter-stage series inductor on the performances of LNA is analyzed in detail in [13]. The results show that the voltage gain and current gain are not affected by the quality factor of the inter-stage series inductor. Therefore, in this design, L_c is implemented by on-chip spiral inductor. A simple L-C network using an off-chip inductor L_o and an on-chip capacitor C_o are used to match the output of the LNA. The high-Q off-chip inductor L_o helps to improve the linearity of the LNA [14]. In Fig. 3, the LNA is designed based on 0.18 μm CMOS technology and it dissipates the total current of 4 mA from the supply voltage of 3 V.

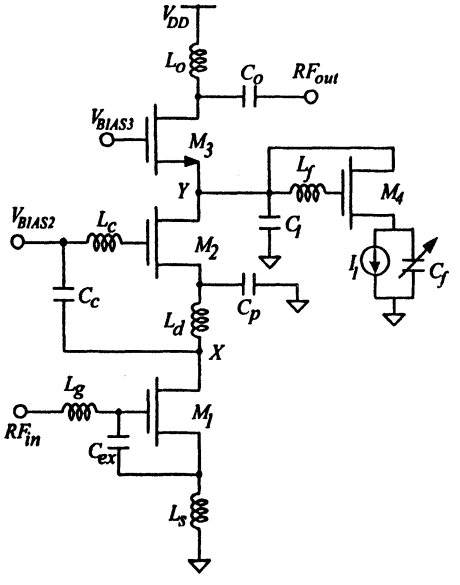

Fig. 3 The complete schematic of the IR-LNA

III. Experiment Results

In order to make sure the effect of the proposed notch filter on the performances of LNA, two versions of LNA are designed. Version 1 is a LNA without the proposed notch filter, and version 2 includes the proposed third order notch filter. The LNAs are fabricated based on 0.18 μm CMOS technology and optimized for 5-GHz WLAN applications. The matching inductors L_g and L_s are implemented by bonding wire. Fig. 4 shows the measured NF versus the frequency of LNAs. As can be seen from Fig. 4, the version 2 presents high NF near the image frequency that can be understood as the signal loss through the notch filter. However, as the frequency approaches 5.25 GHz, the NF reduces below that of the version 1. The improvement in NF at the wanted frequency is described as the resonant effect between L_f and the parasitic capacitor at node Y [2].

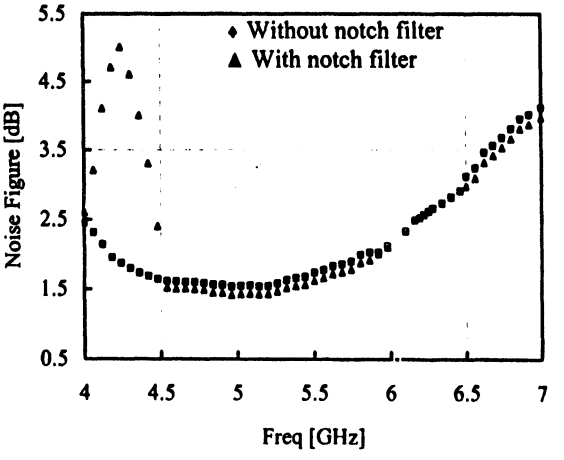

Fig. 4 NF of LNAs: with and without the notch filter

Fig. 5 shows the power gain of the two LNAs. As can be seen from Fig. 5, the image rejection filter provides approximately 26dB of overall image rejection. At 5.25 GHz, the power gain of the version 2 is higher than that for version 1. The improvements in NF and power gain at the operating frequency are 0.1 and 0.5 dB, respectively, which are explained as the resonant effect between L_f and the parasitic capacitor at node Y [2].

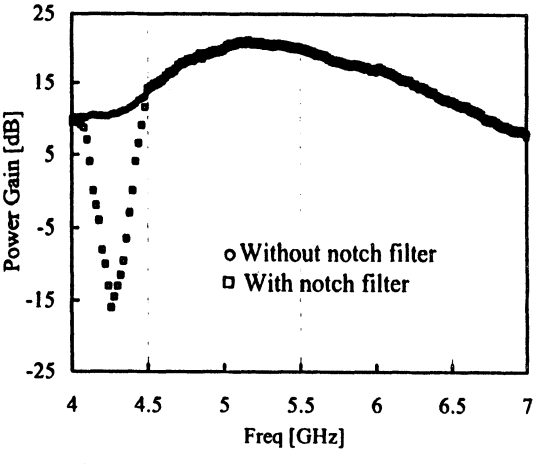

Fig. 5 Gain of LNAs: with and without the notch filter

A two-tone IP3 measurement was performed on the proposed LNA and results are shown in Fig. 6. The two tones were applied with equal power levels at 5.25 GHz and 5.245 GHz. The measurement indicates –5 dBm and –8dBm input-referred third order intercept point for the case of using and not using the notch filter. The effect of the linearity improvement is not clear at this point, however, this result is confirmed by measurement. The photographs

of two LNA versions are shown in Fig. 7.

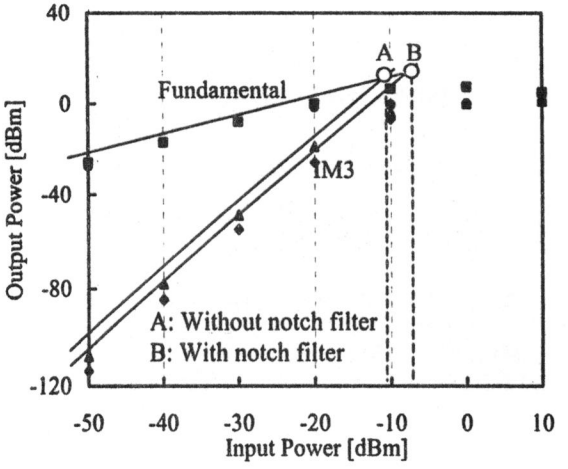

Fig. 6 IIP3 of LNAs: with and without the notch filter

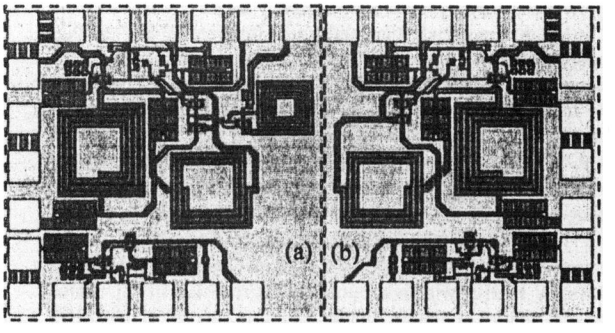

Fig. 7 Chip Microphotographs: (a) with notch filter, (b) without notch filter

IV. CONCLUSION

The image rejection signal is the main problem in the superheterodyne architecture. To eliminate using off-chip SAW filter, the on-chip image rejection techniques have been developed. Among them, the image rejection notch filter is the suitable for on-chip integrated image receiver. In this paper, the low noise, high gain and image rejection LNA is introduced. High gain without increasing the power dissipation is implemented by using two stages current reused technique with inter-stage resonate network. Low noise, low power dissipation LNA can be optimized by using the external capacitor, C_{ex}, in parallel with the intrinsic gate-source capacitor. Another word, by using C_{ex}, the power constrained simultaneous noise and gain matching can be achieved. The proposed image rejection LNA is implemented by integrated LNA with the third order active notch filter. Also, by using the proposed notch filter, the NF and power of LNA are improved. Besides, by using the third order notch filter, the linearity of the LNA can be improved. The improvement in linearity is confirmed by measuring even the reason is not clear at the moment. The proposed IR-LNA is implemented based on 0.18 μm CMOS technology. Measurements show 20.5 dB of power gain, lower than 1.5 dB of NF, and –5 dBm of IIP3, for the dc power supply of 4mA at 3V.

V. REFERENCES

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