A High Linearity, Efficient Bandwidth, and High Stability Transimpedance Amplifier

D.B. Yen Nguyen, Quan Le, Yong-Hun Oh, Huy-Binh Le, and Sang-Gug Lee, IEEE member
Radio Frequency Micro Ellectronics Laboratory
Information and Communications University
119 Munji-ro, Yuseong-gu, Daejeon 305-714, Korea
yenndb_vn@icu.ac.kr

***Abstract*—This paper presents a new high performance wideband CMOS transimpedance amplifier (TIA) for 2.5 Gbps optical transceiver. Our proposed TIA self-regulating adjusts the controllable inductive peeking load and feedback resistances whenever overload condition occurs. The proposed TIA design exhibits bandwidth enhancement, lower input referred noise, and higher amplifier stability. This TIA has 69dBΩ gain at 3dB bandwidth, 7.2 $pA/\sqrt{Hz}$ input referred noise and good performance of eye diagram. The TIA operates at the 3.3V supply voltage, and dissipates about 34mA for whole circuit. The simulation is accomplished with 1pF capacitance and 0.85A/W responsibility photodiode model.**

I. INTRODUCTION

The rapid development of optoelectronic integrated circuits (OEICs) prompts MOS technology to become a main technology in the high speed optical transceiver designs. In the typical optical receiver system (Figure1), Transimpedance Amplifier (TIA) amplifies the photodiode output then converts it into the voltage. Due to the critical role of TIA compared to adjacent blocks, there are a considerable number of TIA topologies designed to deal with inherent trade-offs in noise, bandwidth, stability, etc... Some techniques are introduced to achieve the high performance of one or more parameters, such as gain, speed, noise, and stability [1].

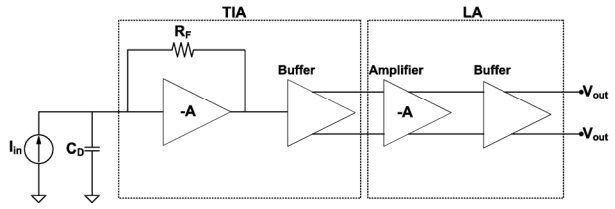

Figure 1. Optical Receiver

One of those techniques is using inductive peaking at the TIA load resistance. This technique allows enhancing about 40% of the TIA circuits' bandwidth. In the inductive peaking technique, the inductor is placed to resonate with load capacitance reducing the bandwidth. As the result, the bandwidth of circuit is improved. In [2], one idea using the on-chip inductor serried with the controllable load resistance has increased the bandwidth of 2.5 Gbps transceiver to 1.45GHz at 57dBΩ gain (Figure 2 (a)). The 3.3V supply voltage chip was fabricated based on 0.35μm CMOS technology. The result of [2] has confirmed that the obvious advantage of the inductive peaking technique is improving transimpedance bandwidth without sacrificing low-frequency gain. However, the stray capacitance that degrades bandwidth is directly proportional to the size of the inductor. The smaller the size of the inductor, the less bandwidth degradation. Besides, the effect of high frequency overshoot severely lessens amplifier stability.

Other technique called Automatic Gain Control (AGC) function is also used for high performance improvement. Inthe feedback TIAs, which are usually used in high speed

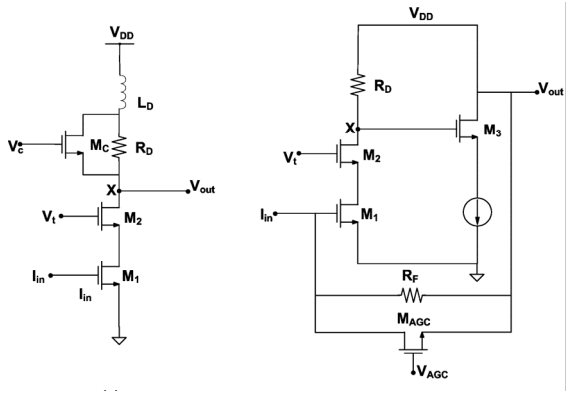

Figure 2. Illustration of TIA for (a) inductive peaking, (b) AGC function

0-7803-9197-7/05/$20.00 © 2005 IEEE.

and wideband optical receiver, the wide dynamic range is required to accommodate with various input currents. Even if the TIA has wide dynamic range, the large input currents. Even if the TIA has wide dynamic range, the large input currents will distort the output waveform, that is, the overload behavior appears. To avoid the overload condition, the ACG function is used to adjust the input current by controlling the value of feedback resistance (Figure 2(b)). The variation of the feedback resistance corresponds with the variation of the TIA gain. In general case, the AGC function is called the technique to satisfy the requirement of the amplifier stability. In [4], one design that utilizes AGC function effectively achieves the high circuit stability. That idea is applied for 1.25 Gbps TIA and claimed for bandwidth, noise, stability optimum concurrently. Obviously, there is a trade-off among bandwidth extension, lower noise and amplifier stability improvement. The higher feedback resistance,the smaller bandwidth, lower noise, the more unstable circuit.

This paper proposes a new feedback TIA design applying the inductive peaking technique for enhance bandwidth while using AGC function for improving circuit stability. The new design allows adjusting load and feedback resistance simultaneously to extend bandwidth without effect on amplifier stability. This TIA design achieves the incredible performance for 2.5 Gbps TIA, 69 dBΩ gain at 3dB bandwidth, 7.2 $pA/\sqrt{Hz}$ input referred noise and good performance of eye diagram. The proposed TIA is simulated based on 0.18 μm CMOS process in Cadence under 3.3V supply voltage, and dissipates DC current of 34mA.

II. THE ANALYSIS ON PROPOSED TIA TOPOLOGY

The proposed TIA given in Figure 3 consists of a cascode M1, M2; source followers M3, M4; a controllable load with inductive peaking that includes R_D, L_D, M_C and the feedback network that comprises R_F, M_{AGC}. Examining the overall transfer function of the proposed topology involves very complex calculation of fifth-order polynomial. Therefore, for the simplicity, the possible analysis is examining the effects of each part in the proposed TIA topology.

The core amplifier contains M1, M2 and can be considered as a single pole amplifier with the dominant pole at node X, a typical case of a cascode amplifier. From the detail calculation in [2], the bandwidth of TIA can be given as:

$$f_{-3dB} = \frac{1}{2\pi}\frac{\sqrt{2}A_0}{R_F C_{PD}} \qquad (1)$$

where, A_0 is the open loop gain, R_F is the feedback resistor and C_{PD} is capacitance of photodiode. The open loop gain, A_0, is affected directly from the impedance of the inductive peaking load. The inductor L_D is placed serried to the load of cascode M1, M2 and affects directly on an open loop gain to extend the bandwidth. The transistor M_C has a

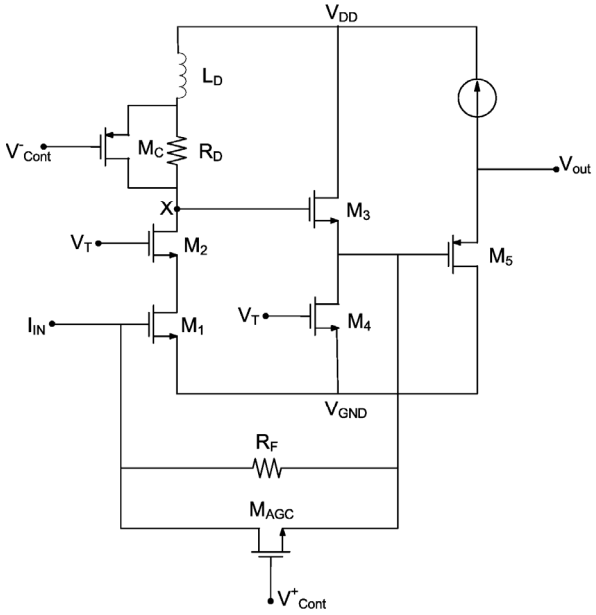

Figure 3. The core circuit of the proposed TIA

role as current bleeding to reduce the voltage drop across load resistor R_D. Hence, for the same available voltage drop, much larger load resistor can be used and the flat gain cannot be decreased. As follow [3] the impedance of inductive source degeneration, Z_D can be calculated:

$$Z_D = r_0 + j\omega L_D(1 + G_m r_0) \qquad (2)$$

Where r_0 is the load resistance of the transistor M_C, G_m is the overall transconductance of transistor M_C. Assume r_0 is large enough, $r_0 \approx R_D$ and $G_m R_D >> 1$ then Z_D can be rewritten as:

$$Z_D = R_D(1 + j\omega L_D G_m) \qquad (3)$$

Figure 4 shows the impedance of inductive source degeneration and its equivalent circuit.

For the voltage gain of cascade topology $|A_0| = g_m |Z_D|$,

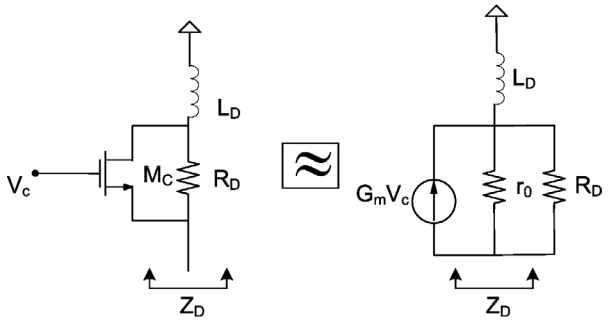

Figure 4. Inductive source degeneration and its equivalent circuit

from [3] we calculate the absolute value of Z_D hence, the 3dB bandwidth of TIA in (1) can be achieved and given as:

$$f_{-3dB} = \frac{1}{2\pi}\frac{\sqrt{2}g_m\sqrt{R_D^2\left(1+L_D{}^2G_m{}^2\right)}}{R_F C_{PD}} \qquad (4)$$

Hence, the f_{-3dB} can be expressed as the function of ratio of R_D to R_F while the variations of other parameters are neglected. Because of voltage headroom restriction in cascode topology, the load resistance should be designed for smaller value than that of the feedback resistance. When the value of R_F varies vastly, the value of R_D changes little in order to maintain the constraint ratio of R_D to R_F. The purpose to adjust the load resistance R_D and the feedback resistance R_F simultaneously is voidance the over-peaking pole during gain variation.

Furthermore, changing the values of the load resistance R_D and the feedback resistance R_F in the invariable ratio maintains the constant damping factor [2].

$$\zeta \cong \frac{1}{2}\sqrt{\frac{R_F C_{PD}\omega_O}{A_O+1}} \qquad (5)$$

Replace the absolute value of A_0, (5) can be rewritten as:

$$\zeta \cong \frac{1}{2}\sqrt{\frac{R_F C_{PD}\omega_O}{g_m\sqrt{R_D^2\left(1+L_D{}^2G_m{}^2\right)}+1}} \qquad (6)$$

Finally, the control of R_F and R_D values is not only to maintain the broad 3dB bandwidth achieved by inductive peaking but also to enhance the circuit stability by upholding the constant damping factor.

III. Simulation Result and Discussion

The simplified 2.5Gbps TIA topology shown in Figure 5 is preferred in CMOS design because it suppresses the over-peaking during gain degradation and maintains the broad 3dB bandwidth. This TIA topology comprised of three main parts: the core TIA, an AGC control signal, and a Serial to Differential (S2D) buffer. The core TIA, as described in part 2, receives the input current from photodiode, amplifies and converts to output voltage. The control signal from the AGC control signal part will switch transistors M_C, M_{AGC} on as soon as the output voltage exceeds a threshold voltage. The AGC control signal part has a comparator to compare the output voltage with the threshold voltage and accommodates to the control voltage signal. The last part of overall topology takes part in converting the serial output to the deferential outputs in order to match with 50 ohm input impedance of the next block, limiting amplifier (LA).

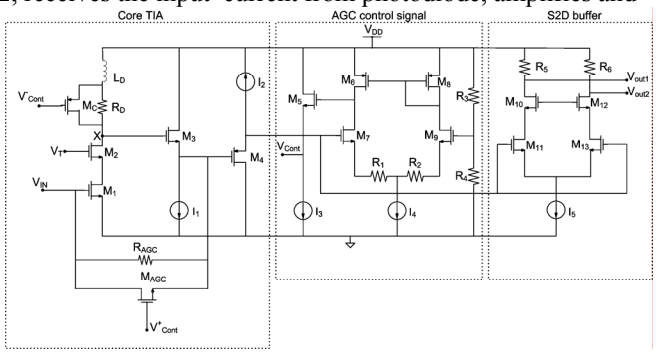

Figure 5. Simplified schematic of 2.5 Gbps TIA design

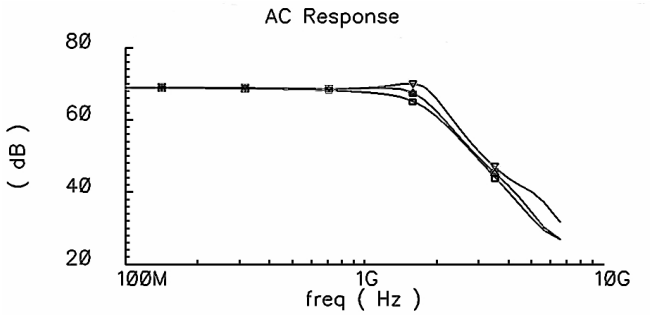

Figure 6. AC gain in different overload input signals 0μA; 200μA; 300μA

The proposed TIA in Figure 5 is simulated in a TSMC 0.18 μm CMOS process in Cadence. The simulation results are shown in Figure 6.

Figure 6 illustrates the gain and the bandwidth variation in the different overload input signals. In the normal condition that the input signals are 0μA, the 3dB bandwidth can get to 1.9GHz while the flat AC gain comes to 69dBΩ. When the overload input signal appears, the AGC adjusts the feedback to keep the required bandwidth; gain will be decreased. Due to the adaptability of controllable inductive peaking load, that is, load resistance is going down, the gain is going to increase. The result is gain is constant and the bandwidth goes down a little. This simulation result is suitable with (4) and (6) keeping the constants of 3dB bandwidth and damping factor. If the overload input signal is 300μA, the 3dB bandwidth is 1.7Gbps that is stillguarantee of the limitation for the operation of 2.5Gbps TIA. The 300μA current is the largest overload input current in this circuit. Figure 7 shows the result of input referred

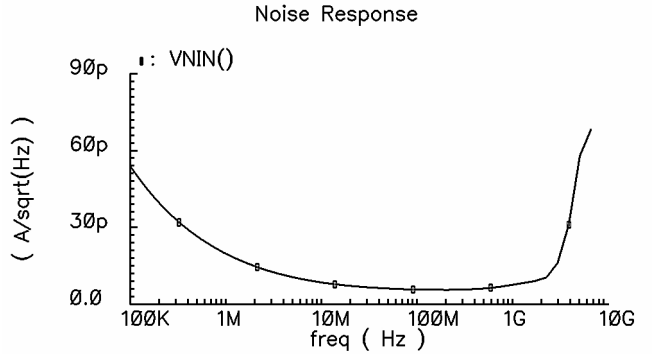

Figure 7. Input referred current noise of the proposed TIA

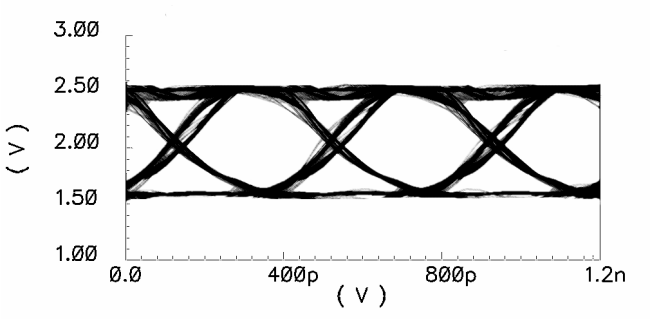

Figure 8. Eye diagram of the proposed TIA

current noise. The lowest noise value achieved at 150 MHz and the 9 $pA/\sqrt{Hz}$ is the noise value at 2GHz. The input referred current noise of this circuit, 7.2 $pA/\sqrt{Hz}$ is lower than that of many other previous works [5-7-9].

Figure 8 illustrates the eye diagram of the proposed TIA when the input signal is 1mA. The diagram has a good eye closure not only in horizontal but also in vertical axis.

To the best of our knowledge 2.5Gbps TIA using the controllable inductive peaking load and the AGC feedback resistance has been not reported so far particularly. As shown in Table 1 our design has better result in comparison to other previous works.

IV. CONCLUSION

The proposed TIA circuit in this paper has extremeadvantage compared to that of the previous works [2-5-6-7-8-9]. In this paper, the TIA design achieved 69dBΩ gain at the 3dB bandwidth, 7.2 $pA/\sqrt{Hz}$ input referred noise and good performance of eye diagram. The proposed TIA can control the value of the inductive peaking load and feedback resistances automatically to improve gain, bandwidth, and stability performances when the overload situation occurs.

REFERENCES

[1] Behzah Razavi, Design of integrated circuits for optical communications, textbook, Mc Graw Hill, 2003.

[2] Yong-Hun Oh, Sang Gug Lee, Inductance Enhancement technicque and its application to a Shunt-peaked 2.5 Gb/s transimpedance amplifier design, IEEE transactions on circuits and systems-II: express briefs, 2004.

[3] Mohan. S.S Hershenson, M.D.M., Boyd, S.P, Lee. T.H. *Bandwidth extension in CMOS with optimized on-chip inductors,* IEEE Journal of Solid-State Circuits, Volume: 35, Issue: 3, March 2000.

[4] Quan Le, Sang-GugLee, Yong-Hun Oh, Ho-Yong Kang, Tae-Hwan Yoo, Burst-mode receiver for 1.25 –Gb/s Ethernet PON with AGC and internally created reset signal, IEEE Journal of Solid-State Circuits, Volume: 39, Issue: 12, December 2004 .

[5] S.M. Rezaul Hasan, A high performance wide-band CMOS transimpedance amplifier for optical transceivers, proceedings of the 3rd IEEE international workshop on Sysytem on chip for real-time applications,2003.

[6] N. Haralabidis, S. Katsafouros, G. Halkias, A 1GHz CMOS transimpedance amplifier for chip to chip optical interconnects, IEEE international Symposium on circuits and systems (ISCAS 2000), May, 2000.

[7] Sung Min Park, Jeoseo Lee, Hoi Jun Yoo, *1-Gb/s 80-dB/spl Omega/ fully differential CMOS transimpedance amplifier in multichip on oxide technology for optical interconnects,* Journal of Solid-State Circuits, Volume: 39, Issue: 06, December 2004.

[8] Jaeseo Lee; Seong-Jun Song; Sung Min Park; Choong-Mo Nam, Young-Se Kwon, Hoi-Jun Yoo**,** *A multichip on oxide of 1 Gb/s 80 dB fully-differential CMOS transimpedance amplifier for optical interconnect applications,* Digest of Technical Papers in IEEE International (ISSCC) , Volume: 1 , Febuary, 2002.

[9] Kromer. C., Sialm. G., Morf. T., Schmatz. M.L., Ellinger. F., ErniD., Jackel. H., *A low-power 20-GHz 52-dB/spl Omega/ transimpedance amplifier in 80-nm CMOS*, Journal of Solid-State Circuits, Volume: 39, Issue: 06, December 2004.

[10] Makoto Nakamura, Yuhki Imai, Yohtaro Umeda, Jun Endo, Yuji Akatsu, 1.25 Gb/s burst-mode receiver ICs with quick response for PON systems, IEEE International Solid-State Circuits Conference (ISSCC), 2005.

TABLE I. COMPARISON TIA PERFORMANCE BETWEEN PUBLICATIONS AND THIS WORK

Design	3dB Bandwidth	Gain (dBΩ)	IN ($pA/\sqrt{Hz}$)	Topology	Technology	Year
[5]	3.5GHz	60	20	Inductive peaked feedback	0.5 µm CMOS	2003
[6]	1.8GHz	48	7.4	Standard feedback	0.8 µm CMOS	2000
[7]	670 MHz	80	54	Differential regulated cascade	0.25 µm CMOS	2004
[8]	310MHz	80		Fully differential	0.25 µm CMOS	2002
[2]	1.73GHz	68	3.3	Shunt peaked cascode	0.18 µm CMOS	2004
[9]	20GHz	52	50	Single-ended regular cascade	0.08 µm CMOS	2004
This work	**1.9GHz**	**69**	**7.2****	**Proposed**	**0.18 µm CMOS**	**2005**

**: for full-circuit TIA design.