Low Power High Linearity Driver Amplifier for 900 MHz Zigbee Applications

Le Viet Hoang, Nguyen Trung Kien, Sok-Kyun Han and Sang-Gug Lee
RFME Lab, Information and Communications University
119 Munjiro, Yuseong-gu, Daejeon, 305-741, Korea
Email: hoangle@icu.ac.kr

***Abstract*-This paper presents a low power high linearity driver amplifier for 900 MHz Zigbee applications based on 0.18 μm CMOS technology. In this work folded cascode amplifier is adopted to get more efficient power transmission. High gain and linearity are achieved by applying resonating load and gain boosting technique. Measurements show 11.5 dB gain, 3 dBm output P1dB while dissipating 1.8mA DC current from 1.8 V supply.**

I. INTRODUCTION

In the last few year, the demand for low cost, low power and small size wireless transceivers has been increased significantly with extensive researches on transceiver architectures and RF circuit design techniques utilizing standard CMOS technology [1], [2]. With the introduction of IEEE 802.15.4 Zigbee standard [3], these demands tend to dominate the transceiver developments.

For low power application driver amplifier which is the last block in the transmitter chain and dominates the power transmission performance of transmitter, should provide high output power while not consume much dc current. There are several works on low power transmitter that have been reported in literature [4], [5] and [6]. However, for example, in [6], Molnar introduced low power transceiver for sensor network applications. In that work, the power consumption is quite low but the linearity is rather poor. With the motivation of low power high linearity transmitter to fulfill the demand of new technology trends, this paper presents a low power high linearity driver amplifier for 900 MHz Zigbee applications based on 0.18μm CMOS technology. The simulated results show 13 dB power gain, 5 dBm output P-1dB and -19 dB the output return loss while dissipating 0.8 mA from 1.8 V supply.

II. CIRCUIT DESIGNS

From a PAPR (defined as the ratio of the peak envelope power to the average power of the transmit signal) simulation with rolloff factor of 1, the required peak-to-average power ratio is about 2 dB. Assuming the nominal transmit output power of 0 dBm, 2 dB PAPR means that the transmitter should be capable of transmitting up to 2 dBm. Therefore, the output 1 dB compression point of the transmitter output state should be over 2 dBm, and the output third-order intermodulation products, OIP3, should be over 12 dBm.

Considering the required radio specifications and with the key point of high gain, low power consumption and high linearity, the solution we are presenting here is folded cascode driver amplifier shown in Fig. 3. In general, the conventional cascode amplifier can provide good linearity. However stacking two transistors limits the output voltage swing at the output. Therefore, to maximize output voltage swing, the folded-cascode structure is adopted.

In this folded cascode amplifier shown in Fig. 1, the current source is replaced by an inductor L_2 such that voltage swing at the output is maximized. In order to introduce high impedance to ac ground at node X then prevents the signal loss into the silicon substrate to get the highest achievable gain [9], high inductance, L_2 is needed, up to 50 nH which could be impossible since its resonated frequency is below our interested frequency. In order to overcome this problem an additional capacitor C_1 is added at node X which help to reduce the value of L_2. As can be seen in Fig. 1, an additional capacitors C_{ex} is added to gate-to-source of input transistors to keep the input signal linear because otherwise the intrinsic gate source capacitance which is essentially a bias dependent varactor may lead to significant distortion at high input power levels [10]. To save the DC current the input transistor is bias at very low gate to source voltage. At this low bias voltage transistor drops into class A-B operation. When high power signal is applied, DC drain current is then increased leading to power gain is boosted. As a result, output power and therefore output 1dB compression point is increased.

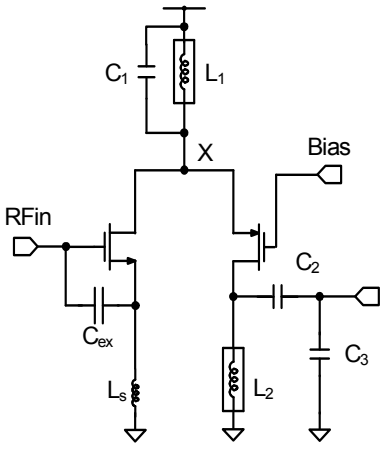

Figure 1. Driver amplifier.

From simulation we have seen that by applying the gain booting technique the output P-1dB compression point is improved significantly. In Fig. 1, an inductive degeneration L_s which is implemented as wire-bonding, help to improve linearity by lowering the gain through negative feedback. At the drain output, inductor L_3 plays as the load as well as output matching with capacitor C_2 and C_3. In this design, two inductors L_1 and L_2 are made off-chip to get high linearity and gain since off-chip inductor has much higher quality factor than on-chip inductor [11].

III. SIMULATION RESULTS

Driver amplifier is designed in TSMC 0.18μm CMOS technology in Cadence. Fig. 2 shows the simulated S-parameters, S_{11}, S_{22} and S_{21}, of the proposed DA. As can be seen in Fig. 2, DA exhibits 13 dB gain at working frequency (902-928 MHz) and good input and output return losses. Fig. 3 shows the simulated output P-1dB of the DA which is 4.8 dBm. The obtained results satisfy the required specification of IEEE 802.15.4 standard. Fig. 4 shows the layout of the DA chip with the chip's size of 0.4 mm^2 which is now under fabricating process and the measured results can be presented at the conference. Table.I summarizes the simulated results of the DA.

TABLE I
SUMMARY OF THE SIMULATION OF DRIVER AMPLIFIER

Parameter	Simulation values
Opearating frequency [MHz]	902-928
S11 [dB]	-16
S22 [dB]	-19
S21 [dB]	13
Output P1 dB [dBm]	5
Supply voltage [V]	1.8
Power consumption [mW]	1.4
Technology [μm]	CMOS 0.18

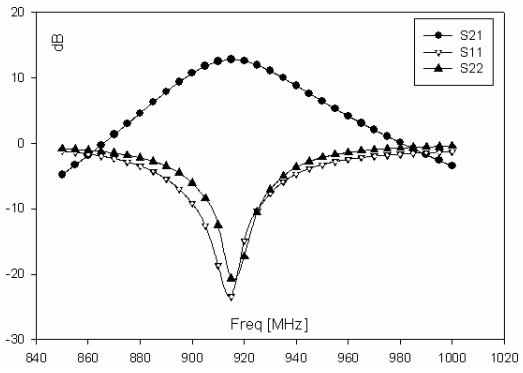

Figure 2. Simulated S-parameters of DA.

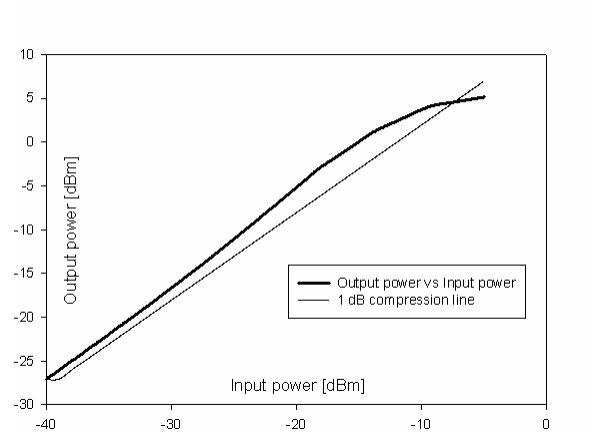

Figure 3. Simulated output P-1 dB of the DA

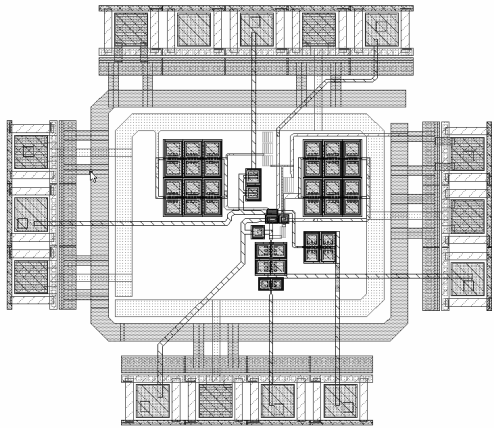

Figure 4. Driver amplifier layout

IV. CONCLUSION

A 900 MHz CMOS driver amplifier is presented for IEEE 802.15.4 ZigBee application. To get high output power and high linearity under low power consumption, the gain boosting technique is applied. In addition, an added capacitor at gate-to-source input transistor linearizes the strong input signal therefore improve the linearity. Simulated driver amplifier shows 13 dB of gain and 5 dBm of output 1 dB compression point at working frequency, current consumption is 0.8 mA from 1.8 V supply.

ACKNOWLEDGMENT

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