PREDICTIVE MODELING OF THERMAL EFFECTS IN BJTS

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Abstract: The effects of self-heating on BJT behavior are demonstrated through measurement and simulation. Most affected are the small-signal parameters Y_{22} and Y_{12}. A frequency-domain solution to the heat-flow equation is presented which applies to any rectangular emitter geometry. This model, although simple enough for CAD, predicts thermal spreading impedance with good accuracy for a wide range of frequencies.

Introduction

It has long been known [1, 2] that collector-to-emitter thermal feedback can profoundly affect bipolar transistor performance. This effect is becoming more important as current densities and thermal spreading impedances rise with technology scaling. Previously developed thermal-impedance models were based in the time domain [3]. It was shown in [4] that neglecting thermal effects caused errors up to 4% in the predicted delay of a simple BJT logic gate. This work will show that local heating causes much larger errors in BJT small-signal parameters. A new model is derived that predicts thermal corrections to BJT small-signal parameters based on a solution of the heat-flow equation in the frequency domain. The model is applicable in principle to any emitter geometry. Polynomial approximations provide simplified expressions for rectangular emitters. These expressions are simple enough for CAD.

Model for thermal spreading resistance

Figure 1a shows typical measurements of the emitter temperature response to a negative step in collector power. The measurement set-up is shown in Fig. 1b. Electrical transients dominate the earliest time scale of the measurement, so the temperature is plotted only for $t > 0.4\ \mu s$. This presumably hides a short delay before the emitter temperature begins to respond. The emitter temperature continues to fall for several microseconds. After 100 μs the local heating transient is complete and the temperature is constant. Then, about 10 ms after the power step, the whole package begins to cool; this transient continues for many minutes. The cooling of the package is controlled by the package thermal impedance, which causes a coupling of all of the devices on the chip. Figure 2a shows the effect of a negative power step in one transistor's power on the emitter temperature of a nearby transistor. Only the longer time-scale transient, controlled by the package thermal impedance, is visible. Consistent with the model of [3], thermal spreading impedance falls off strongly with distance, so that for modest powers, even adjacent devices are thermally decoupled over the shorter time scale. This paper is concerned primarily with local heating effects.

If a unit impulse of heat occurs instantaneously at some point in a uniform medium, the temperature rise at a point a distance r away is given by [5]

$$T(r,t) = \frac{1}{8\rho c(\pi\kappa t)^{3/2}}\exp\left(-r^2/4\kappa t\right) \qquad (1)$$

where ρ is the density, c is the specific heat, and κ is thermal diffusivity. An identical image source can be added to create an adiabatic surface at the plane equidistant between the sources. In their time-domain derivation, Joy and Schlig [3] integrated Eqn. 1 over the volume of the collector space-charge region (SCR) and its image. The result is a closed-form expression for the impulse response at any point in the semiconductor. The time integral of this expression gives the response to a unit step in the collector power. The integral is complicated and is not available in closed form. The step response at $t = \infty$ gives the thermal resistance R_{th}, defined as the total temperature rise caused by a unit step in the collector power.

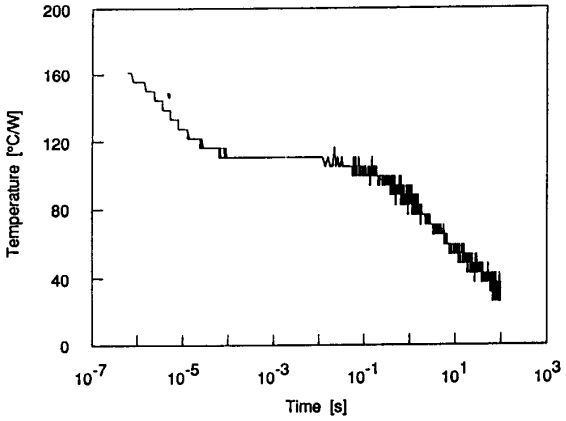


Fig. 1a. Measured response to negative collector-power step. Results of several measurements are superimposed.

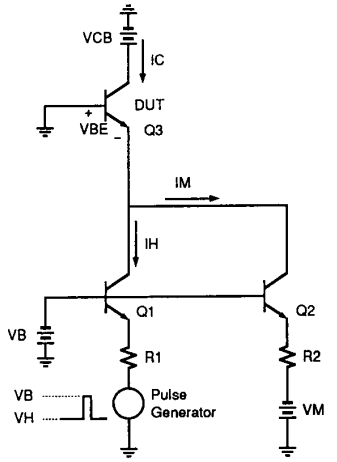


Fig. 1b. Experimental setup for self-heating. Heating current I_H is turned off during brief intervals, during which $V_{BE}(t)$ is measured for small fixed current I_M.

A frequency-domain model can be derived by first taking the Laplace transform of Eqn. 1, yielding

$$Z_{th}(r,s) = \frac{1}{4\pi Kr}\exp\left(-r\sqrt{\frac{s}{\kappa}}\right) \qquad (2)$$

where K is thermal conductivity. For $s = 0$, this equation gives R_{th} for the point source. R_{th} can be integrated over the collector

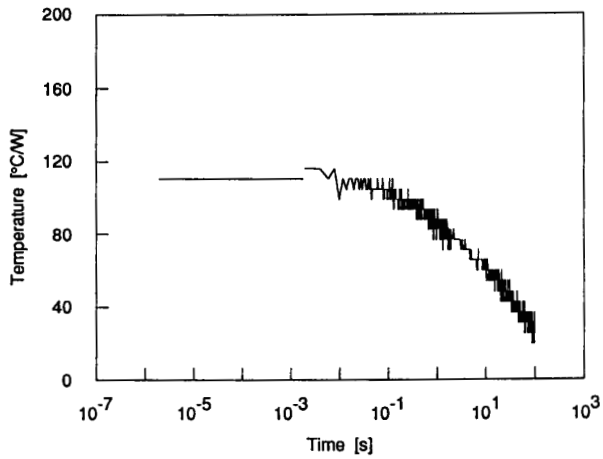


Fig. 2a. Measured response of transistor heated by nearby transistor.

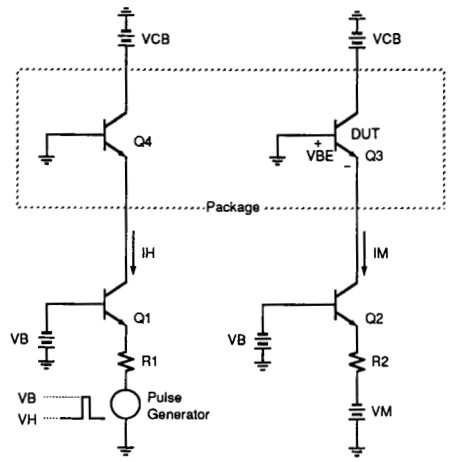


Fig. 2b. Setup for measuring thermal response of transistor heated by nearby transistor.

SCR and its image to yield the thermal resistance at any point r′ = (x′,y′,z′) for arbitrary geometry. In rectangular coordinates

$$R_{th}(W,L,H,D,r') = \frac{1}{4\pi K}\int_0^W\int_0^L\left[\int_D^{D+H}\frac{dxdydz}{r} + \int_{-D}^{-(D+H)}\frac{dxdydz}{r}\right] \quad (3)$$

where $r = \sqrt{(x-x')^2+(y-y')^2+(z-z')^2}$, W and L are the width and length of the emitter, D is the depth of the base-collector junction, and H is the SCR width. This integral is not solvable in closed form, so least-squares fitting was used to generate the following approximation to Eqn. 3.

$$f_1(d,h) = (0.058\,d + 0.14)\,h + 0.34\,d + 0.28 \quad (4a)$$

$$f_2(a) = 0.98 + 0.043\,a - (6.9\cdot10^{-4})\,a^2 + (3.9\cdot10^{-6})\,a^3 \quad (4b)$$

$$r_{eff} = 2\sqrt{WL}\,f_1 f_2 \quad (4c)$$

$$R_{th} = 1/2\pi K r_{eff} \quad (4d)$$

where $d = D/\sqrt{WL}$, $h = H/\sqrt{WL}$, and $a = W/L$. The approximation agrees with numerical solution of Eqn. 3 to within 5% for all reasonable geometries. Figures 3 and 4 show how f_1 and f_2 vary with device geometry. In this approximation, r′ is taken as the point at the surface above a corner of the emitter. Up to eight evaluations of the approximating functions, with adjusted values for d, h, and a, are needed to find R_{th} for an arbitrary point in the emitter. Figure 5 is a contour plot of predicted R_{th} variation with position. Good fits to measured variations of output resistance with current are obtained when r′ is taken at the surface at the corner of the emitter. This requires only a single evaluation of Eqn. 4.

Small-signal circuit model

Mueller [6] showed that BJT common-emitter y-parameters can be corrected for thermal feedback using

$$Y_{mn} = \frac{Y_{mnE} + D_m Z_{th} I_m I_n}{1 - D_m Z_{th} P} \quad (5)$$

where m or n = 1 for the base or 2 for the collector, Y_{mnE} is the uncorrected electrical Y parameter, Z_{th} is the thermal impedance, and P is the dissipated power. D_2 is the fractional temperature coefficient of the collector current, (typically about 7 %/K) and D_1 is that of the base current, equal to D_2 - D_β, where D_β is the

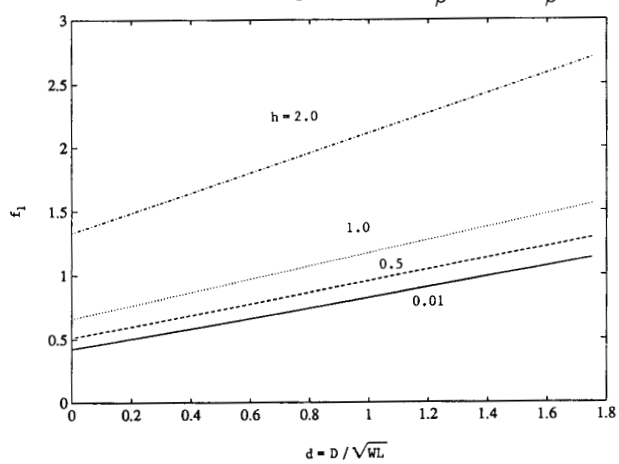


Fig. 3. Variation of function $f_1(d, h)$ with $d = D/\sqrt{WL}$, with $h = H/\sqrt{WL}$ as a parameter.

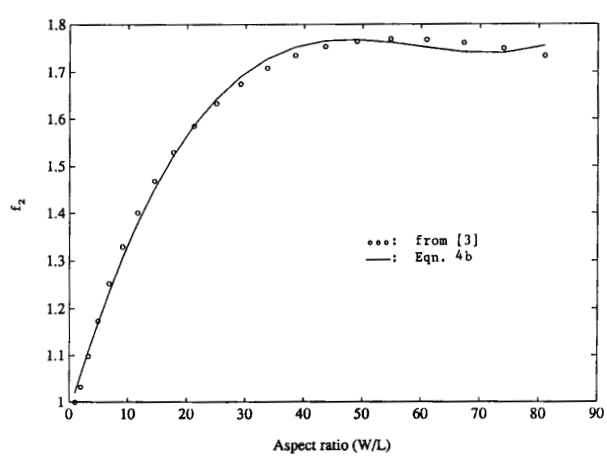


Fig. 4. Variation of function $f_2(a)$ with aspect ratio a = W/L.

fractional temperature coefficient of β, (typically around 0.7 %/K). Eqn. 5 can be used with $Z_{th} = R_{th}$ to thermally correct the DC small-signal parameters g_{mn}.

Figure 6 shows typical measured and simulated values for the normalized output resistance $V_A = I_C/g_{22} - V_{CE}$ of a silicon BJT with 23 x 23 $(\mu m)^2$ emitter, collector junction depth of 3.0 μm and epi doping of 10^{15} /cm^3. The value for H in Eqn. 4 was 2.8 μm, calculated assuming a step junction, which led to R_{th} = 70 K/W. The simulation used $g_{22E} = I_C/V_{AE}$, where V_{AE} = 350 V is the electrical Early voltage, measured at low currents. The data were corrected to account for package thermal resistance of 110 K/W, measured using the plateau region shown in Fig. 1. Fitting measured output resistance variations to Eqn. 5 provides a useful way to extract R_{th}. Differences between predicted and measured R_{th} values are typically < 10% for emitter areas > 100 $(\mu m)^2$. For smaller geometry (< 16 $(\mu m)^2$) emitters, differences up to 40% have been noted; these may represent errors in the specification of the device geometry.

The other DC small-signal parameter which is strongly affected by thermal feedback is g_{12}. Electrical models predict only a small negative value for this parameter, caused by Early-effect modulation of recombination in the quasi-neutral base. This effect is normally neglected. Eqn. 5 predicts a substantial positive value for g_{12} approaching g_{22}/β with increasing I_C. This can have a major effect on circuit performance, as the input and output impedances become strongly dependent on the loading at the opposite port. Note that Eqn. 5 shows that errors in small-signal parameters due to neglecting thermal feedback can occur without large DC power dissipation.

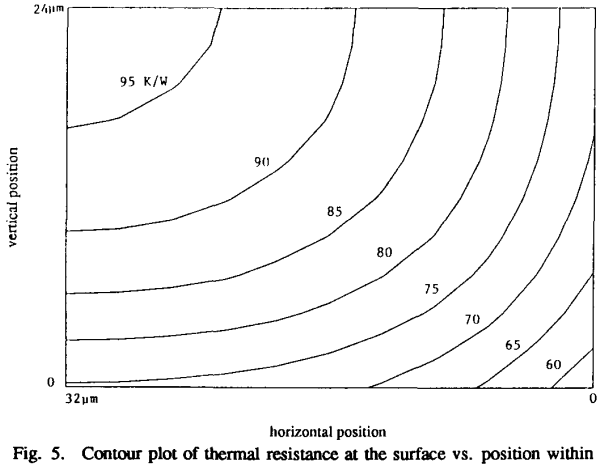


Fig. 5. Contour plot of thermal resistance at the surface vs. position within emitter for a transistor with W = 32 μm, L = 24 μm, H = 4 μm, D = 3 μm. Only one quadrant is shown and the center of the emitter is at the upper left.

AC Modeling

Equation 2 can be used to model thermal spreading impedance above DC if the r_{eff} from Eqn. 4 is substituted for r in Eqn. 2. The results are compared to the inverse Fourier transform of Joy & Schlig's predicted impulse response in Fig. 7. For this case (the same device as in Figs. 1 and 6) the magnitudes differ by less than 6% for frequencies up to f_{pk} = 350 kHz, defined as $1/(2\pi t_{pk})$, where $t_{pk} = r_{eff}^2/(6K) = 0.45$ μs is the time at which the impulse response in Eqn. 1 reaches a maximum. At this frequency $|Z_{th}|$ has dropped to 18% of R_{th}.

The phase response is not as accurate, differing by more than 30 degrees for frequencies greater than f_{pk}. These phase errors are easily understood – the model represents the transistor as a point-source collector and a point emitter, separated by an r_{eff} which is inevitably greater than the base width. Thus the model overestimates the initial delay. The authors are presently seeking simple ways to improve the phase modeling. However, since they coincide with decreasing $|Z_{th}|$, these phase errors may be tolerable in many applications.

SPICE Implementation

The model described above provides a simple and practical way to improve the accuracy of BJT circuit simulation. At this writing the small-signal model has been implemented in SPICE. Later the modeling will be extended to include DC and transient analyses. The implementation allows two modeling approaches. In the first (predictive) approach the user supplies for each model the parameters W, L, and D, plus the epitaxial-layer doping, which is used to determine the space-charge region width, H. The other modeling approach is empirical: for each model the user supplies values for R_{th} and a thermal capacitance C_{th}, which are used as constant real and imaginary parts for Z_{th}. Alternatively the user can supply R_{th} alone. In that case, Eqn. 4d is solved for r_{eff}, which is used in Eqn. 2 to compute Z_{th}. Typical SPICE results using the

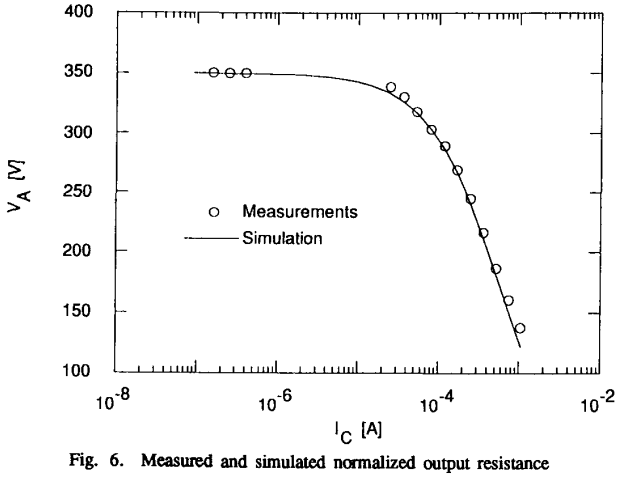


Fig. 6. Measured and simulated normalized output resistance V_A I_C/g_{22} - V_{CE}. Simulations are based on Eqns. 4 and 5.

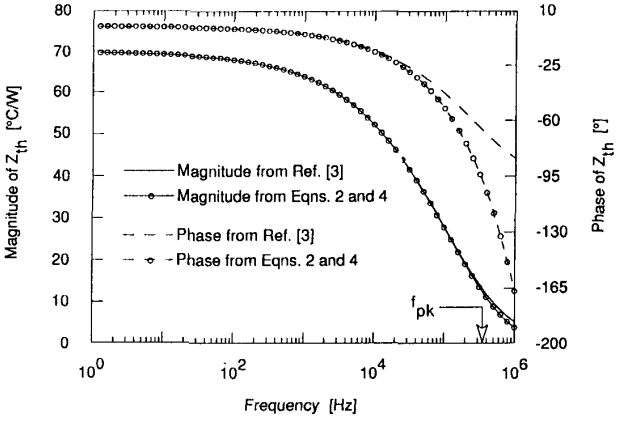
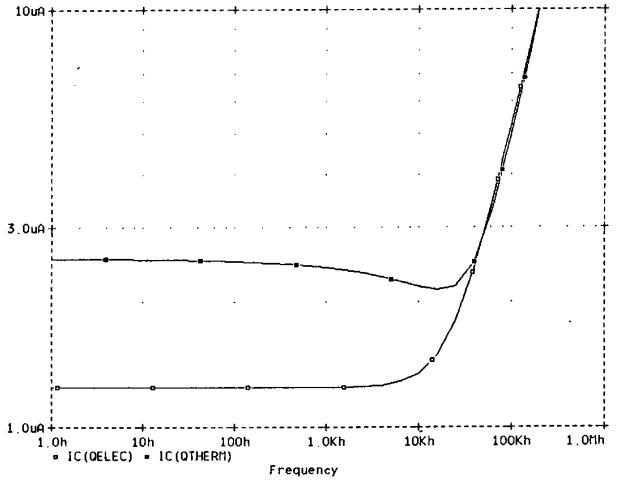


Fig. 7. Magnitude and phase of thermal spreading impedance Z_{th}. Circled values were computed using Eqns. 2 and 4; uncircled curves were computed using the Fourier transform of the model in [3].

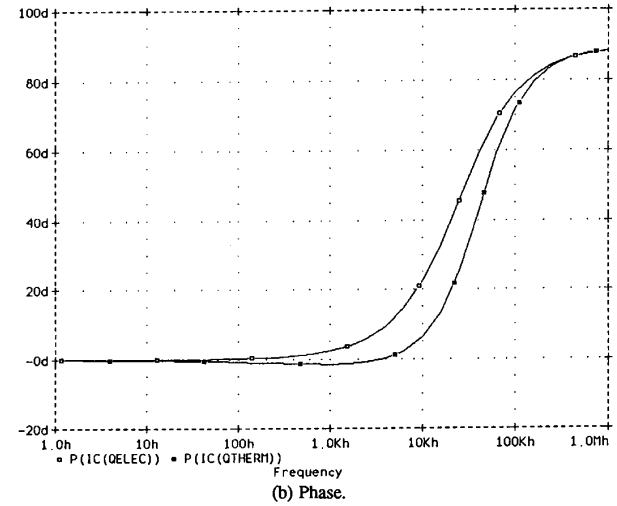
first modeling approach are shown in Fig. 8. The 500 μA current is quite modest for the device under simulation; thermal effects become more significant at higher current densities.

Conclusion

Considering the significant effects which thermal feedback has on BJT behavior, it is interesting to speculate why thermal effects are not yet routinely included in circuit simulators, in spite of prior work on including such effects, [7, 8]. One contributing factor may be the willingness of many circuit designers to accept empirical models — model parameters can be adjusted to account for many thermal effects. Figure 9 demonstrates that even this empirical approach can lead to significant errors. Extractions of the SPICE parameter VAF were done under several different conditions. Differences greater than 30% were found depending on HP4145 integration time, and whether or not a fan was blowing on the package to change its effective thermal impedance. This should give pause to the analog IC designer — such thermal effects could cause the gain of a two-stage op amp to vary more than 2 to 1 depending on package type and mounting conditions.



(a) Magnitude.



(b) Phase.

Fig. 8. Y_{22} of transistor from Figs. 1 and 6, predicted by modified PSPICE with and without correction for thermal effects. I_C = 500 μA.

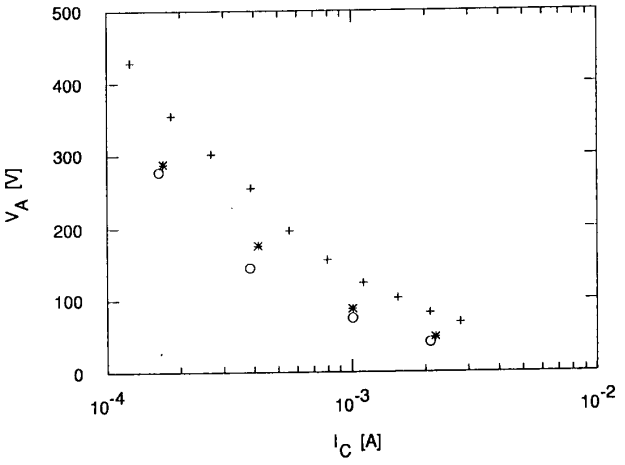


Fig. 9. V_{AF} values optimized for various currents, extracted under different thermal conditions: +: using an HP-4145 at minimum delay between points; *: static measurement with small fan blowing on the 14-pin DIP; o: static measurement without fan.

Acknowledgments

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References

1. J. J. Sparks, "Voltage Feedback and Thermal Resistance in Junction Transistors," Proc. IRE, vol. 46, pp. 1305-1306, June 1958.
2. G. Meijer, "The Current Dependency of the Output Conductance of Voltage-Driven Bipolar Transistors," IEEE J. Solid-State Circuits, vol. SC-12, no. 4, pp. 428-429, August 1977.
3. R. C. Joy and E. S. Schlig, "Thermal Properties of Very Fast Transistors," IEEE Trans. Electron Devices, vol. ED-17, no. 8, pp. 586-594, August 1970.
4. R. T. Dennison and K. M. Walter, "Local Thermal Effects in High Performance Bipolar Devices/Circuits", Proc. IEEE Bipolar Circuits and Technology Meeting, pp. 164-167, Sept. 1989.
5. H. S. Carslaw and J. C. Jaeger, "Conduction of Heat in Solids," 2nd ed. Oxford: Oxford University Press, 1962.
6. O. Mueller, "Internal Thermal Feedback in Four-Poles Especially in Transistors," Proc. of the IEEE, pp. 924-930, August 1964.
7. K. Fukahori and P. R. Gray, "Computer Simulation of Integrated Circuits in the Presence of Electrothermal Interaction," IEEE J. Solid-State Circuits, vol. SC-11, pp. 834-846, Dec. 1976.
8. R. Vogelsong and C. Brzezinski, "Simulation of Thermal Effects in Electrical Systems," APEC '89, Baltimore, MD, March 1989.