A Low Power CMOS RF Transmitter Front-end For 2.4 GHz ZigBee Applications

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Abstract - **This paper presents a low-power transmitter front-end for 2.4 GHz ZigBee applications, in a 0.18 μm CMOS technology. The upconversion mixer is implemented by using a passive mixer topology which dissipates no DC current and exhibits good linearity. Low-power, high-linearity driver amplifier is designed by adopting a folded cascode topology with an additional gate-source capacitor. The measurements show 12 dB conversion gain, 0 dBm output power, 11 dBm OIP3 and 30 dB LO rejection while dissipating 1.8 mA from 1.8 V supply.**

I. INTRODUCTION

With the success of wireless local area networks (WLANs), the wireless networking community has been focused on enhancing WLAN capabilities and developing new approaches to meet the needs of the growing pool of applications requiring wireless devices. So far wireless networking has been mainly focused on high data-rate and relatively long range applications. Recently, the concept of a standardized low data rate wireless personal area networking (LR-WPAN), IEEE 802.15.4 ZigBee, in the frequency band of 868/915 MHz and 2.4 GHz, has been emerged [1]. Table I shows the target market and applications of ZigBee standard.

TABLE I
MARKETS & APPLICATIONS OF ZIGBEE STANDARD

Target Markets	Applications
Industrial & Commercial	Monitor, Sensors, Automation, Control
Home Automation	Security, Lighting, Locking, Heathing, Ventilation and air conditioning (HVAC)
PC peripherals	Mouse, Keyboard, Joystick, Gamepad
Consumer Electronics	TV, VCR, DVD, CD, Remote control
Personal Heath Care	Monotors, Diagnostics, Medical Sensors
Toy & Games	Pets, Games, Educational

As shown in Table I, there are so many applications for this low date rate standard such as industrial and commercial, home automation, personal compu er peripherals, consumer electronics, personal health care, and toys and game that should be able to operate for six months to two years in just button cells or batteries [2].

There are several works on low power 2.4 GHz transmitter that have been reported in literature [3], [4]. However, those works still consume high power. With the motivation of low power, high linearity to fulfill the demand of new trends, this paper presents a low-power CMOS transmitter front-end for 2.4 GHz IEEE 802.15.4 ZigBee standard based on 0.18 μm CMOS technology. The transmitter architecture and the radio specifications are described in Section II. Section III presents the practical circuit design. The measured results are summarized in Section IV and Section V concludes this work

II. TRANSMITTER ARCHITECTURE AND SPECIFICATIONS

With the main goals of low cost, low power and small size wireless transceiver, the direct conversion transceiver architecture based on CMOS technology is one of the popular architectures where the off-chip IF filters and IF c rcuits are no longer necessary such that the power dissipation can be saved and easily implemented as a single-chip [5], [6]. The proposed transmitter architecture is shown in Fig. 1 consisting of low pass filter (LPF), variable gain amplifier (VGA), I/Q up-mixer and a single-ended driver amplifier (DA). In this architecture, single-ended DA is adopted following the double-balanced mixers. The adoption of a single-ended DA eliminates the requirement of balun circuit or differential circuitry to reduce power consumption. As can be seen in Fig. 1, one of the differential upconversion output signals is connected to DA while the second one is connected to AC ground. From the simulation we have found that by using this approach the gain of overall RF front-end is reduced by 3 dB while taking fully advantages of the differential circuitry.

In the design of digital communications, Nyquist filtering is typically used to limit the required bandwidth of the transmitted signal without producing inter-symbol interference (ISI). A common Nyquist filtering method is to use a raised cosine pulse shaping with different rolloff factor ($0 \leq$ rolloff factor ≤ 1). With decreasing the rolloff factor, the bandwidth decreases further, and the frequency response becomes more like a rectangular pulse. Since the ZigBee standard allows larger channel spacing (5 MHz for 2.4 GHz band), therefore the bandwidth limitation can be relaxed with increasing the rolloff factor. The standard specifies the rolloff factor of 1 for the raised cosine filter, and this condition relaxes the filtering requirement of the TX low pass filter (LPF). With different rolloff factor of the raised cosine pulse shaping filter, the peak-to-average power ratio (PAPR) at the TX output increases. PAPR

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is defined as the ratio of the peak envelope power to the average power of the transmit signal [7]. This PAPR parameter gives a theoretical maximum output back-off requirement in the transmitter. From a PAPR simulation with rolloff factor of 1 and assuming the nominal transmit output power of 0 dBm, the output 1 dB compression point of the transmitter output state should be over 0 dBm, and the output third-order inter-modulation products, OIP3, should be over 10 dBm.

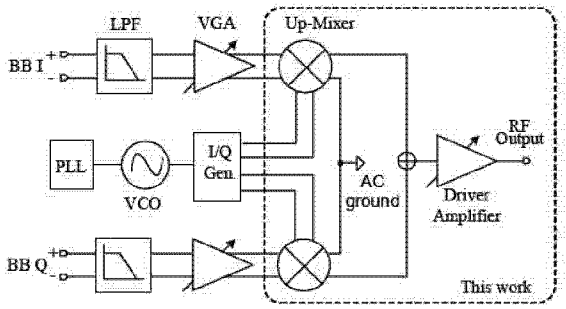

Fig. 1 The transmitter architecture

III. CIRCUIT DESIGN

A. Upconversion Mixer

High performance mixers in CMOS are either active based on current switching, or passive based on voltage switching mixers. In this design, as the way to minimize the power consumption, the passive mixer shown in Fig. 2 was chosen since it dissipates no DC current. The absence of DC current through the switches also makes it possible to eliminate the 1/f noise, which otherwise is a problem especially for direct conversion receivers [8]. However, in the transmitter wise, linearity and power conversion gain of the mixer are the most critical parameters that need to be considered carefully.

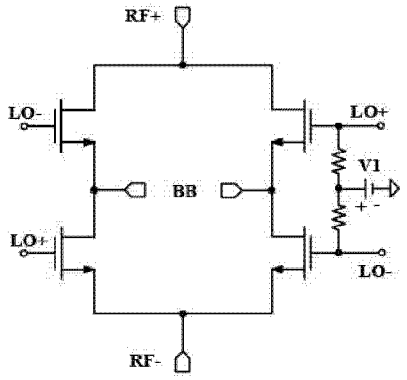

Fig. 2. Schematic of upconversion mixer

In the Fig. 2, there are two parameters that designer can play with are the device's size and the DC level of the LO signals, V_1. Typically, the LO signal is driven by the narrow band buffer which is normally implemented by inductive load amplifier. The function of the inductive load is to resonate with the gate-source capacitor of the switching transistors. Therefore if the size of the switching transistors is larger, the loading inductance is smaller leading to low output power of LO signal. Therefore low mixer conversion gain is obtained ii) When the size of switching transistors is small, the loading inductance becomes larger leading larger silicon area, low linearity and stability problem of the buffer. The DC level at the gate of the switching transistor, V_1, is also important since it controls the switching mode. In the balanced driver case, equal amount of time in both on and off state, the voltage conversion gain of the mixer is theoretically equal to $2/\pi$. If the switches are set to have less on-time than off-time, often referred to break-before-make, the conversion gain will maximally equal to 1 [8], but the mixer will also be less linearity. Thus there will be a trade-off between the mixer conversion gain and linearity. In this design, in order to compromise the gain, linearity and the inductive load of the LO buffer the size of switching transistors and their bias voltage, V_1, are 130 μm and 1.42 V, respectively.

B. Driver Amplifier

The proposed driver amplifier, DA, shown in Fig. 3 is a single-ended folded cascode amplifier topology. The folded-cascode topology is chosen due to the following reasons: i) folded-cascode structur allows higher voltage headroom which helps the linearity improvement, ii) gain can be controlled by varying the DC current of PMOS transistor by changing the DC voltage at the gate of the cascode transistor [9]. As can be seen in Fig. 3, the proposed DA is differs by one additional capacitor, C_{ex}, in comparison with the conventional folded cascode topology. This additional capacitor is added in order to keep the amplifier operate in class-A mode while dissipating low DC current.

As a linear amplifier, the class-A operation provides the best linearity [10]. The class-A operation implies that the dynamic output current should not exceed the bias current (I_D) at its maximum input power level (P_{in}). To achieve higher power efficiency it is also important that the current swing is maximized, i.e., output current swing is maximized when maximum input power is fed to DA. This means that the power-to-current gain of the input stage is fixed for a given bias current and maximum input power level. Therefore, the bias current needed to guarantee class-A operation is given by [11]

$$I_D = i_{d,peak} = \frac{f_t\sqrt{2P_{in}}}{f_o\sqrt{R_s}} \quad (1)$$

where R_s is the source resistance of the amplifier, f_t the cut-off frequency of input transistor, f_o the operating frequency.

Considering the low power objective of the given transmitter design, it is important to reduce the bias current I_D. From (1) it can be seen that, for the given level of input power P_{in}, to reduce I_D while keeping the input transistor in class-A operation, reducing f_t is the only solution as R_s is typically determined by the preceding stage (in this design it is equal to the output impedance of the up-mixer). This can only be done if another design parameter is introduced that decouples

the relation between g_m and C_{gs}. A straightforward way of reducing f_t is to increase the transistor length L which reduces g_m and increases C_{gs}. Increasing L has undesirable effect of linearity degradation due to the quadratic I-V relation. Alternatively, a PMOS transistor, which have much lower f_t, can be used in the input stage. However, for a given amount of bias current, PMOS transistors provide lower transconductance which lead to lower gain of amplifier.

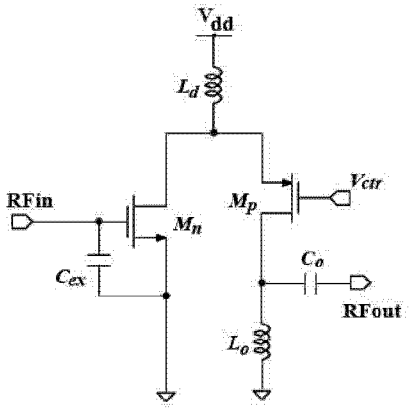

Fig. 3 Schematic of the driver amplifier

A third method is to add an external capacitor C_{ex} between the gate and source terminals of the input transistor. This way the effective f_t, $f_{t,eff}$ is reduced without reducing the intrinsic transistor f_t. Of course the reduction of effective f_t of the input transistor would lower the power gain. However, the power gain is a slow function of C_{ex}. For example, if $C_{ex} = 3C_{gs}$, the f_t of input transistor will be reduced by the factor of 4. This would lead to the reduction of the maximum oscillation frequency (f_{max}) by the factor of $\sqrt{2}$ due to the square-root functional dependence of the f_{max} on f_t. In this design, the method that used C_{ex} is chosen.

In Fig. 3, the parasitic capacitances at the drain node of the input transistor can easily be eliminated by the adoption of inductor L_d to the supply voltage. The elimination or the reductions of these parasitic capacitances help to avoid the signal loss into the silicon substrate, leading to better DA gain [12]. In Fig. 3, a simple L_o-C_o network is used to match the output impedance of DA to 50Ω. High-Q off-chip inductor L_o helps to improve the linearity of driver amplifier [13].

IV. Measurement Results

The RF transmitter front-end with the EDS protection is fabricated in 0.18 um CMOS technology which is shown in Fig. 4. It has an active area of 1.5 mm^2 and consumes 2 mA from 1.8 V supply. The testing board has been built by directly bonding the die on a two-layer FR4 substrate. To supply differential signal at input LO port, a commercial passive balun has been used and 5 dB of balun loss according to its measurement has been de-embedded from the measurement.

Fig. 5 shows the output spectrum of the transmitter front-end baseband input signal power of -12 dBm at 5 MHz and LO signal power of 0.5 dBm at 2.4 GHz. As can be seen in Fig. 5, the measured power conversion gain is 12 dB and LO suppression is 30 dB. In this measurement, only one channel (I or Q) is applied such that there exits a low side band (LSB) signal. However, the LSB signal can be removed if I/Q signals are applied as shown in Fig. 6.

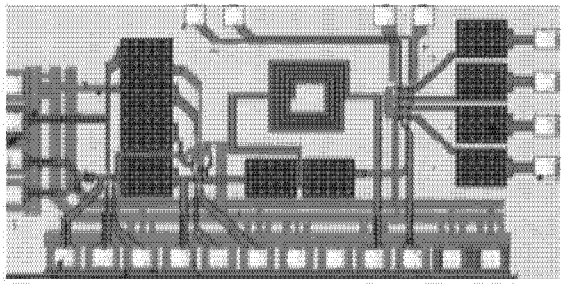

Fig. 4. Microphotograph of the RF transmitter front-end

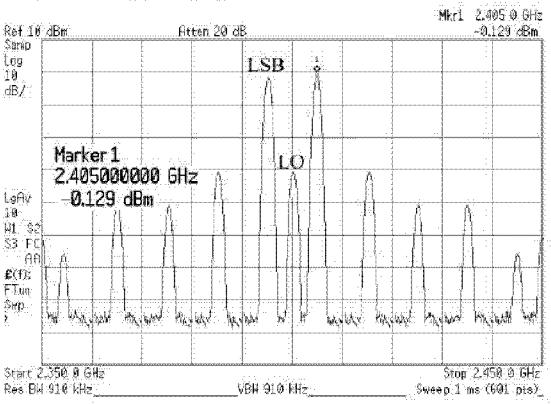

Fig. 5. Measured output spectrum of the RF transmitter front-end at the -12 dBm input power

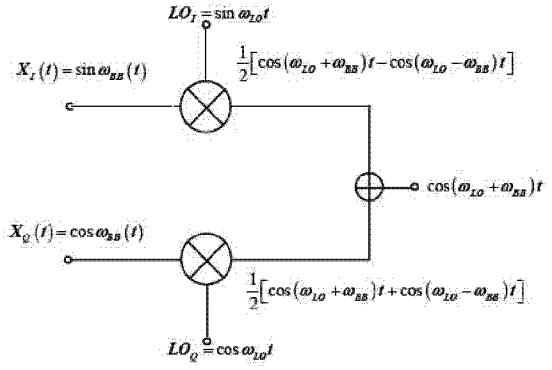

Fig. 6. LSB signal canceling mechanism in IQ path

Fig. 7 shows the measured result of output third-order nonlinearity, OIP3, of the RF transmitter front-end at its highest gain. As can be seen in Fig. 7, the obtained result of OIP3 is 11 dBm which satisfies the standard requirement as mentioned before. Fig. 8 shows the output return loss, S_{22}, of the RF transmitter front-end. The measured results are quite compromising with the

simulated results. The overall measured performances of RF transmitter are summarized in Table II.

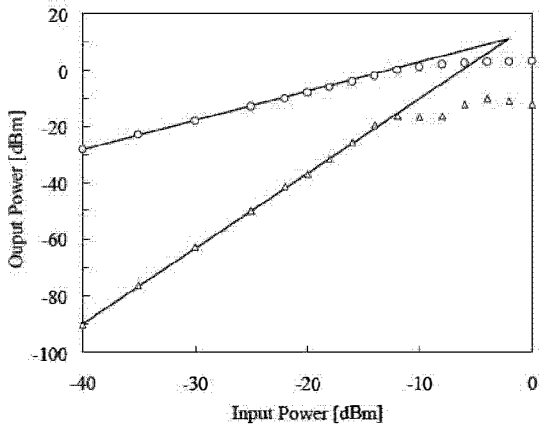

Fig. 7. Measured OIP3 of the RF transmitter front-end at its highest gain mode

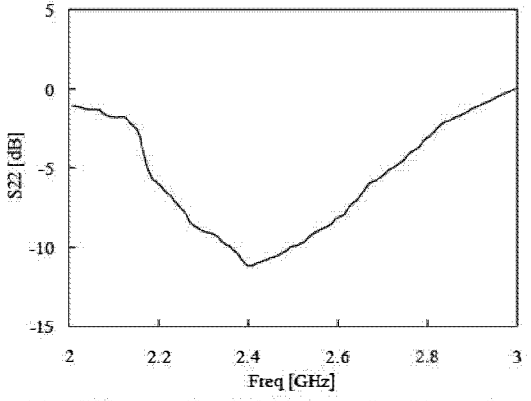

Fig. 8. Measured S_{22} of the RF transmitter front-end

TABLE I
MEASURED SUMMARY OF RF TRANSMITTER FRONT-END

Parameters	Value
Operation frequency [GHz]	2.4
Power conversion gain [dB]	12
Output power [dBm]	0
OIP3 [dBm]	11 dBm (at high gain mode)
Gain-range variation [dB]	12
LO suppression [dB]	30
Output return loss [dB]	-12
Supply voltage [V]	1.8
Current dissipation [mA]	2
Chip area [mm^2]	1.5
Technology [μm]	0.18 CMOS

V. CONCLUSION

This work presents a low voltage low power RF transmitter front-end for 2.4 GHz Zigbee applications. The upconversion mixer is implemented by adopting the passive topology which is suitable for low power applications. With the driver amplifier, high linearity under low power consumption is archived by using a folded cascode amplifier topology with an extra capacitor at the gate-source terminal of the input transistor. The proposed RF transmitter front-end is implemented in a 0.18 μm CMOS technology. The measurements show the total power conversion gain of 12 dB, output power 0 dBm, LO rejection of 30 dB, a d dB-linear gain-range of 12 dB with the linearity less than ± 0.5 dB. The RF transmitter front-end dissipates 1.8 mA from 1.8 V supply and occupies 1.5 mm^2 of silicon area.

ACKNOWLEDGEMENTS

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