Low Power High Linearity Driver Amplifier for 1.9 GHz WCDMA Applications

V.H Le, T.K Nguyen, S.K Han and S.G Lee

Abstract –**This paper presents a low power high linearity driver amplifier for 1.9 GHz WCDMA applications based on 0.18 μm CMOS technology. In this work folded cascode amplifier is adopted to get more efficient power transmission. High gain and linearity are achieved by applying resonating load and gain boosting technique. Simulation shows 11 dB of gain, 5.8 dBm output P1dB while dissipating 0.8 mA DC current from 1.8 V supply.**

I. INTRODUCTION

Building low-power operation wireless systems will probably be one of the most important design goals. This is a prerequisite for the full penetration of wireless systems in our daily life, especially for short-range communication between, e.g., cellular phones, personal digital assistants (PDAs), wrist watches, headsets, etc. In a wireless system RF power amplifier (PA) in the transmitter front-end is one of the most power-consuming building blocks.

With the motivation of low power high linearity transmitter to fulfill the demand of new technology trends, this paper presents a low power high linearity driver amplifier (DA), which eases the burden of high linear power transmission in the following PA, for 1.900 GHz WCDMA applications. As suggested in [1] RF CMOS is a strong contender for W-CDMA applications since it has advances with respect to improved devices, circuit topologies, and system-level architecture. The proposed amplifier in this paper is simulated in CMOS 0.18 μm process. The simulated results show 11 dB power gain, -19 dB of output return loss in operating frequency and very high linear power transmission which is presented in 5.8 dBm output P-1dB while dissipating 0.8 mA from 1.8 V supply.

II. CIRCUIT DESIGNS

Considering the required radio specifications and with the key point of high gain, low power consumption and high linearity, the solution we are presenting here is folded cascode driver amplifier shown in Fig. 1. In general, the conventional cascode amplifier can provide good linearity. However stacking two transistors limits the output voltage swing at the output. Therefore, to maximize output voltage swing, the folded-cascode structure is then adopted.

In this folded cascode amplifier shown in Fig. 1, the current source is replaced by an inductor L1 such that voltage swing at the output is maximized. Inductor L1 resonated with parasitic capacitor at this node X will introduce high impedance to ac ground at this node and prevent the signal loss into the silicon substrate to get the highest achievable gain [2]. As can be seen in Fig. 1, an additional capacitors Cex is added to gate-to-source of input transistors to keep the input signal linear because otherwise the intrinsic gate source capacitance which is essentially a bias dependent varactor may lead to significant distortion at high input power levels [3]. To save the DC current the input transistor is bias at very low gate to source voltage. At this low bias voltage transistor drops into class A-B operation. When high power signal is applied, DC drain current is then increased leading to power gain is boosted. As a result, output power and therefore output 1dB compression point is increased. From simulation, we have seen that by applying this gain booting technique the output P-1dB compression point is improved significantly. At the input transistor, in Fig. 1, an inductive degeneration Ls, which is implemented as wire-bonding, helps to improve linearity by lowering the gain through negative feedback. At the drain output, inductor L2 which introduces very high impedance to this node plays as the load as well as output matching with capacitor C2 and C3.

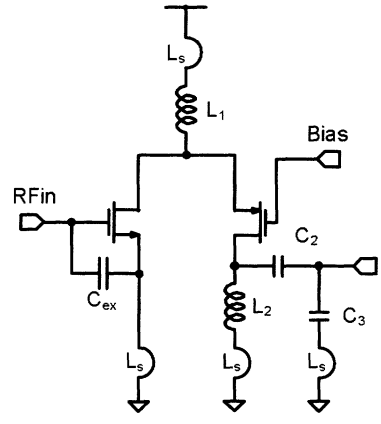

Fig. 1. Proposed driver amplifier.

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III. SIMULATION RESULTS

The driver amplifier is designed in 0.18μm CMOS technology on the Cadence spectre simulator. Fig. 2 shows the simulated power gain, S_{21}, of the proposed DA. As can be seen in Fig. 2, DA exhibits 11 dB gain at operating frequency (1920-1980 MHz) with 0.3 dB variation. Output return loss is also shown in Fig. 2, the result is < -15 dB in operating frequency (1920-1980 MHz). Fig. 3 shows the simulated output P-1dB of the DA which is 5.8 dBm. Fig. 4 shows the layout of the DA chip with the chip's size of 0.6x1 mm^2. Table. I summarizes the simulation results of the DA.

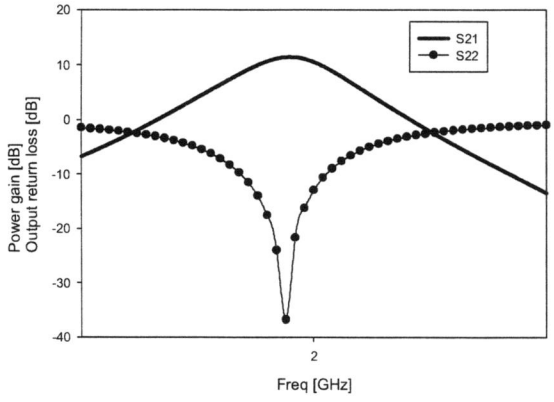

Fig. 2. Simulated power gain of DA.

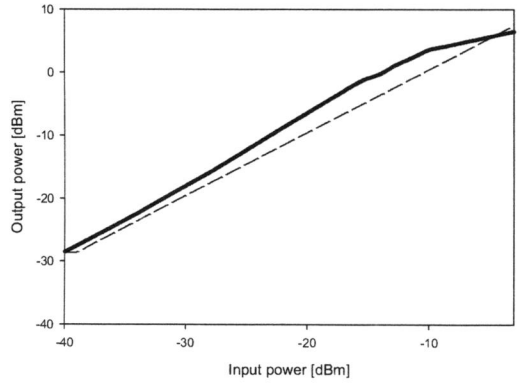

Fig. 3. Simulated output P-1 dB compression point of the DA

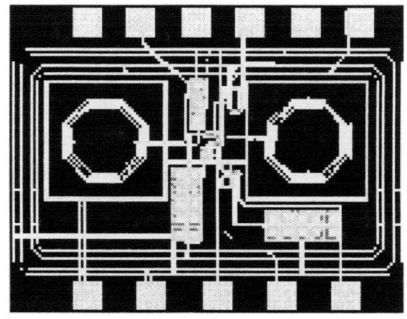

Fig. 4 Driver amplifier layout

III. CONCLUSION

A 1.9 GHz CMOS driver amplifier is presented for WCDMA application. To get high output power and high linearity under low power consumption, the gain boosting technique is applied. In addition, an added capacitor at gate-to-source input transistor linearizes the strong input signal therefore improve the linearity. Simulated DA shows 11 dB of gain and 5.8 dBm of output 1 dB compression point at operating frequency. Current consumption is 0.8 mA from 1.8 V supply.

TABLE I
SUMMARY OF THE SIMULATION OF DRIVER AMPLIFIER

Opearating frequency [MHz]	1920-1980
Power gain S_{21} [dB]	11
Inband gain ripple [dB]	0.3
Output return loss [dB]	<-15
Output P1 dB [dBm]	5.8
Supply voltage [V]	1.8
Power consumption [mW]	1.4
Technology [μm]	CMOS 0.18

ACKNOWLEDGEMENT

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