An All CMOS 743MHz Variable Gain Amplifier for UWB Systems

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ABSTRACT- A newly proposed variable gain amplifier (VGA) that offers wide bandwidth and gain variation characteristics is described for ultra wideband system applications. The proposed VGA combines a cascade-input stage and bandwidth-extension loads to obtain a wide bandwidth. The VGA is simulated in 0.13μm CMOS technology and simulations show a gain variation range of 54dB in a single-stage VGA and a minimum 1-dB bandwidth of 743MHz at the maximum gain of 20dB. The 1-dB bandwidth improvement of 58% compared to conventional VGAs at the same supply current is obtained. In addition, the newly proposed control stage results in a compact VGA, which leads to low power consumption. The VGA dissipates an average supply current of 4.5mA from 1.8V supply voltage.

Keywords: Variable gain amplifier (VGA), automatic gain control (AGC), amplifier, UWB

I. INTRODUCTION

Variable gain amplifier (VGA) is an indispensable block at the front end of many communication systems to maximize the dynamic range of the receivers. VGAs are also used in the transmitter part of communication transceivers to control the transmission signal power. The VGA is usually embedded in an automatic gain control amplifier (AGC) loops to provide constant output signal amplitudes regardless of variations in the input signal.

Recently, many approaches to achieve dB-linear gain variation characteristics of the VGA in CMOS technology have been reported; such as master-slave control [1] and signal-summing techniques [2], or using Taylor concept [3] and pseudo-exponential generator [4, 5, 7, 9, 10] for realizing the dB-linear gain characteristic. The signal-summing VGA has the advantages of high frequency operation, low-noise, and low-distortion; but the gain control range of the one-stage VGA is limited to less than 20 dB and the gain error is large [2]. The master-slave control technique has a gain variation range of less than 20dB per one-stage VGA [2]. The VGAs that adopt the Taylor concept and the pseudo-exponential generator even exhibits less amount of gain control range, which is 12 and 15dB with a gain error of less than ±0.5dB, respectively [3, 5, 7]. Owing to the limitation of the gain range in recent researches, the multiple-stage VGAs are used to satisfy the required dynamic gain range of communication systems (for example; to satisfy 60dB of the gain variation range, 3 gain stages for signal-summing and master-slave control techniques, 4 gain stages for pseudo-exponential generator VGA, and 5 gain stages for Taylor concept approach must be used). Obviously, the multistage VGAs result in a high power consumption and a large chip size (or high cost), which is not compatible with low-voltage low-power small-chip size portable radio transceiver integrated circuit.

Due to the limitation of the gain variation range in conventional VGA designs, a new approximation function that can provide a wider dB-linear variation range has been introduced in [8]. However, the previously reported works show limited bandwidth at a high gain setting [5, 7, 8, 9, 10]. Consequently, these VGA designs can be implemented in narrow band application only.

In this paper, the new VGA topology with bandwidth enhancement techniques is proposed. The gain of the proposed VGA is the same form of expression as in [8] such that a wide variation range VGA is obtained. The proposed VGA is compact, which leads to low-power consumption.

II. CONVENTIONAL VGA DESIGNS

The conventional VGA topology that is widely used in previously reported works is depicted in Fig. 1 [5, 7, 8, 9, 10]. As shown in Fig. 1, the core of the VGA consists of a differential amplifier ($M_{1,2}$) and diode-connected loads ($M_{3,4}$). The differential gain of this VGA is equal to $g_{m-M1,2} \times R_{out}$, where $g_{m\text{-}M1,2}$ is the transconductance of the input differential pair and R_{out} is the output impedance. Since the output is diode-connected loads, R_{out} is proportional to $1/g_{m\text{-}M3,4}$, where $g_{m\text{-}M3,4}$ is the transconductance of the loads ($M_{3,4}$). Since the transconductance is a function of the bias current, the gain variation is obtained by control the bias currents of the input-pair ($M_{1,2}$) and loads ($M_{3,4}$). The gain of the VGA shown in Fig. 1 is given as

$$A_v = \frac{g_{m-M1,2}}{g_{m-M3,4}} = \sqrt{\frac{(W/L)_{M1,2} I_{M1,2}}{(W/L)_{M3,4} I_{M3,4}}} \quad (1).$$

Considering the frequency response of the circuit shown in Fig. 1, the bandwidth of the VGA is dominated by the input and output poles. Since the output loads are diode-connected transistors, the output pole is mainly dependent on the bias current of the transistors $M_{3,4}$. At a lower gain setting, $I_{M3,4}$ and the bandwidth are extended. However, at a higher gain setting, $I_{M3,4}$ is reduced, leading to a reduction of the bandwidth [8]. The input pole is a function of input capacitances. In Fig. 1, the total capacitances at the input node of M_1 is equal to C_{GS} plus the Miller multiplication of C_{GD}: $C_{GS} + (1+ |A_v|)C_{GD}$, where C_{GS} and C_{GD} are gate-source and gate-drain capacitances of transistor M_1, A_v is given in (1). Consequently, the input pole is proportional to the gain A_v such that the bandwidth is reduced significantly at higher gain settings; for example, reference [8] shows a max/min 3-dB bandwidth of 1GHz/40MHz at the minimum and maximum gains, respectively. Therefore, [8] can only be implemented in applications limited to 40MHz. As reported in [9], the cascade input stage was also adopted;

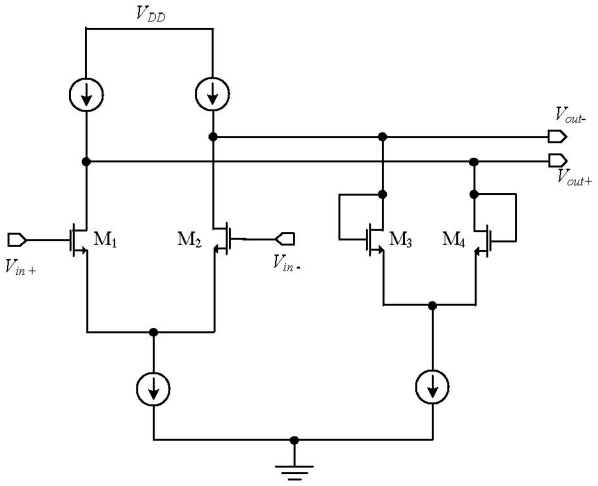

Fig. 1 Schematic of the core pseudo-exponential approximation-based VGAs [5, 7, 8, 9, 10].

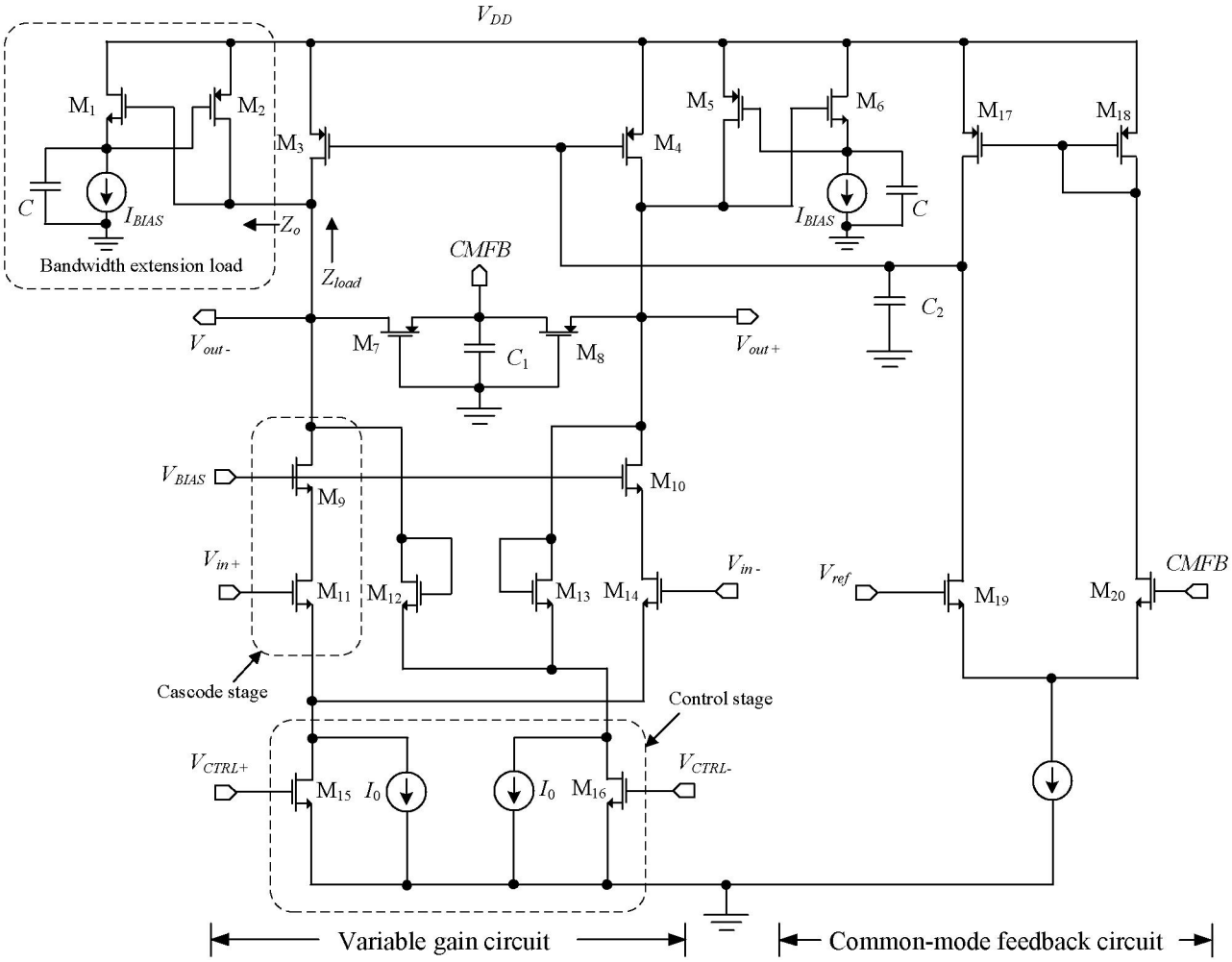

Fig. 2 The complete schematic of the newly proposed VGA

however, the gain of the input different pair remains high, so that no reduction of the Miller multiplication is realized such that the input pole reduces the bandwidth at higher gain settings significantly.

III. NEWLY PROPOSED VGA TOPOLOGY

The newly proposed circuit schematic of the VGA is illustrated in Fig. 2, which is composed of a variable gain circuit and a common-mode feedback circuit. The variable gain circuit utilizes a cascade input stage and a bandwidth extension loads for bandwidth improvements. In Fig. 2, due to the cascade input stage, by setting the size of M_9 equally to M_{11}, the gain from the gate to drain terminals of transistor M_{11} is equal to $g_{m\text{-}M11}/g_{m\text{-}M9} = 1$, therefore the Miller multiplication is minimized so that the input capacitances reaches the smallest value. Consequently, the input pole is moved to a higher frequency, leading to a wider bandwidth.

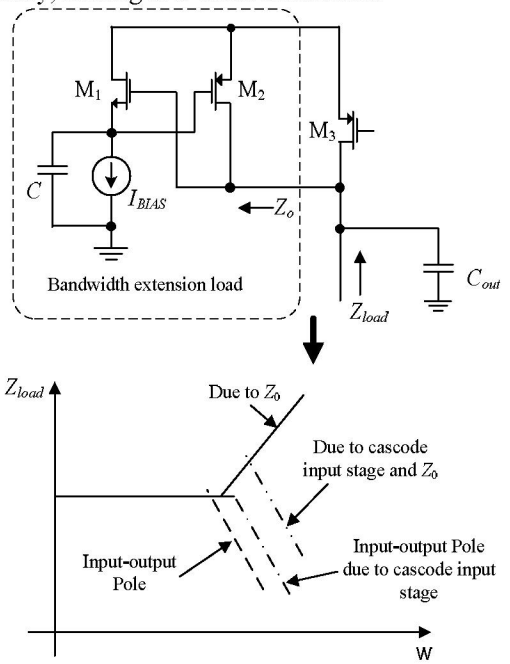

Fig. 3 Bandwidth extension due to cascade input stage and bandwidth extension loads.

In Fig. 2, the load impedance is equal to $Z_0//Z_{M13} \sim Z_0$. From [9], the input impedance of the bandwidth extension loads can be given as

$$Z_0 \cong \frac{1}{g_{m-M2}}\left(1+\frac{s}{g_{m-M1}/C}\right) \quad (2).$$

Equation (2) shows a "zero" at the output node, leading to the extension of the bandwidth. The summary of the bandwidth extension techniques is depicted in Fig. 3. In Fig. 3, the conventional VGAs is depicted by the dashed line, by utilizing the cascade input stage, the dashed line is moved to the dash-dotted line, resulting in a wider bandwidth. The load Z_0 given in (2) and shown in Fig. 3 by the solid line leads to the shift of the dash-dotted line to the dash-dot-dotted line, which provides additional bandwidth improvement.

In Fig. 2, the control stage is newly proposed with a differential control signal, $V_{CTRL+} = V_{BIAS} + V_{CTRL}$ and $V_{CTRL-} = V_{BIAS} - V_{CTRL}$, where V_{BIAS} is a bias voltage and V_{CTRL} the differential control voltage. Transistors M_{15} and M_{16} are biased in saturation mode. The bias currents of the input pair ($M_{11,14}$) and loads ($M_{12,13}$) are respectively given as

$$I_{M11,14} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{BIAS}+V_{CTRL}-V_{th}\right)^2 + I_0 \quad (3)$$

$$I_{M12,13} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{BIAS}-V_{CTRL}-V_{th}\right)^2 + I_0 \quad (4)$$

where V_{th} is the threshold voltages of NMOS transistors $M_{15,16}$, I_0 the bias current. From (1), (3), and (4), the gain of the proposed VGA shown in Fig. 2 is given as

$$A_v = \frac{g_{m-M11,14}}{g_{m-M12,13}} = \sqrt{\frac{(W/L)_{M11,14} I_{M11,14}}{(W/L)_{M12,13} I_{M12,13}}} \quad (5).$$

Assuming that $(W/L)_{M11,14} = (W/L)_{M11,14}$, from (3), (4), and (5), the gain of the proposed VGA is calculated as

$$A_v = \left(\frac{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{BIAS}+V_{CTRL}-V_{th}\right)^2 + I_0}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{BIAS}-V_{CTRL}-V_{th}\right)^2 + I_0}\right)^{1/2}$$

$$= \left(\frac{\frac{I_0}{K\left(V_{BIAS}-V_{th}\right)^2}+\left(1+\frac{V_{CTRL}}{V_{BIAS}-V_{th}}\right)^2}{\frac{I_0}{K\left(V_{BIAS}-V_{th}\right)^2}+\left(1-\frac{V_{CTRL}}{V_{BIAS}-V_{th}}\right)^2}\right)^{1/2}$$

$$= \left(\frac{\left[k+(1+ax)^2\right]}{\left[k+(1-ax)^2\right]}\right)^{1/2} \quad (6)$$

where $k = I_0/K(V_{BIAS} - V_{th})^2$, $a = 1/(V_{BIAS} - V_{th})$, and $K = \mu_n C_{ox}W/2L$. As reported in [8], the proposed VGA can achieved 60dB gain variation for $k = 0.15$.

IV. SIMULATION RESULTS

The proposed VGA is simulated in 0.13μm CMOS technology and dissipates 4.5mA from the supply voltage of 1.8V. Fig. 4 shows the simulated gain versus control voltage V_{CTRL} at 100MHz. As expected, the proposed VGA shows a very wide gain variation range of 54dB.

To verify the validity of the bandwidth enhancement techniques, two VGAs are designed; one with cascade input stage and bandwidth extension loads and the other (the conventional one) without any bandwidth enhance-

ment techniques at the same supply current. Fig. 5 shows the frequency response of the proposed VGA and the conventional one at different gain settings. As shown in Fig. 5 by the dashed lines, at a high gain mode, the bandwidth of the conventional VGA is reduced. The 1-dB bandwidths of the conventional VGA (dashed line) and the proposed VGA (solid line) at a gain of 20dB are respectively 470 and 743MHz. The bandwidth improvement of 58% compared to the conventional one is achieved, while dissipating the same bias current.

The comparisons of the proposed VGA with the conventional one is given in Table. I.

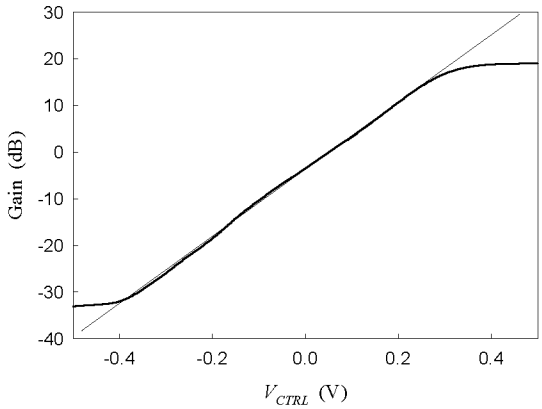

Fig. 4 Simulated gain versus control voltage V_{CTRL} of the proposed VGA shown in Fig. 2.

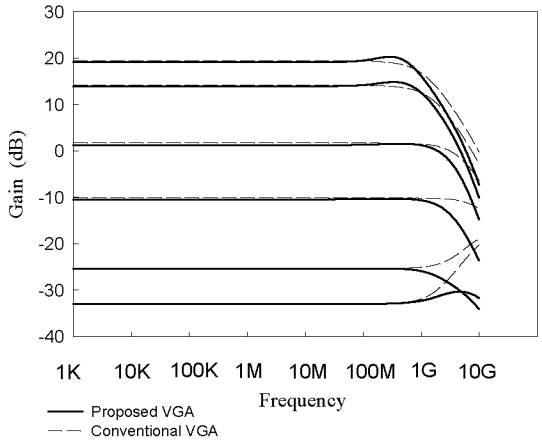

Fig. 5 Simulated gain versus frequency at different gain settings.

V. CONCLUSIONS

The newly proposed VGA topology shows a very wide bandwidth compared to the conventional topology of VGAs reported in previous works [3, 4, 5, 6], while consuming the same supply current. The newly proposed control stage is compact, which results in low-power consumption and obtains a wide gain variation range in a single-stage VGA. The proposed VGA could be used for the wideband system applications.

TABLE I. SUMMARY OF SIMULATION RESULTS

	Conventional VGA	Proposed VGA
Technology	0.13μm	0.13μm
Power consumption	4.5mA/1.8V	4.5mA/1.8V
Minimized 1-dB bandwidth	470MHz	743MHz
Gain range	-34~20dB	-34dB ~ 20dB
Gain error	±0.5dB	±0.5dB

ACKNOWLEGENMENT

This work was supported by SAMSUNG ELECTRO-MECHANICS CO., LTD under the SRC/ERC program of MOST/KOSEF (Intelligent Radio Engineering Center). SAMSUNG ELECTRO-MECHANICS CO., LTD. 314, Maetan3-Dong, Yeongtong-Gu, Suwon, Gyunggi-Do, Korea 443-743.

REFERENCES

[1] T. Yamaji, N. Kanou and T. Itakura, "A Temperature-Stable CMOS Variable-Gain Amplifer with 80-dB Linearly Controlled Gain Range," ***J. of Solid-State Circuits***, vol. 37, no. 5, pp553-558, May. 2002.

[2] O. Watanabe, S. Otaka, M. Ashida, T. Itakura, "A 380-MHz CMOS linear-in-dB signal-summing variable gain amplifier with gain compensation techniques for CDMA systems," ***Digest of Technical Papers Symposium on VLSI Circuits***, pp. 136-139, 2002

[3] C.-C Chang, M.-L. Lin, and S.-I. Liu, "CMOS Current-mode Exponential-Control Variable-Gain Amplifier," ***IEE Electronics Letters***, vol. 37, no. 14, pp 868-869, July 2001.

[4] R. Harjani, "A Low-Power CMOS VGA for 50 Mb/s Disk Drive Read Channels," ***Transaction on circuit and system-II***, vol. 42, pp 370-376, June 1995.

[5] Christopher W. M, "A Variable Gain CMOS Amplifier with Exponential Gain Control," ***Digest of Technical Papers Symposium on VLSI Circuits***, pp. 146-149, 2000.

[6] Gurkanwal Singh Sahota, Charles James Persico, "High Dynamic Range Variable-Gain Amplifier for CDMA Wireless Applications," ***Digest of Technical Papers IEEE ISSCC***, pp. 374-375, 1997.

[7] P. Huang, L.Y. Chiou, and C.K. Wang, "A 3.3-V CMOS Wideband Exponential Control Variable-Gain-Amplifier," ***International Symposium on Circuit and System***, pp. I-285-I-288, May 1998.

[8] Quoc-Hoang Duong, Le-Quan, and Sang-Gug Lee, "An All CMOS 84dB-Linear Low-Power Variable Gain Amplifier," ***Digest of Technical Papers Symposium on VLSI Circuits***, pp. 114-117, 2005.

[9] J.K. Kwon, K.D. Kim, W.C. Song and G.H. Cho, "Wideband high dynamic range CMOS Variable-Gain Amplifier for low voltage and low power wireless applications," ***IEE Electronics Letters***, vol. 39, no. 10, pp 759-760, May 2003.

[10] R. Saito, K. Hosoda, A. Hyogo, T. Maruyama, H, Komuraki, H. Sato, K. Sekine, "A 1.8-V 73-dB Dynamic-Range CMOS Variable Gain Amplifier," ***ESSCIRC03***, pp301-304, 2003.