Low-Voltage, Low-Power CMOS Operation Transconductance Amplifier with Rail-to-Rail Differential Input Range

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***Abstract*—This paper presents a new configuration for linear MOS operation transconductance amplifier (OTA) based on a standard 0.25 μ CMOS technology. The proposed circuit combines two previously reported linearization techniques: source degeneration using MOS transistor and class AB linearization. Measured results show that the proposed circuit provides rail-to-rail differential input range. Total harmonic distortion of the proposed circuit is –60 dB at 5 MHz for 0.6-Vpp differential input voltage while dissipating only 25 μW from 1.25 V supply.**

I. INTRODUCTION

The trend toward lower operating supply voltages and lower power consumption in mixed signal ICs has some strong motivations: 1) portable equipment capable of the operating with minimum number of battery cells to reduce volume and weight, 2) voltage limitations resulted from smaller feature sizes of modern IC technology, and 3) longer operating periods without battery recharging or replacement.

The operational transconductance amplifier (OTA) is a basic building block in analog circuit applications including continuous-time filter, data converter, variable gain amplifiers and other interface circuit [1]-[3]. In many of these applications, OTA at the input determines the overall linearity of the system [4]. As device sizes, supply voltage and power consumption are scaled down to achieve higher operating-speeds, obtaining high linearity with reasonable signal levels becomes ever challenging. Several circuit techniques have been proposed in literature to improve the linearity of MOS transconductors. The linearization methods include: cross-coupling of multiple differential pairs, [5]-[7], adapting biasing [8], source degeneration (using resistor or transistor) [9], [10], shift level biasing [11], series connection of multiple differential pairs [12], class AB configuration [13], and pseudodifferrential stages (using transistors in the triode region or in saturation) [14], [15]. This paper presents an improved linear MOS transconductor that uses both the source degeneration using MOS transistor and class AB configuration approaches. Section II reviews these two linearization techniques and the configuration of the newly proposed transconductor is described. The experimental results and discussions are presented in Section III. The proposed transconductor has been fabricated in a standard 0.25 μm CMOS technology, using 1.25 V supply. And then, the conclusion is presented in Section IV.

II. CIRCUIT DESIGN

A. Circuit topologies for linear CMOS OTA

In this section, we will review some linearization techniques that are reported in literature. The simplest technique to linearize the transfer characteristic of the MOS transconductor is the one with source degeneration using resistors as shows in Fig. 1.

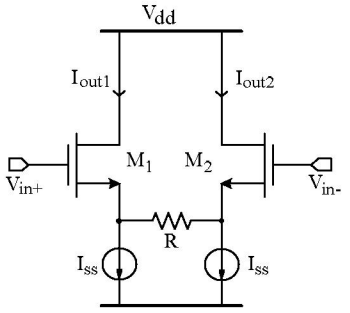

Fig. 1 MOS transconductor with resistive degeneration

The linearization is achieved because now the output current $I_{out} = I_{out1} - I_{out2}$ becomes

$$I_{out} = \frac{1}{2}(V_{id} - I_{out}R)\sqrt{2I_{ss}K_n}\sqrt{1-\frac{(V_{id} - I_{out}R)^2 K_n}{2I_{ss}}} \quad (1)$$

where

- $K_n = \frac{1}{2}C_{ox}\frac{W}{L}$
- V_{tn} and V_{id} are the threshold voltage of NMOS and the differential input voltage respectively.

- W and L are the width and length of the transistor. I_{ss} and R are the bias current and degeneration resistor respectively.

The transconductance G_m is

$$G_m \approx \frac{g_m}{1+g_m R} \tag{2}$$

where g_m is the transconductance of transistor M_1, M_2 (here we assume that M_1, M_2 are matched)

Notice that in (1), the nonlinear term now depends on $V_{id} - I_{out}R$ rather than V_{id}. When $R >> 1/g_m$ the non-linear term becomes zero so high linearity can be obtained. The disadvantage of this configuration is the large resistor value, which is needed to achieve a widely linear input range. Since in this case $G_m \approx 1/R$, the obtained transconductance is restricted by the value of degeneration resistor. If we would like to obtain high transconductance with higher linearity R should be reduced while g_m should be increased. High g_m requires higher power consumption. Moreover, this technique eliminates the tenability of the G_m is set by the degeneration resistor.

The second technique is also using source degeneration but replacing the degeneration resistor with two MOS transistors operating in the triode region that is shown in Fig.2 [9]. Qualitatively, when the amplitude of the input signal rises, the triode-mode degeneration MOS resistors will be more biased such that the synthesized resistance is reduce. This allows less degeneration and results in more G_m of the differential pair to compensate for the drop of G_m. As discussed in [9], the size ratio of M_1/M_3 = 6.7 is used to obtain the maximally linear behavior. The quantitative relationship is given by

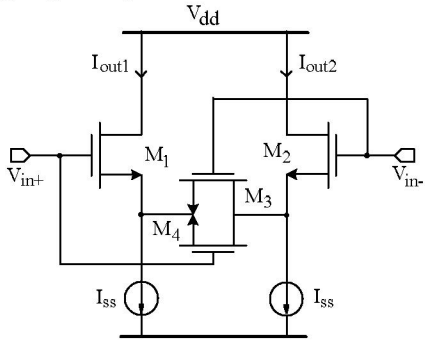

Fig. 2. Transconductor with source degeneration using MOS transistors [9]

$$G_m = \frac{4K_{n1}K_{n3}(V_{GS1}-V_{tn})\sqrt{I_{ss}}}{(4K_{n3}+K_{n1})\sqrt{K_{n1}}} \tag{3}$$

As can be seen in (3), the transconductance can be tuned by changing I_{ss}. However the nonlinearity is up to 1% for I_{out}/I_{ss}. In some filtering application it is required to have better linearity in order to achieve a total harmonic distortion (THD) of –60 dB or less [16]

Another topology to achieve highly linear MOS transconductance with low supply voltage is reported in [13]. The idea is to use class AB V-I linearization technique which is shown in Fig. 3. In this topology, the transistors M_3, M_4, M_5, M_6 are biased in triode region, therefore the voltage at drain of M_1, M_2 would be very close to supply voltage and the source voltage can be as low as several tens mV and can be neglected [13]. The transfer function is given by

$$I_{out} = I_{M7} - I_{M8} = \frac{K_n' K_n (V_{cm}-V_{tn})(V_{nl}-2V_{tn})}{2K_p(V_b'-V_{tp})} V_{id} \tag{4}$$

where K_n, K_n', K_p are transconductance parameter of NMOSs (M_1, M_2), (M_7, M_8), and PMOS (M_3, M_4), respectively. V_{tp} is threshold voltage of PMOS. $V_{id} = V_{in+} - V_{in-}$, $V_b' = V_{dd} - V_b$ $V_{nl} \approx V_1 + V_2 - 2V_{s,M_7,M_8}$, and $V_1 - V_2 = V_{d,M_3} - V_{d,M_4}$. As can be seen from (4) that the output current I_{out} is a function of the differential input voltage V_{id}. V_1 and V_2 are very close to V_{dd}, thus V_1+V_2 is almost constant and its nonlinear effect can be ignored. However, with the supply voltage lower than 2 V, the nonlinear term can be occurred [13]

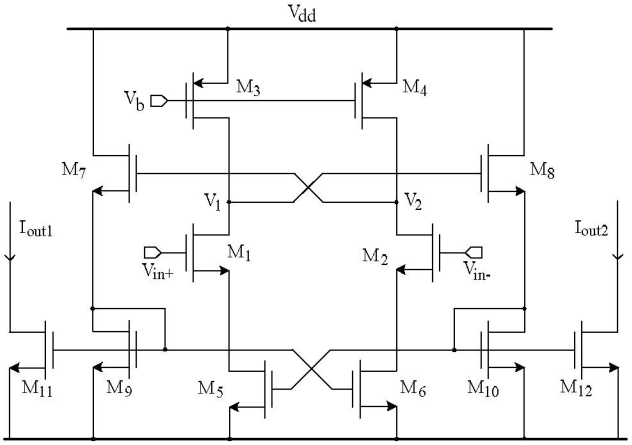

Fig. 3 Class AB Transconductor [13]

B. Proposed Transconductance Amplifier

As discussed in [13], when the supply voltage is reduced below 2V the nonlinear can be increased due to the value of $V_1 + V_2$ is not constant. In this design, since we use supply voltage of 1.25V, therefore, the nonlinearity becomes more significant. To resolve this problem, this paper proposes the new transconductor stage configuration that combines the two techniques discussed above: source degeneration using MOS transistor and class AB linearization. The proposed V-I circuit is shown in Fig. 4. In this topology, transistors M_3 – M_8 are operated in triode region. Now, the small-signal drain-source resistance of M_7, M_8 is given by [17]

$$r_{ds7} = r_{ds8} = \frac{1}{2K_{n7}(V_{GS1}-V_{tn})} \tag{5}$$

The small-signal source resistance of M_1, M_2 is

$$r_{s1} = r_{s2} = \frac{1}{2K_{n1}(V_{GS1} - V_{tn})} \quad (6)$$

In order to understand how the varying triode transistors help to improve the linearity of this circuit, let us start with a small differential input signal. Qualitatively, assume that if the amplitude of V_{in+} and V_{in-} is increased, which will reduce the value of V_1+V_2 (due to saturation in V_1 or V_2) therefore the value of V_1+V_2 is no longer constant for large input signal. From (4) as discussed before the nonlinear cannot be neglected. To alleviate this reduction for large input signals, the gates of M_7 and M_8 being connected to the input signals as shown in Fig. 4 can be helpful. Now as the input signal is increased, the small signal resistance of one of the two-triode transistors in parallel, M_7 or M_8 is reduced based on (5). This reduced resistance tends to boost the value of the V_1+V_2 resulting in a partial canceling of the V_1+V_2 reduction. Therefore we can conclude that by using two triode transistors M_7 and M_8, constant current through M_1 and M_2 will be forced. The constant current through M_1 and M_2 means the value of V_1+V_2 stays constant that will maintain the linearity range. Simulation results show that when the ratio K_1/K_7 = 5, the proposed topology will give the best linearity. In Fig.4, the V-I characteristic can be tuned by controlling the bias voltage, V_b, of the load transistors, M_3, M_4. Another advantage of this topology is that it is easily modified to have multiple outputs current by multiplying the size of transistor M_{13}, M_{14} while it does not affect the V-I conversion process

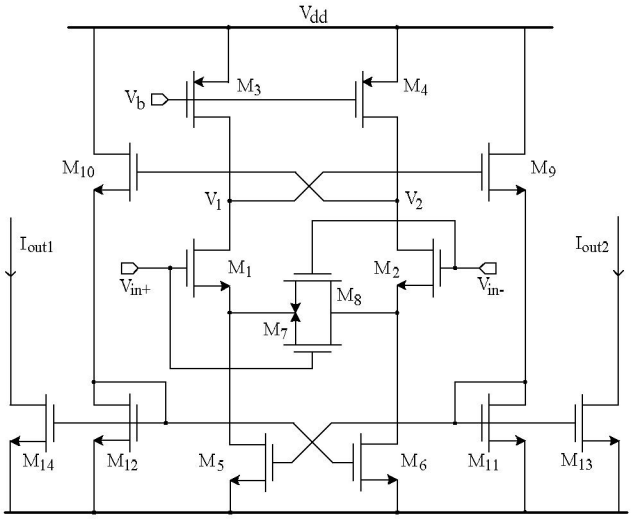

Fig. 4. Schematic of the proposed OTA

III. Results and Disscussions

In order to compare the performance of different linearization techniques, three circuits: transconductor using MOS degeneration, class AB transconductor, and the proposed transconductor are fabricated using the standard 0.25 μm CMOS process from TSMC. Measured output current as a function of the differential input voltage for three topologies are shown in Fig. 5. As can be seen in Fig. 5, the proposed circuit shows widely linear behavior over the full input voltage range (rail-to-rail) compare to all the other ones. The total harmonic distortion (THD) of the output differential current versus the amplitude of the input voltage for three topologies is plotted in Fig. 6. Once can be seen in Fig. 6, the proposed OTA achieves approximately -60 dB at 5 MHz for 0.6-Vpp differential input voltage. The obtained result is lower than other linearization techniques. The measured DC characteristics are shown in Fig. 7. The transconductance plot has been obtained by differentiating the measured output V-I characteristic. From Fig. 7 we can see that the transconductance of proposed OTA almost flattens in the input signal range. The microphotographs of three topologies are shown in Fig. 8. The active sire are of the proposed OTA is 0.1 mm^2.

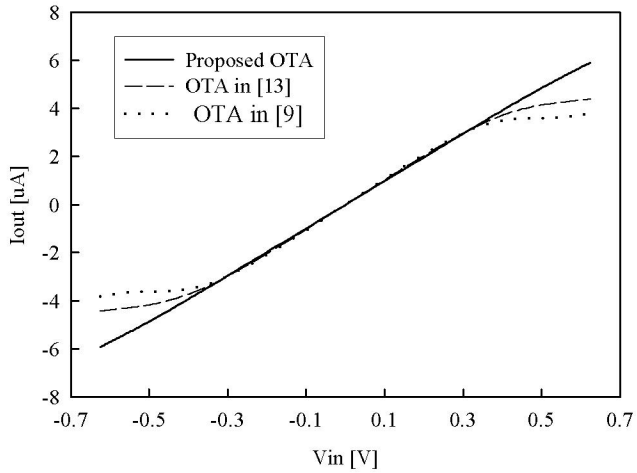

Fig. 6. The comparison measured V-I characteristic of OTA in [9], [13] and proposed OTA.

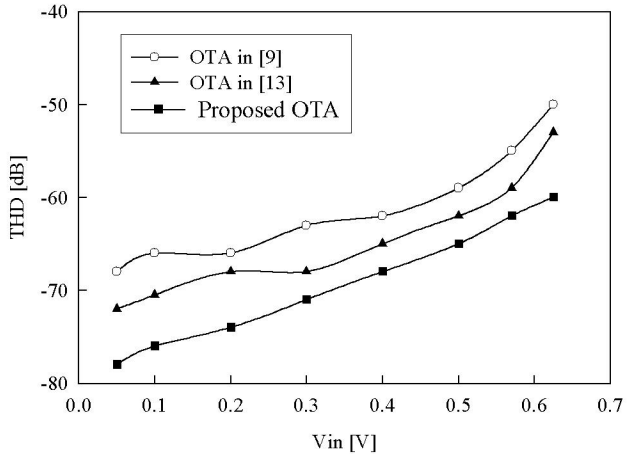

Fig. 7 The comparison measured THD of OTA in [9], [13], and proposed circuit

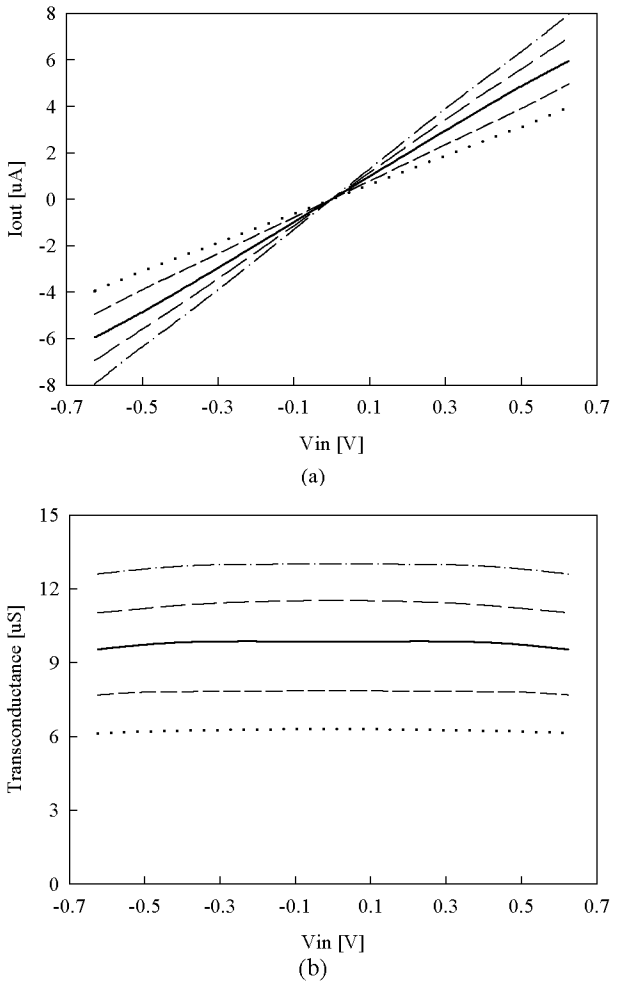

Fig. 8. Measured dc response of the proposed OTA: (a) V-I transfer characteristic, (b) transconductance

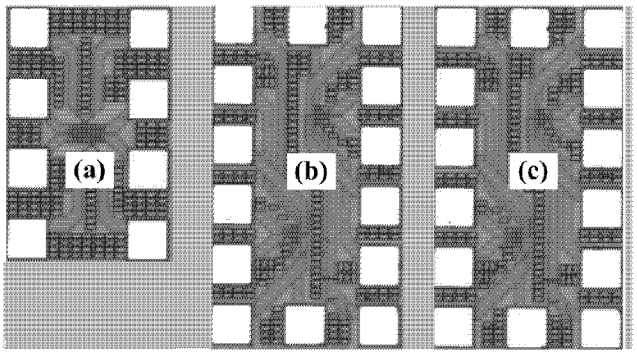

Fig. 5 Microphotograph of the fabricated OTAs: (a) OTA in [9], (b) OTA in [13] and (c) proposed OTA

IV. Conlusion

A new linear MOS transconductor, combining two linearization techniques has been presented. The topology can achieve rail-to-rail linear V-I transfer characteristic and it can be used in implementing fully differential G_m-C filter with severe linearity requirement. The proposed circuit has good tuning capability and lower THD compared to other approaches. The proposed OTA dissipates only 25 μW from 1.25 V supply.

Acknowledgment

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