A Sub-mA, High-Gain CMOS Low-Noise Amplifier for 2.4 GHz Applications

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***Abstract*— This paper presents a sub-mA, low-noise, high-gain CMOS low noise amplifier (LNA) for 2.4-GHz band applications based on 0.18 μm CMOS technology. Low-noise under power-constrained can be achieved by using an inductive cascode degeneration amplifier with an extra gate-source capacitor. Gain enhancement can be obtained by using capacitive feedback at the cascode transistor. Measurements show 16 dB gain, 1.8 dB NF, -10 dBm IIP3 while dissipating only 0.5 mA from 1.5 V supply.**

I. Introduction

With the introduction of IEEE 802.15.4 ZigBee standard [1], the demands for low cost, low power and small size wireless transceivers has been increased significantly. CMOS has become a competitive technology for radio transceiver implementation due to the technology scaling, higher level of integrability, lower cost, etc. [2]. In the typical radio receiver, LNA is one of the most critical blocks that determine the sensitivity of wireless receiver systems [3]. Consequently, LNA should contribute as low noise as possible. Not only that LNA should have a sufficient gain to suppress noise contributed by the subsequent stages. Besides, the input impedance of LNA need to be matched to 50 Ω. Generally, the goal of LNA design is to achieve noise and input matching simultaneously at any given amount of power dissipation. A number of LNA design techniques have been reported to satisfy these goals [4]-[6]. Typically, low-noise and high-gain LNAs require high power dissipation, which is not a desirable option with portable wireless system, especially with IEEE 802.15.4 standard. In this paper, LNA is designed to achieve simultaneous noise and input matching at very low current dissipation by introducing an extra gate-source capacitor at the input transistor of the cascode topology. Additionally, the power gain can be improved without any additional power dissipation by using a capacitive feedback at the cascode transistor. The detail analyses are shown in Section II. The proposed LNA is fabricated in a standard 0.18 μm CMOS technology. Measurement results show 16 dB power gain with stability factor greater than 1, 1.8 dB noise figure, -10 dBm IIP3, while dissipating 0.5 mA from 1.5 V supply.

II. Circuit Design

The proposed LNA shown in Fig. 1 adopts a conventional inductive degeneration cascode amplifier with the additional capacitors: a gate-source capacitor, C_{ex}, and a feedback capacitor C_f. The insertion of C_{ex} adds a degree of freedom to play with to achieve the noise figure equal to noise figure minimum of the given LNA topology under very low power dissipation. And the insertion of C_f will improve the power gain of amplifier without any DC current payment as can be explained later.

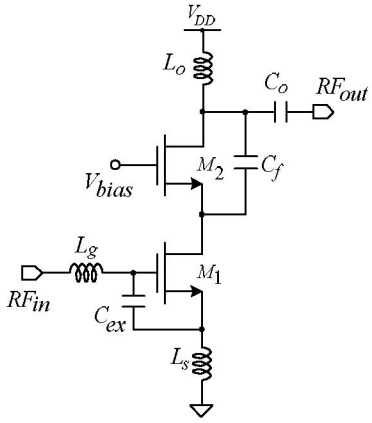

Fig. 1 Schematic of the high gain LNA

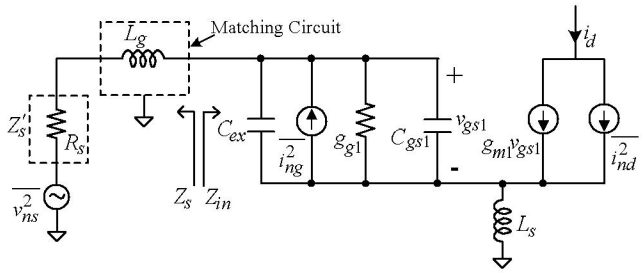

Fig. 2. Small signal equivalent circuit of the LNA for noise analysis.

To analysis the noise parameters of the proposed LNA, the small signal equivalent circuit shown in Fig. 2 is used. Typically, the noise figure, NF, of the LNA is dominated by the input state such that in Fig. 2, the effects of common-gate transistor M_2 on the NF of LNA are neglected [5], as well as

the parasitic resistances of gate, body, source, and drain terminals. The gate-drain capacitance of M_1 is also neglected [5]. The noise parameter expressions for a circuit with series feedback, shown in Fig. 2, can be obtained by applying the Kickoff's law [5]. The results are simple enough to provide useful insights as shown below .

$$F = 1 + \frac{1}{g_{m1}^2 R_s} \cdot \left\{ \gamma g_{d0} \cdot \left\{ \left[1 + s^2 C_t \left(L_g + L_s \right) \left(1 + |c| \alpha \sqrt{\frac{\delta_{eff}}{5\gamma}} \right) \right]^2 - \left(sC_t R_s \right)^2 \left(1 + |c| \alpha \sqrt{\frac{\delta_{eff}}{5\gamma}} \right)^2 \right\} - \frac{\alpha \delta_{eff}}{5} \left(1 - |c|^2 \right) g_{m1} \left(sC_t \right)^2 \left(R_s^2 - sL_g^2 \right) \right\} \quad (1)$$

$$F_{min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega_0}{\omega_{T1}} \sqrt{\gamma \delta \left(1 - |c|^2 \right)} \quad (2)$$

$$Z_{opt} = \frac{\alpha \sqrt{\frac{\delta}{5\gamma \left(1 - |c|^2 \right)}} + j \left(\frac{C_t}{C_{gs1}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)}{\omega C_{gs1} \left\{ \frac{\alpha^2 \delta}{5\gamma \left(1 - |c|^2 \right)} + \left(\frac{C_t}{C_{gs1}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\}} - sL_s \quad (3)$$

$$R_n = \frac{\gamma}{\alpha} \cdot \frac{1}{g_{m1}} \quad (4)$$

where $g_g = \frac{\omega_0^2 C_{gs1}^2}{5 g_{d0}}$, $\delta_{eff} = \delta . \left(\frac{C_{gs1}^2}{C_t^2} \right)$ and $C_t = C_{gs1} + C_{ex}$.

$2/3 \le \gamma \le 1$ for long channel, but for short channel γ is much greater than 2/3. δ is the coefficient of gate induced noise, equal to 4/3 for long channel devices [7]. ω_o is operating frequency. C_{gs1} and ω_{T1} are the gate-source and the cut-off frequency of the M_1. c is equal to 0.4 in the long-channel devices and increase as the technology scaling down [8].

Interestingly, as can be seen from (2) and (4), F_{min} and the noise resistance R_n are the same as those in [3]-[5] meaning that they are not affected by the addition of C_{ex}.

From Fig. 2, the input impedance of the LNA is given by

$$Z_{in} = sL_s + \frac{1}{sC_t} + \frac{g_{m1} L_s}{C_t} \quad (5)$$

As can be seen in (5), the source degeneration inductor, L_s, generates real part at the input impedance. This is important because there is no real part in the input impedance without degeneration while there is in the optimum noise impedance. Therefore, L_s helps to reduce the discrepancy between the real parts of the optimum noise impedance and the LNA input impedance. Furthermore, from (5), the imaginary part of Z_{in} is changed by sL_s, and this is followed by nearly the same change in Z_{opt} in (3), especially with advanced technology considering the value of c is higher than 0.4, and α becomes lower than 1 [8], [9].

Now, for the LNA circuit shown in Fig. 1, the condition that allows the simultaneous noise and input matching is

$$Z_{opt} = Z_{in}^* \quad (6)$$

From (3) and (5), (6) can be satisfied when the following conditions are met:

$$\frac{\alpha \sqrt{\frac{\delta}{5\gamma \left(1 - |c|^2 \right)}}}{\omega_0 C_{gs1} \left\{ \frac{\alpha^2 \delta}{5\gamma \left(1 - |c|^2 \right)} + \left(\frac{C_t}{C_{gs1}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\}} = \mathrm{Re}[Z_s] \quad (7)$$

$$\frac{j \left(\frac{C_t}{C_{gs1}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)}{\omega_0 C_{gs1} \left\{ \frac{\alpha^2 \delta}{5\gamma \left(1 - |c|^2 \right)} + \left(\frac{C_t}{C_{gs1}} + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\}} - sL_s = \mathrm{Im}[Z_s] \quad (8)$$

$$\frac{g_{m1} L_s}{C_t} = \mathrm{Re}[Z_s] \quad (9)$$

$$sL_s + \frac{1}{sC_t} = -\mathrm{Im}[Z_s] \quad (10)$$

As mentioned above, for the advanced CMOS technology parameters, (8) is approximately equal to (10). Therefore, (10) can be dropped, which means that for the given value of L_s, the imaginary value of the optimum noise impedance becomes approximately equal to that of the input impedance with opposite sign. Now, the design parameters that satisfy (7)-(9) are gate-source DC voltage of the transistor M_1, V_{GS1}, W_1 (or C_{gs1}), L_s, and C_{ex}. Since there are three equations and four unknowns, (7)-(9) can be solved for an arbitrary value of Z_s, by fixing the value of one of the design parameters, which is possibly the power dissipation or V_{GS1}. In other words by using this design optimization technique a LNA can achieve simultaneous noise and input matching at any given amount of power dissipation.

The limitation of the power-constrained simultaneous noise and input matching technique is high value of noise resistance and lower cut-off frequency. As can be seen in (4), the noise resistance, R_n, of the proposed topology is not affected by the addition of C_{ex}, but only the function of g_m. Therefore, the small transistor size and low power can lead to very high R_n. High R_n can be a serious limitation for the practical high yield LNA design therefore be careful when apply this technique. Considering the relationship between the cut-off frequency (f_T) and the total input capacitance, the addition of C_{ex} leads to power gain degradation. For example, if $C_{ex} = 3C_{gs}$, the f_T of LNA is expected to be

reduced by the factor of 4. This would lead to the reduction of the maximum oscillation frequency (f_{max}) by the factor of $\sqrt{2}$, 71%, due to the square-root functional dependence of the f_{max} on f_T. Therefore, it could be considered that the power gain is slow function of C_{ex}.

The qualitative description of the proposed design process would be as follows. First choose the DC bias, V_{GS1}, for example the bias point that provides minimum F_{min}. Then, choose the size of M_1, W_1, based on the power constraint, P_D. At this point, the value of Re[Z_{opt}] is determined. Now choose the additional capacitance, C_{ex}, as well as the degeneration inductance, L_s, to satisfy Re[Z_{opt}] = Re[Z_{in}]. The value of C_{ex} should be chosen considering the compromise between the size of L_s and the available power gain. As described before, large L_s can lead to the increase in F_{min}, while large C_{ex} leads to the gain reduction due to the degradation of the effective cut-off frequency of the composite transistor (transistor including C_{ex}). At this point, the simultaneous noise and input matching is achieved. As the last step, if there exists any mismatch between input impedance of the amplifier and the source impedance, an impedance matching circuit can be added. The limitations of this topology are high R_n due to low power consumption and low effective cut-off frequency. High R_n can be a serious limitation for the practical high yield LNA design.

In Fig. 1, the feedback capacitor C_f is used to enhance the gain of the amplifier. This configuration was described before [10] but, to the authors knowledge, never actual fabrication. The operation principle of the gain enhancement technique can be described as follows. The gain of a cascode LNA topology (without C_f) is given by [10]

$$A_v = G_{eff}\frac{1}{G_{total}} \tag{11}$$

where G_{eff} is the effective transconductance of amplifier and G_{total} is the total conductance at the drain of M_2 and is dominated by equivalent parallel conductance of the loading inductor, G_P, where G_p is given by

$$G_p = \frac{1}{Q_L^2 R_{Lo}} = \frac{R_{Lo}}{(\omega_0 L_o)^2} \tag{12}$$

where R_{Lo} and Q_L are the series resistance and the quality factor of the loading inductor L_o, respectively. From (11) and (12) the lower Q_L, the lower A_v is. Therefore, in order to have high gain G_{total} should be minimized. In this work, G_{total} is reduced by introducing the negative resistance, implemented by C_f, shown in Fig. 1, at the drain note of M_2. The conductance generated by C_f is given by

$$G_f = \frac{\omega_o^2 C_{gs2}\left(C_f + C_{gd2}\right)}{g_{m2}} \tag{13}$$

where C_{gs2}, C_{gd2} and g_{m2} are the gate-source, gate-drain and transconductance of the M_2 respectively. Now the total conductance at the drain of M_2 is given by

$$G_{total} = G_p - G_f \tag{14}$$

As can be seen from (14), by using C_f the G_{total} is reduced such that A_v is enhanced. Note that no additional active is used therefore no more DC power dissipated and no noise contributed. The limit to amount of feedback is governed by stability consideration. To ensure the stability condition, G_{total} must always positive or G_f cannot be greater than G_p.

III. Experimentail Results

The proposed LNA is optimized for 2.4 GHz ZigBee and fabricated in a standard 0.18 μm CMOS technology. Fig. 3 shows the measured S-parameters of the proposed LNA under power dissipation of 0.5 mA from 1.5 V supply. As can be seen in Fig. 3, the proposed LNA exhibits 16 dB gain, -19 dB S_{11}, and -18 dB S_{22} at the operating frequency. The NF and NF_{min} of the proposed LNA are measured by using *N8975A noise figure analyzer* and the obtained results are shown in Fig. 4. One can be seen in Fig. 4 that the proposed LNA achieves NF almost equal to NF_{min} meaning that the experimental results agree well with the theoretical analyses.

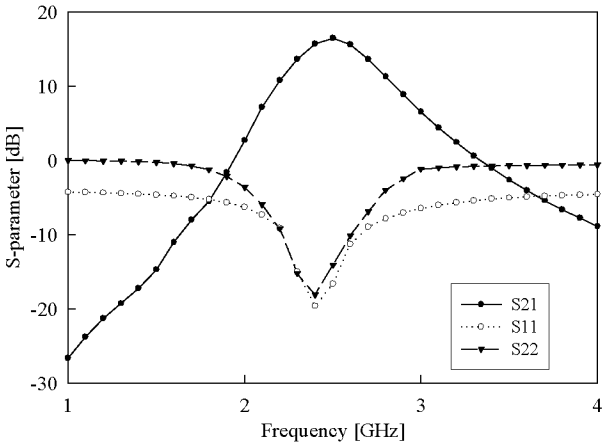

Fig. 3 Measured S-parameters of the proposed LNA

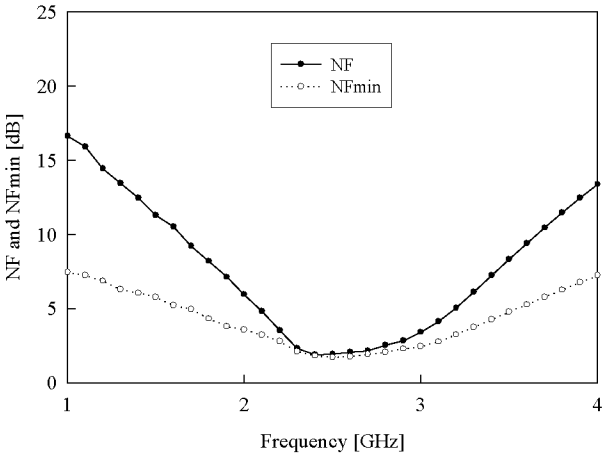

Fig. 4 Measured NF and NF_{min} of the proposed LNA

To estimate the linearity of the LNA, two signal sources at 2.4 GHz and 2.405 GHz with the same power are applied at the input port of the LNA. Fig. 5 shows the measured third-order nonlinearity (IIP3) of the proposed LNA As can be seen from Fig. 5, the obtained result of IIP3 is about -10 dBm. Fig. 6 shows the microphotograph of the fabricated LNA with a chip area of 0.76 mm^2. Table I summaries the measured performance of the proposed LNA.

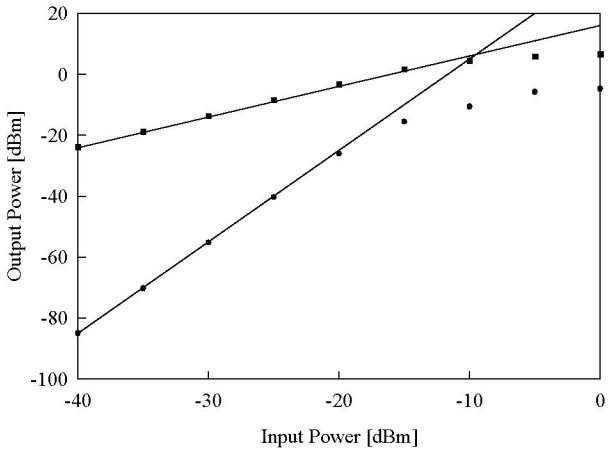

Fig. 5 Measured IIP3 of the proposed LNA

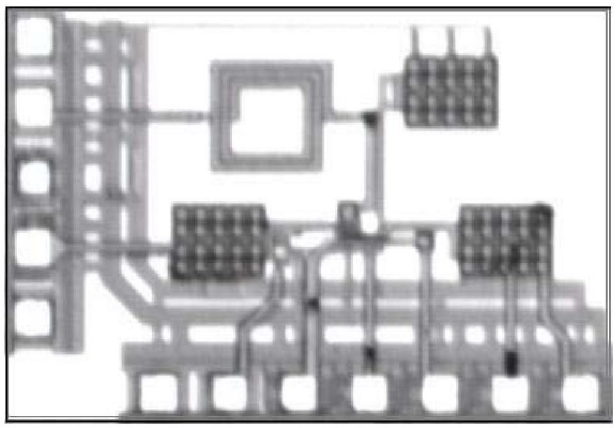

Fig. 6 Microphotograph of the proposed LNA

IV. Conclustion

A sub-mA, low-noise, high-gain LNA is designed for 2.4 GHz ZigBee applications based on 0.18 μm CMOS technology. Simultaneous noise and input matching under very low power consumption can be achieved by using an additional gate-source capacitor and the input transistor. The noise parameters of the LNA topology including C_{ex} have been derived to understand the insight of the noise design optimization. In additional, the power gain of the simple cascode topology can be enhanced by using an additional capacitive feedback at the cascode transistor. The proposed LNA is fabricated in a standard 0.18 μm CMOS technology. The measurement results show 16 dB gain, 1.8 dB NF, -10 dBm IIP3 and good input/output return losses while dissipating 0.5 mA from 1.5 V supply.

TABLE I. Summary Performacmes of The Proposed LNA

Parameters	Value
Operating frequency [GHz]	2.4
Power gain [dB]	16
NF [dB]	1.8
S11 and S22 [dB]	-19/-18
IIP3 [dBm]	-10
Input P-1dB [dBm]	-20
Current dissipation [mA]	0.5
Supply voltage	1.5
Technology [㎜]	0.18 CMOS

Acknowledgement

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