Gain Mismatch-Balanced I/Q Down-Conversion Mixer for UWB

Tuan-Anh Phan, Chang-Wan Kim, and Sang-Gug Lee
u-Radio Lab, Information and Communications University
119 Munjiro, Yuseong-gu, Daejeon 305- 714, Korea.
Email: anh@icu.ac.kr Tel: 82-42-866-6293

T.-J. Park, E.-J. Kim
Samsung Electro-Mechanics Co., Ltd
314, Maetan3-dong, Yeongtong-gu, Suwon, Gyunggi-do, 443-743 Korea.

***Abstract*—This paper presents an I/Q down conversion mixer in the receiver of ultra-wide band (UWB) systems with gain mismatch compensation capability by integrating the two PMOS variable gain amplifiers (VGA) at the output. The I/Q mixer is designed in 0.18 um Samsung CMOS technology. The proposed mixer operates at 1.584 GHz with the power conversion gain of 5.9 dB, IIP3 of 4.1 dB and NF of 7.9 dB. By adjusting the gain of VGA, the I and Q outputs perfectly have the same gain. LO-RF leakage is smaller than -72 dB. The designed mixer consumes total 11.5 mA from 1.8 V of supply voltage.**

I. INTRODUCTION

Ultra Wideband (UWB) system adopted by Federal Communication Commission (FCC) has emerged as an attractive future technology for wireless communications and local area networks. This is a short range, low power, high data rate and wide band wireless system [1]. With the bandwidth of 528 MHz and other characteristics, UWB transceivers have to meet the stringent requirements of 802.15.3a standard [2].

UWB spectrum is from 3.1 to 10.6 GHz, in the multi-band approach, this spectrum is divided into four groups. Group A, 3.1- 4.9 GHz, is intended for first generation devices, group B, 4,9 –6 GHz is reserved for future use, group C, 6.0-8.1 GHz is planed for devices with improved system on a chip (SOP) performance. The last group D, 8.1-10.6 GHz is also reserved for future use. In the first phase, our research group use only group A's spectrum which includes three bands, each band is 528MHz wide. Our approach for UWB transceivers is to use the dual conversion architecture, shown in Fig. 1.

This architecture has two frequency shifting stages, the first stage converts signal from three bands 3.432, 3.960 and 4.488 GHz to 1.056 -1.584 GHz band. The LO frequency is generated from sub-band generator (SBG) block, which generates three LO frequencies of 2.112, 2.640 and 3.168 GHz according to three bands. The output of the first mixing stage has center frequency of 1.32 GHz.

The I/Q direct down conversion mixer in this architecture is the second stage, the center operating frequency is chosen at 1.32 GHz for image reduction. The I/Q mixer translates the RF signal at the frequency band from 1.056 GHz-1.584 GHz to the base band signal.

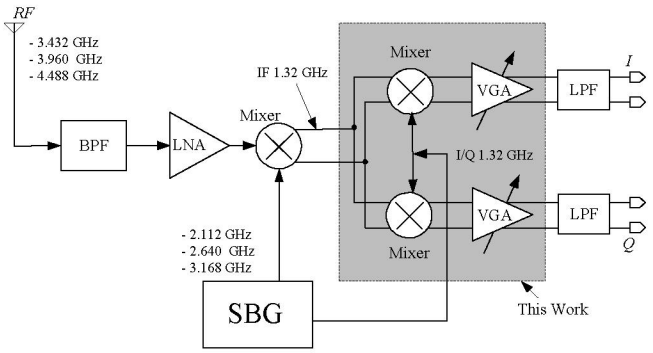

Figure 1. UWB architecture

In a quadrature system, a little mismatch in amplitude and phase between the I and Q channels is required. I/Q mismatch refers to phase and gain imbalances between in-phase (I) and quadrature (Q) paths. When the phase difference of LO signals for I and Q channels is not exactly 90 degree, phase imbalance occurs. Gain imbalance refers to gain mismatch along the I and Q signal paths.

The requirement for UWB system receiver is enough gain, high linearity and reasonable noise figure. The most important thing for maintaining high signal to noise ratio (SNR) is to reduce the signal degradation due to I and Q paths mismatch.

The I/Q mismatch corrupts the down-converted signals, causes the signal degradation, raising bit error rate. In this paper, we deal with the gain mismatch, which often and easily happens due to the gain mismatch of the blocks along the signal paths of I and Q channels.

To overcome the I/Q mismatch issues, there are several ways mentioned in previously published papers. Calibration

technique and careful layout [3], and digital techniques [4], [5] were introduced, but they are all complicated methods.

In this paper, our approach is to use a simple PMOS VGA at the output of I/Q mixer to control the gain mismatch of I and Q paths. Hence, the amplitude mismatch is overcome.

The core I/Q mixer has a modification that is to use a common transconductance stage. That helps increase the symmetry of the topology and simplify the circuit. The VGA is designed using PMOS transistor that avoid us using large capacitors between core I/Q mixer and VGA.

The I/Q mixer is designed and manufactured in 0.18 um Samsung CMOS technology. The measurement shows a good performance of the mixer, which is suitable for wide band application like UWB. The conversion gain is 6 dB, IIP3 of 4.1 dB, NF of 7.9 dB. The IQ mixer operates at 1.8 V and consumes 11.5 mA in total. The amplitude mismatch is completely overcome.

II. I/Q MIXER DESIGN

In order to perform the quadrature mixer, two Gilbert mixers are often required, they have the same RF input and quadratue LO.

The mismatch between the mixers will cause the imbalance of amplitude and phase in I and Q channels. The switching transistors operate like a switch so the effect of mismatch is negligible. On the contrary, I/Q error due to the mismatch of transconductance transistors is significant.

One of the major problem for the I/Q mixer is the mismatch, it degrades the signal to noise ratio (SNR) at the receiving ends. In this design, we are using one common transconductance stage for the I/Q mixer. With this change, the possibility of mismatch is reduced in the real circuit, further more it make the circuit simpler.

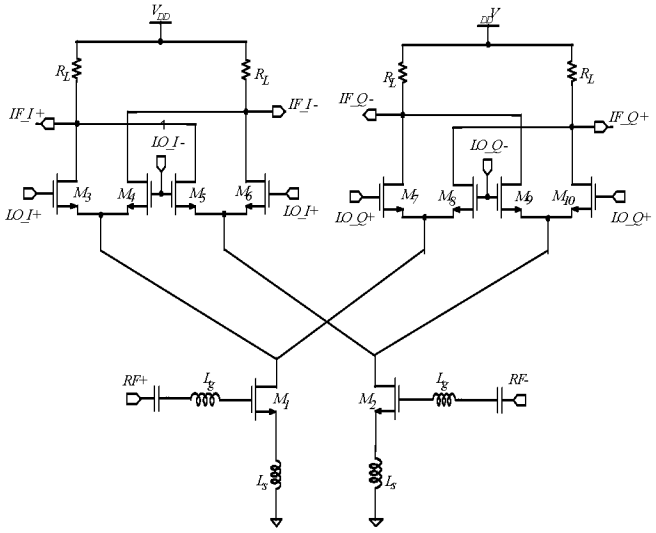

Figure 2. I/Q mixer schematic

In Fig 2, the core I/Q mixer is developed to minimize the mismatch of transconductance transistors. In this architecture [6], two Gilbert mixers use one common transconductance stage, therefore, there is no mismatch in transconductance transistors anymore since they are shared by both I and Q channels.

From [6], given the power consumption, same input capacitance and LO capacitance, this I/Q mixer has the same linearity as a pair of Gilbert mixers. However, it has a 3dB advantage of NF.

The load resistor is used, since it has no flicker noise and makes the circuit simple and wide band.

Inductors L_g and L_s are used for conjugate matching when connected with previous stage.

III. VGA DESIGN

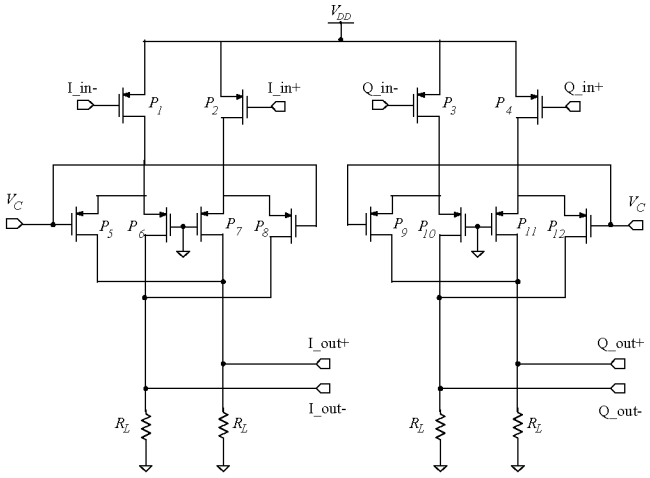

Figure 3. PMOS VGA schematic for I and Q channels

Our approach for I/Q amplitude mismatch correction is to balance the difference between output amplitudes of I and Q channels, hence VGA block plays an important role in this design.

In [7], the NMOS VGA is mentioned. That VGA can not be used in this design since we need large capacitors between core I/Q mixer and VGA blocks to separate the DC voltage of the two block when connected. Moreover, VGA works at IF, the down I/Q mixer output frequency, so the needed capacitors are relatively large.

Fig. 3 shows the proposed PMOS VGA. With the PMOS transistors, we don't need the capacitors when connecting the core I/Q mixer and VGA block. The PMOS VGA and core I/Q mixer is directed connected, but another challenging task is to design the PMOS VGA with high linearity, low power with given dc voltage from output of I/Q core mixer applied to the gate of input PMOS devices.

Transistor P_1-P_4 are the input devices, they connect to the I/Q mixer and convert voltage signal to current signal. The load resistor turns the current to voltage output signals.

The. P_5-P_{12} cooperatively control the gain of VGA, they are cross coupling PMOS transistors. $P_{6,7}$ and $P_{10,11}$ always connect their gate to the ground, in other word, they are always on. The control voltage V_c will control the operation of $P_{5,8}$ and $P_{9,12}$. If Vc is high enough, these transistors are turned off, the whole current signal flows to the load resistor. On the contrary, if V_c is low, these transistors are turned on, part of current signal is steered away from the main signal path, as a result, not all the current signal flows to output load. Hence the VGA gain is reduced and controllable.

By varying the value of control voltage V_c, the gain is linearly changed. The required gain controllable range is small, just a few dB. That is because, the function of this VGA is to adjust the output I/Q signal to compensate the mismatch caused by process variation, asymmetry of circuit designs.

IV. Results And Discussion

Fig. 4 shows the measurement result of I/Q mixer conversion gain. The RF input frequency is from 1.056-1.584 GHz, with LO frequency of 1.32 GHz. The bandwidth is larger than the required bandwidth of 264 MHz. The power conversion gain is 5.9 dB with 50 Ohm load. This gain is high enough for the requirement of the system. However, the gain ripple is more than 1 dB, which is the flatness requirement.

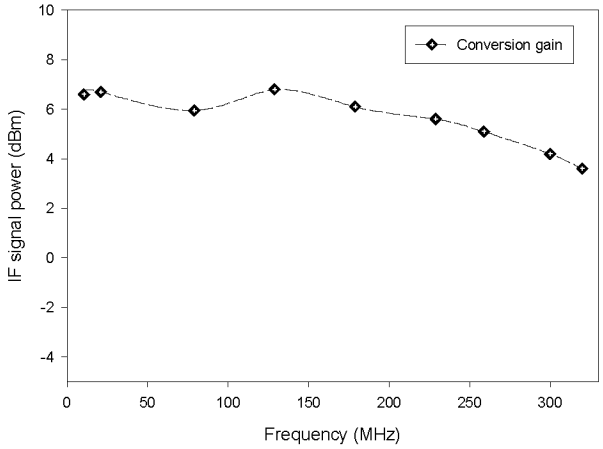

Figure 4. I/Q mixer conversion gain

The VGA block is also measured. The operating frequency is the output frequency (IF) of the core I/Q mixer, from base-band to 256 MHz. After calibration, we have the characteristic function of VGA as in Fig. 5. By changing the control voltage, the output gain is linearly changed. With two VGAs at the output of I and Q channels, the output gain of each channel is independently controlled. Hence, amplitude mismatch is cancelled. Since the gain mismatch between the two signal paths is at the order of a few dB, the controllable range of the designed VGA is from –15 to 2.1 dB, corresponding with the control voltage range from 0.2 to 0.43 V. This controllable range is far enough for the mismatch correction purpose. The VGA characteristic is close to that of the post simulation results.

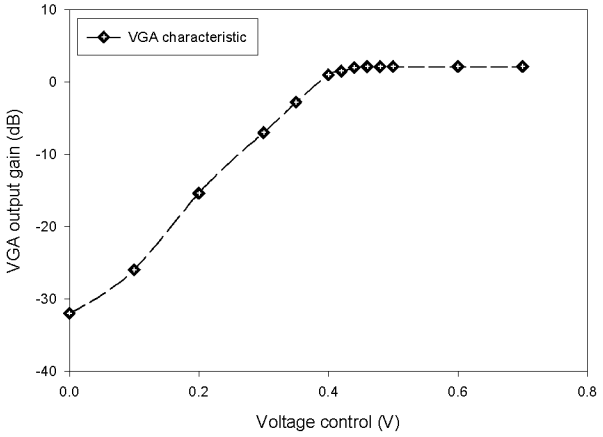

Figure 5. Characteristic of VGA gain versus voltage control

The two tones test results is shown in Fig. 6. Two tones at frequency of 264 MHz and 265 MHz are used at the input. The I/Q mixer shows a high linearity with IIP3 of 4.1 dB.

The DSB noise figure (NF) measured with the whole receiver is 7.9 dB while the design goal is 10 dB.

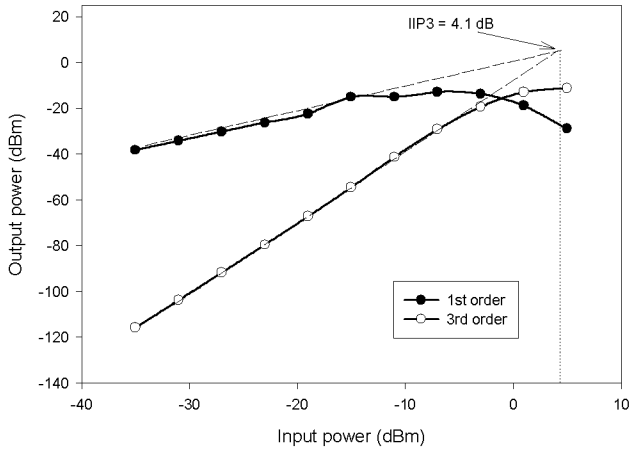

Figure 6. Mixer Input third order intercept point IIP3

Output waveforms of channel I and Q is shown in Fig. 7. These waveforms are obtained by running the transient of the extracted layout. Since the chip works closely to the post-simulation results, this form can be similar to the one on oscilloscope.

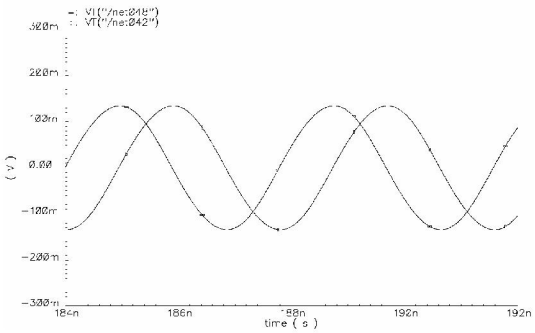

Figure 7. Wave forms of I and Q paths

The post-simulation shows phase error is 2 degree. By using VGA to control the gain, the amplitude imbalance is perfectly solved.

In Fig .8, the output spectrum of I/Q mixer is shown. The LO power is 0 dBm. The LO-RF leakage is –72 dB, the self-mixing of LO signal is quite small, leading to a good second order intercept point (IIP2).

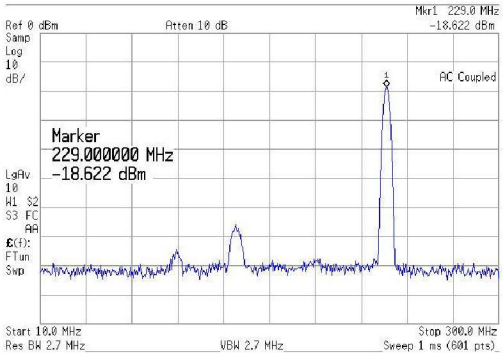

Figure 8. Measued I/Q mixer output signal spectrum

Fig. 9 is the die photo of the fabricated chip in 0.18µm CMOS Samsung technology.

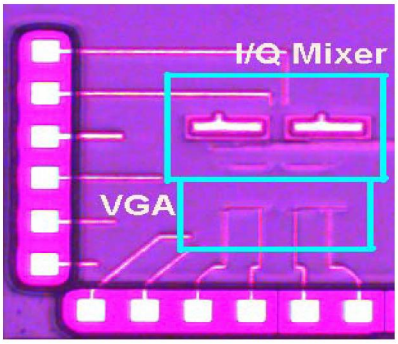

Figure 9. Microphotopraph of the fabricated I/Q down mixer with VGA

The I/Q mixer core chip size is 430µm x 360µm. This chip is part of the whole UWB receiver, in which the Sub-band generator (SBG) produces quadrature LO signals for I/Q mixer.

The I/Q down mixer consumes totally 11.5 mA from 1.8V of supply voltage, in which, the I/Q core mixer consumes 6 mA and 5.5 mA from VGA block. The I/Q mixer performance results are summarized in Table. 1. The performance is quite good to meet the system requirements.

TABLE I. I/Q MIXER PERFORMANCE TABLE

Parameters	Results
Input IP3 (dBm)	4.1
Power Conversion Gain (dB)	5.9
DSB NF (dB)	7.9
RF / LO frequency (GHz)	1.056-1.584 / 1.32
LO-RF leakage (dB)	-72
Supply Voltage (V)	1.8
Current Consumption (mA)	11.5

V. CONCLUSION

This paper described an I/Q direct down-conversion mixer for UWB with gain mismatch imbalance capability by integrating a PMOS VGA. The IQ mixer is designed and fabricated in Samsung 0.18µm CMOS technology. The designed IQ mixer operates frequency band from 1.056-1.584GHz, at 1.8V supply voltage and consumes totally 11.5mA. The measurement shows that conversion gain is 5.9 dB with band-with over 300 MHz which is suitable for wide-band application like UWB, IIP3 is 4.1 dB, LO-RF leakage is –72 dB with NF of 7.9 dB. The mismatch in I and Q path is perfectly overcome. This design demonstrates the soon appearance of UWB chip in the commercial markets.

ACKNOWLEDGEMENT

This work was supported by Samsung Electro-Mechanics Co., Ltd under SRC/ERC program of MOST/KOSEF (Intelligent Radio Engineering Center).

REFERENCES

[1] http://www.ieee802.0rg.15/pub/TG3a.html

[2] G. Roberto Aiello, "Challenges for Ultra-wideband (UWB) CMOS Integration," *IEEE IMS/RFIC Symposium*, Jun.2003.

[3] B. Razavi, "Design considerations for direct conversion receivers," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 428-435, June 1997.

[4] Li Yu and Snelgrove, W.M, " A novel adaptive mismatch cancellation system for quadrature IF radio receivers," *IEEE Trans. Circuits Syst. II* , vol. 46 , no. 6, pp. 789 – 801, June 1999.

[5] Iason Vasssiliou et al, " A Single-Chip Digitally Calibrated 5.15-5.85 GHz 0.18 um CMOS Tranceiver for802.1a wireless LAN," *IEEE JSSC*, vol. 38, No. 12, pp. 2221-2231, Dec 2003

[7] J. Harvey and R. Harjani, "Analysis and design of an integrated quadrature mixer with improved noise, gain and image rejection," *IEEE International Symposium on Circuits and Systems* (ISCAS), vol. 4, 6-9 May 2001

[8] Chunbing Guo and Luong, H.C,"A 70-MHz 70-dB-gain VGA with automatic continuous-time offset cancellation, " *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, vol. 1, 8-11 Aug.2000.