

# A 900 MHz CMOS RF Direct Conversion Receiver Front-end with 3-dB NF and 30-KHz 1/f Noise Corner

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**Abstract**—A low-power, low 1/f noise RF receiver front-end for 900 MHz IEEE 802.15.4 ZigBee standard in 0.18  $\mu\text{m}$  CMOS technology is implemented. In combination with LNA, a passive mixer showing excellent 1/f noise is adopted. The measured results show the conversion gain of 30 dB, NF of 3 dB with 1/f noise corner frequency of 30 KHz. Two-tone test measurements indicate -5 dBm IIP3, +45 dBm IIP2. The RF receiver front-end dissipates 2 mA from 1.8 V supply.

## I. INTRODUCTION

In the last few years, the demand for low cost, low power and small size wireless transceivers has been increased significantly with extensive researches on transceiver architectures and RF circuit design techniques utilizing standard CMOS technology [1]. Especially, with the introduction of IEEE 802.15.4 ZigBee standard, a low-rate, low-cost and low-power network [2], these demands tend to dominate the transceiver developments.

The direct conversion receiver (DCR) has attracted widespread attention recently for its simple architecture and easy integration with the baseband circuit, as well as for its low power consumption and potentially low manufacturing costs [3]. However, DCR has some disadvantages such as DC-offset, even-order distortion, flicker noise, I/Q mismatch, LO leakage etc [3], [4]. Recently, the DC-offset problem can be removed by using digital calibration [5] or the feedback  $-$ loop in the analog part [6], [7]. The even-order distortion and I/Q issues can be solved by careful layout and symmetric tracing of RF and LO paths or using digital calibration [8].

With the key point of low-power and low 1/f noise RF receiver front-end, the solution we are presenting is based on the low-power, low-noise LNA followed by passive mixer which shows very excellent 1/f noise. The measured results show the conversion gain of 30 dB, NF of 3 dB with 30 KHz 1/f noise corner frequency. Two-tone measurements show IIP3 of -5 dBm, IIP2 of +45 dBm and the gain variation of 10 dB. The overall RF receiver front-end dissipates 2 mA from 1.8 V supply.

## II. RF RECEIVER FRONT-END ARCHITECTURE

The proposed receiver architecture is shown in Fig. 1 which includes the low noise amplifier, down-conversion mixer, and

the baseband amplifier combination with first filtering circuit. In this configuration, direct down-conversion is implemented by passive mixers without DC current. By using this approach, the 1/f noise contribution from the mixers is made negligible. In this architecture, single-ended RF drive of double-balanced mixers is used, which allows single-ended RF gain circuitry and reduction of current consumption compared to differential one. The output of the low noise amplifier (LNA) is connected to one terminal of differential RF input of the mixer via coupling capacitor while the second terminal of the mixer is connected to AC ground. From the simulation result we have found that by using this approach the gain of overall RF front-end is reduced by 3 dB while taking fully advantages of the differential circuitry. The gain variable is adopted in the RF LNA in order to satisfy the linearity requirement since it operates at very low-power consumption. The baseband signal after down-conversion is amplified and filtered by the first baseband amplifier and filter circuit thus the linearity requirement of the following analog stages such as variable gain amplifier and low pass filter can be relaxed.

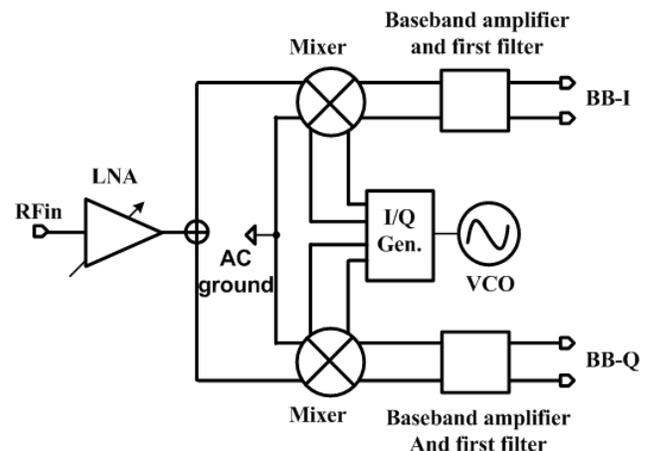


Fig. 1 RF receiver front-end architecture

## III. CIRCUIT DESIGN

### A. Low Noise Amplifier

The LNA has been designed to have a very low noise since it sets a lower bound for the total receiver sensitivity. Typically, an inductive degeneration cascode low noise amplifier topology is used widely since it provides high gain,

low noise, wideband, and high input/output isolation etc [9]. In this configuration, the inductive degeneration,  $L_s$ , is used to achieve simultaneous noise and input matching since  $L_s$  generates real part at the input impedance. This is important because there is no real part in the input impedance without degeneration while there is in the optimum noise impedance. Therefore,  $L_s$  helps to reduce the discrepancy between the real parts of the optimum noise impedance and the LNA input impedance. Furthermore, the imaginary part of input impedance is changed by  $j\omega L_s$ , and this is followed by nearly the same change in the optimum noise impedance, especially with advanced technology [10]. However, under low power consumption meaning that low gate-source overdrive voltage or small transconductance,  $g_m$ , the required  $L_s$  value that satisfies the simultaneous noise and input matching condition has to be very large. The problem is that for the  $L_s$  to be greater than some value, the minimum noise figure,  $NF_{min}$ , of a given technology increases significantly [11]. As a result, the minimum achievable noise figure,  $NF$ , of the LNA can be considerably higher than its  $NF_{min}$ , spoiling the idea of simultaneous noise and input matching. To overcome this problem the proposed LNA topology shown in Fig. 3 is used.

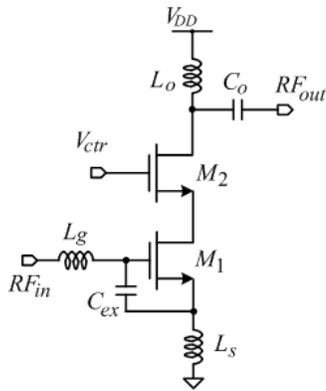


Fig. 2. Schematic of the proposed LNA

As can be seen in Fig. 2, the LNA differs by one additional capacitor  $C_{ex}$  in comparison with the typical cascode LNA. The insertion of this capacitance adds a degree of freedom to play with to achieve a simultaneous noise and input matching at very low power consumption. The bias voltage of transistor  $M_1$ , size of  $M_1$ ,  $L_s$ , and  $C_{ex}$  are chosen by applying the design procedure explained in [10] assuming the size of  $M_2$  is equal to  $M_1$ . The series gate inductor  $L_g$  is added to match the real value of input impedance to be  $50 \Omega$ . In this design, the degeneration inductor,  $L_s$ , is a combination of on-chip spiral inductor and wire-bonding while the gate inductor  $L_g$  uses off-chip one to reduce the series parasitic resistance at the input of LNA which helps to improve the noise performance of LNA further. The loading inductor  $L_o$  is implemented by on-chip inductor. In this LNA topology, gain variation can be obtained by changing the bias voltage of the cascode transistor,  $V_{ctr}$ . As the basic operating principle for CMOS transistor suggests, CMOS have high linearity with low gain in linear region and low linearity with high gain in saturation region. When  $V_{ctr}$  is in high-level

state two input transistor  $M_1, M_2$  remain in the deep saturation region and high gain is obtained. Since the input signal is very small, the distortion is relatively low. On the contrary, when the input signal is high and  $V_{ctr}$  is in low-level state, the input transistor  $M_1$  stays in linear region and low gain with low distortion can be obtained [12].

### B. Downconversion Mixer

High performance mixers in CMOS are either active based on current switching, or passive based on voltage switching mixers. In this design, as the way to minimize the power consumption, the passive mixer shown in Fig. 3 was chosen since it dissipates no DC current. The absence of DC current through the switches also makes it possible to eliminate the  $1/f$  noise, which otherwise is a problem especially for direct conversion receivers [4], [5]. Normally, NMOS transistors have better switch performance than PMOS transistors thanks to the higher mobility of electrons than holes [13]. Therefore NMOS transistors were chosen for the switch. In the Fig. 3, there are two parameters that designer can play with are the device's size and the LO characteristics.

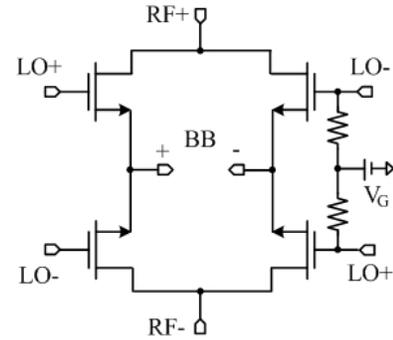


Fig.3. Schematic of the downmixer

In order to have low noise performance, the width of the transistor should be larger enough in order to provide a sufficiently low on-resistance. However, when sizing the switches there will be trade-off between the mixer noise performance and the gain of the LNA. The load impedance of the LNA consists of a parallel resonance circuit made up of the parasitic switch capacitance and the output inductor. If the switch capacitance is increased, the inductance must be decreased in order not to change the resonant frequency. The gain of LNA will then decrease due to the lower load impedance.

The characteristics of the LO signal will affect the mixer performance [14]. The DC level of the LO signal is important since it controls the switching mode. In the balanced drive case, equal amount of time in both on and off state, the voltage conversion gain is theoretically equal to  $2/\pi$ . If the switches are set to have less on-time than off-time, often referred to break-before-make, the conversion gain will maximally equal 1 [14], but the mixer will also be less linear. Thus there will also be a trade-off between the mixer conversion gain and linearity. In order to eliminate  $1/f$ , it is importance that transistors are biased at the condition where there is no DC current flowing

through the switch. In other words the source and drain terminals are bias at  $V_{CM}$ , while their gate voltage is

$$V_G = V_{CM} + V_{TH} \quad (1)$$

where  $V_{TH}$  is threshold voltage of transistors. It has been found from simulation that when  $V_G$  is around 1.4 V with  $V_{CM} = 900$  mV, this mixer topology shows  $1/f$ -free operation. The LO amplitude affects the mixer performances as well, and should be maximized. However, in this design, the LO amplitude of 0.5 dBm is applied considering the measured result of the fabricated VCO which is one of the parts in overall transceiver integration.

### C. Baseband Amplifier and Filter

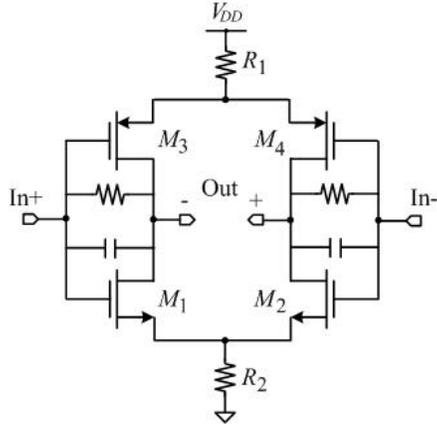


Fig. 4. Schematic of the baseband amplifier and first filter

The baseband amplifier and first filtering shown in Fig. 4 is implemented as a transimpedance amplifier with a RC-combination as feedback network. The bandwidth of this circuit can be controlled by capacitor; however, considering the bandwidth of ZigBee standard, the bandwidth of this circuit is 1 MHz, so that in a zero-IF configuration signals with a bandwidth of 2 MHz can be received. This circuitry not only provides the gain also filters the high order intermodulation products that affect the linearity of following stages. To improve linearity of circuit itself, the transistors have been degenerated resistively. From simulation we have found that  $1/f$  noise of the overall receiver front-end is mainly contributed by the first baseband amplifier and filter. In this design, the transistors were designed for a  $1/f$  noise corner frequency below 30 KHz considering 30 KHz cut-off frequency of the DC-offset feedback loop used in the variable gain amplifier, VGA, following the receiver front-end. From bit-error-rate (BER) simulation for ZigBee system we have found that with 30 KHz DC-offset the receiver needs just only 1 dB stronger signal power to have the same error performance. In other words, the  $1/f$  noise caused by the baseband amplifier is removed by using the DC-offset feedback [15] with the lower cut-off frequency of 30 KHz.

## IV. MEASUREMENT RESULTS

The RF receiver front-end with the EDS protection is fabricated in 0.18  $\mu\text{m}$  CMOS technology which is shown in

Fig. 5. It has an active area of  $1 \text{ mm}^2$  and consumes 2 mA from 1.8 V supply. The silicon area is mainly occupied by the baseband amplifier and filter circuit. The testing board has been built by directly bonding the die on a two-layer FR4 substrate. To supply differential signal at input LO port, a commercial passive balun has been used and 5 dB of balun loss according to its measurement has been de-embedded from the measurement.

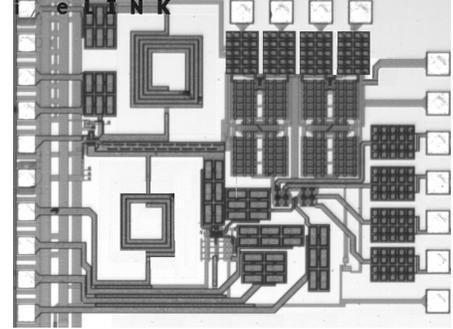


Fig. 5. Microphotograph of the fabricated chip

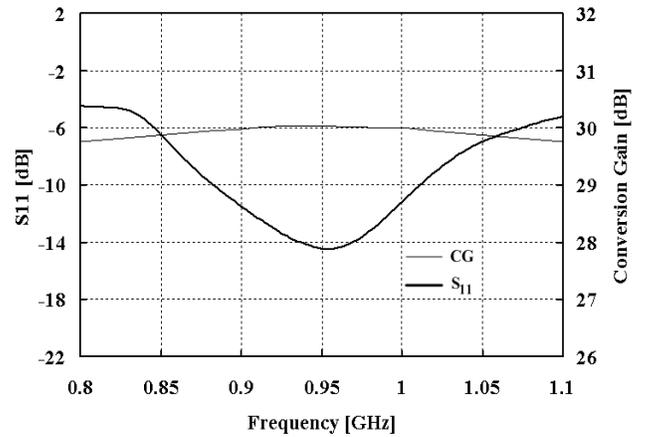


Fig. 6. Measured input return loss ( $S_{11}$ ) and conversion gain of the RF receiver front-end

Fig. 6 shows the measured input matching ( $S_{11}$ ) and conversion gain of the RF receiver front-end sweeping the local oscillator frequency across the entire target band (902-928 MHz). As can be seen in the Fig. 6, the input return loss of RF receiver is low than -13 dB and the conversion gain is about 30 dB and almost flat in all operating frequency band. The conversion gain variation is also performed. The result shows 10 dB gain variation by changing the gate bias voltage of the cascode transistor,  $V_{ctr}$ , in LNA shown in Fig. 2. Fig. 7 shows the measured DSB NF which is 3 dB in the center of the band. As can be seen from Fig. 7,  $1/f$  noise corner frequency appears at 30 KHz and which is caused by the baseband amplifier and filter circuitry as explained. However, as mentioned, this  $1/f$  noise is removed by DC-offset feedback loop used in analog baseband. The measured result is compromising with the simulated result. Fig. 8 shows the measured IIP3 result of the RF receiver front-end where two-tone signal spaced by 300 KHz are applied. The other properties such as IIP2, input P-1dB, LO-RF isolation of RF receiver front-end are also

measured. The overall measured performances are summarized in Table I.

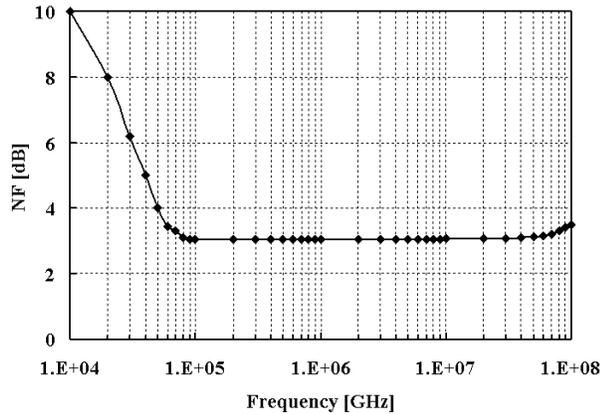


Fig. 7. Measured DSB NF of the RF receiver front-end

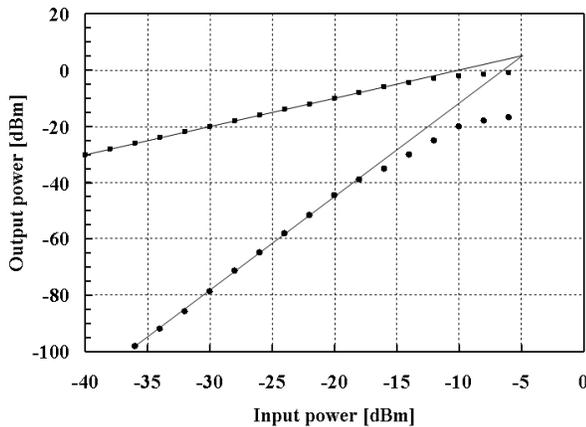


Fig. 8. Measured IIP3 of the RF receiver front-end

TABLE I

SUMMARY MEASUREMENT RESULTS OF RF RECEIVER FRONT-END

Parameters	Value
Operating frequency [MHz]	902-928
Conversion gain [dB]	30
Input return loss [dB]	-13
Gain variation [dB]	10
NF [dB]	3
1/f noise corner frequency [KHz]	30
IIP3/IIP2 [dBm]	-5/+45
Input P-1dB [dBm]	-15
LO-RF isolation	58
Current consumption [mA]	2
Supply voltage [V]	1.8
Technology [ $\mu\text{m}$ ]	CMOS 0.18

## V. CONCLUSIONS

A low-power, excellent 1/f RF receiver front-end for 900 MHz ZigBee applications has been designed and realized in 0.18  $\mu\text{m}$  CMOS technology. The simultaneous noise and input matching LNA design under low power consumption is obtained by using the conventional inductive degeneration

cascode amplifier topology with an extra gate-source capacitor. The passive mixer, showing excellent 1/f noise is adopted to convert RF signal directly to baseband frequency. The transimpedance with RC feedback network is used as the first baseband filter and amplifier. The measured results show conversion gain of 30 dB, IIP3 of -10 dBm, and IIP2 of +45 dBm. The measured NF is 3 dB with 1/f corner frequency of 30 KHz. The RF receiver front-end dissipates 3.6 mW from 1.8 V supply.

## ACKNOWLEDGMENT

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