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A 900 MHz Low Voltage Low Power Variable Gain CMOS Transmitter Front-end

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Abstract - **This paper presents a low-voltage, low-power, variable gain transmitter front-end for 900 MHz ZigBee applications, in a 0.25 μm CMOS technology. The up-mixer achieves a wide range-gain variation by adopting a novel transconductance stage. The measurements show the overall transmitter front-end conversion gain of 16 dB, dB-linear gain variation of over 46 dB with the linearity error less than ± 0.5 dB, output P-1dB of 2 dBm, while dissipating 3 mA from 1.25 V supply.**

I. Introduction

In the last few years, the demand for low cost, low power and small size wireless transceivers has been increased significantly with extensive researches on transceiver architectures and RF circuit design techniques utilizing standard CMOS technology [1], [2]. Especially, with the introduction of IEEE 802.15.4 ZigBee standard, a low-rate, low-cost and low-power network [3], these demands tend to dominate the transceiver developments.

In the architecture of high integration transceiver, the direct-conversion transmitter is one of the popular architecture where the off-chip IF filters and IF circuits are no longer necessary such that the power dissipation can be saved and easily implemented as a single-chip [4], [5].

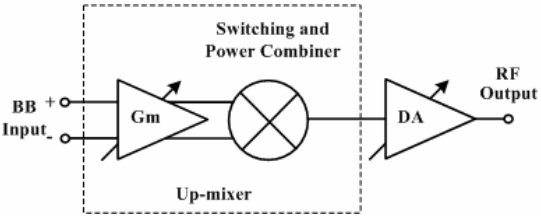

Fig. 1 The proposed RF transmitter front-end

This paper presents a CMOS direct-conversion transmitter front-end for 900 MHz ZigBee applications. The proposed transmitter architecture is shown in Fig. 1 which consists of a differential up-mixer followed by a single-ended driver amplifier (DA). The adoption of single-ended DA saves the power dissipation. However, a differential-to-single-ended conversion circuit following the up-mixer is needed. In Fig. 1, the differential signal is converted into a single-ended signal by using a passive power combiner. In Fig. 1, the up-mixer consists of fully differential variable transconductance stage followed by a switching stage. From the system simulation, in order to satisfy the 900 MHz band ZigBee standard, the transmitter front-end is designed for output P-1dB of greater than 2 dBm and output IIP3 of 12 dBm to transmit output power of 0 dBm without distortion. As the way to reduce the power dissipation, the proposed transmitter is designed for 1.25 V supply. The detail of circuit designs are described in the following sections.

II. Circuit Design

A. Up-mixer

The up-mixer is divided into three sections: a differential transconductance stage, switching stage and power combining circuit which are shown in Fig. 2-(a) and (b). As can be seen in Fig. 2-(a), circuit schematic wise, the variable trans-conductance stage combines the circuit techniques reported as "*Transconductor Using a Fixed-Bias Triode Transistor*" [6], [7] and the "*Source Degeneration Using MOS Transistors*" [8], the linearization techniques. However, in this design, the part of the circuits (transistors M_7 and M_8) that constitute the "*Source Degeneration Using MOS Transistors*" is used as gain control function. In Fig. 2-(a), for the given value of V_{ctr1} where the body-source and body-drain junctions of M_7 and M_8 are not forward biased, these transistors operate in the triode region, therefore they serve as degeneration resistor. Now as V_{ctr1} reduces low enough to forward-biased the body-source and body-drain junction of M_7 and M_8, some amount of DC current (I_3) from I_1 would bleed into V_{ctr1}. In this case, as will be described, the trans-conductance of the circuit shown in Fig. 2-(a) can be controlled as an exponential function of V_{ctr1} (gain-control mode), which allows dB-linear control of the overall mixer conversion gain.

Fig. 3 shows a simplified equivalent circuit schematic of the transconductance stage to explain the exponential dependence of the transconductance on V_{ctr1}. As shown in Fig. 3, under gain-control mode, the transistors M_7 and M_8 can be replaced by the diodes D_s and D_d. From Fig. 3, the output current of the transconductance stage, i_G is given by

$$i_G = I_1 - I_2 - I_3 \qquad (1)$$

And for the given differential input voltage v_{IN}, it can be shown that the output current i_G is given by

$$i_G = I_1 - I_2 - I_s \exp\left(\frac{-V_{ctr1} + V_{SG1} + v_{IN}/2}{V_T}\right) \quad (2)$$

where V_T is thermal voltage, V_{SG1} the DC source-gate voltage of M_1, I_s a constant. From (2), the transconductance (G_m) of the transconductance stage can be given by

$$G_m = \frac{\partial i_G}{\partial v_{IN}} = -\frac{I_s}{2V_T}\exp\left(\frac{-V_{ctr1} + V_{SG1} + v_{IN}/2}{V_T}\right) = K\exp\left(\frac{-V_{ctr1}}{V_T}\right) \quad (3)$$

where K is a constant. As can be seen in (3), the transconductance shows an exponential dependence on the control voltage, V_{ctr1}, which leads to dB-linear behavior of the mixer conversion gain. This newly proposed transconductance stage can be used for other general variable gain amplifier designs as well. Another advantage of this transconductance stage is that it can provide multiple outputs by simply adding more output transistors in parallel with M_5 and M_6. The additional outputs can be used for the design of I/Q mixer or active G_m-C filter with less transconductance stage which can save the power dissipation, an important property for low power design. In Fig. 2, the output current of the transconductance stage is multiplied by the switching pairs M_9-M_{10} and M_{11}-M_{12}, and the differential output signals are combined by the passive *L-C* combiner network [9].

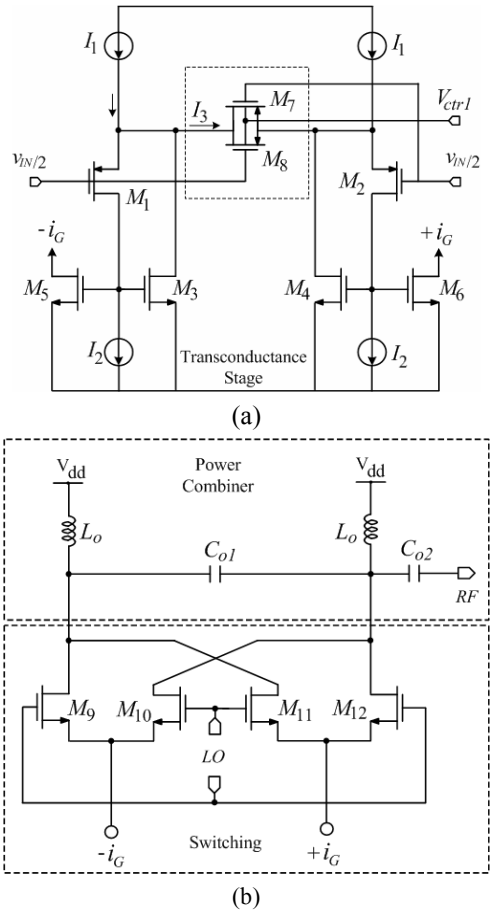

Fig. 2 Up-mixer circuit schematic (a) transconductance stage, (b) switching stage and power combiner

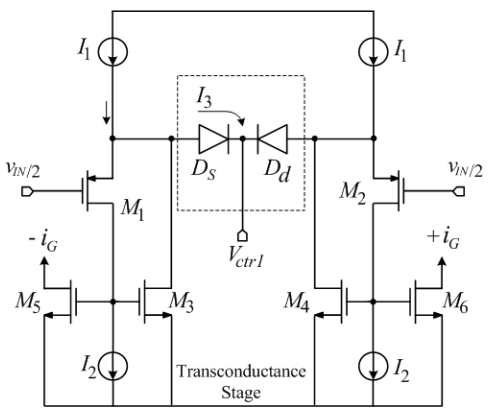

Fig. 3. Simplified equivalent circuit of the transconductance stage

B. Driver Amplifier

Driver amplifier precedes power amplifier. For high power transmit, the driver amplifier should have high gain and linearity [10]. In general, the conventional cascode amplifier can provide good linearity, but not suitable in this work due to the low supply voltage. The proposed driver amplifier shown in Fig. 4 is a single-ended folded-cascode topology. The folded-cascode topology is chosen due to the following reasons: i) folded-cascode structure allows higher voltage headroom which helps the linearity improvement, ii) gain can be controlled by varying the DC current of PMOS transistor by changing V_{ctr2} [11]. Moreover, the folded-cascode DA can be used for variable gain low noise amplifier as well since the gain variation occurs in the cascode transistor such that the noise and input matching conditions, which are dominated by the first transistor, are not affected.

In Fig. 4, the source degeneration inductor, L_s, is used to match the real part of the input impedance to the output impedance of the up-mixer to achieve maximum power transfer. In the Fig. 4, the additional capacitor, C_{ex}, is added to common-source transistor in order to keep the amplifier to operate in class-A mode while dissipating low DC current. As a linear amplifier, the class-A operation provides the best linearity [9]. The class-A operation implies that the dynamic output current should not exceed the bias current (I_D) at its maximum input power level (P_{in}). To achieve higher power efficiency it is also important that the current swing is maximized, i.e., output current swing is maximized when maximum input power is fed to DA. This means that the power-to-current gain of the input stage is fixed for a given bias current and maximum input power level. Therefore, the bias current needed to guarantee class-A operation is given by [12]

$$I_D = i_{d,peak} = \frac{f_t\sqrt{2P_{in}}}{f_o\sqrt{R_s}} \quad (4)$$

where Rs is the source resistance of the amplifier, ft the cut-off frequency of input transistor, fo the operating frequency.

Considering the low power objective of the given transmitter design, it is important to reduce the bias current I_D. From (4) it can be seen that, for the given level of input power P_{in}, to reduce I_D while keeping the input transistor in class-A operation, reducing f_t is the only solution as R_s is typically determined by the preceding stage (in this design it is equal to the output impedance of the up-mixer). This can only be done if another design parameter is introduced that decouples the relation between g_m and C_{gs}. A straightforward way of reducing f_t is to increase the transistor length L which reduces g_m and increases C_{gs}. Increasing L has undesirable effect of linearity degradation due to the quadratic I-V relation. Alternatively, a PMOS transistor, which have much lower f_t, can be used in the input stage. However, for a given amount of bias current, PMOS transistors provide lower transconductance which lead to lower gain of amplifier.

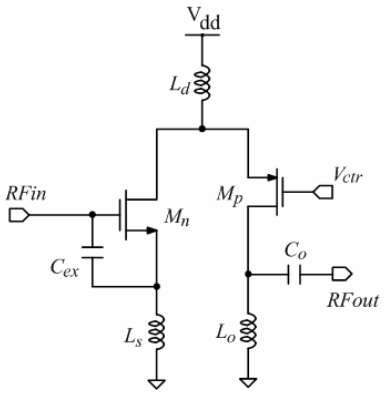

Fig. 4 Schematic of the driver amplifier

A third method is to add an external capacitor C_{ex} between the gate and source terminals of the input transistor. This way the effective f_t, $f_{t,eff}$ is reduced without reducing the intrinsic transistor f_t. Of course the reduction of effective f_t of the input transistor would lower the power gain. However, the power gain is a slow function of C_{ex}. For example, if $C_{ex} = 3C_{gs}$, the f_t of input transistor will be reduced by the factor of 4. This would lead to the reduction of the maximum oscillation frequency (f_{max}) by the factor of $\sqrt{2}$ due to the square-root functional dependence of the f_{max} on f_t. In this design, the method that used C_{ex} is chosen.

In Fig. 4, the parasitic capacitances at the drain node of the input transistor can easily be eliminated by the adoption of inductor L_d to the supply voltage. The elimination or the reductions of these parasitic capacitances help to avoid the signal loss into the silicon substrate, leading to better DA gain [13]. In Fig. 4, a simple L-C network using an off-chip inductor L_o and an on-chip capacitor C_o are used to match the output impedance of DA to 50Ω. The high-Q off-chip inductor L_o helps to improve the linearity further [14].

III. MEASUREMENT RESULTS

The proposed RF transmitter font-end was implemented in a 0.25 μm CMOS technology to dissipate 3 mA from 1.25 V supply. Fig. 5 shows the output spectrum of the transmitter front-end for the baseband input power of -16 dBm and an LO power of 0 dBm. In this measurement, 2 MHz of baseband input and 913 MHz of LO signal are applied. As can be seen in Fig. 5, the measured power conversion gain is 16 dB, LO suppression is 30 dB.

Fig. 6 shows the measured power conversion gain of the transmitter front-end versus V_{ctr1} (gain-control mode in transconductance stage). As can be seen in Fig. 6, the dB-linear gain variation of the proposed transmitter front-end is more than 46 dB with a linearity error less than ± 0.5 dB. To the authors' knowledge, this is the largest reported dB-linear gain variation implemented as a part of RF circuits. Fig. 7 shows the measured output 1-dB compression point of 2 dBm for the transmitter front-end at its highest gain. The two-tone test measurement shows 12 dBm OIP3. The obtained result satisfies the requirement from the system simulation. Fig. 8 shows the measured output return loss (S_{22}) of the transmitter front-end output, which shows lower than –14 dB at operating frequency. Fig. 9 shows the micro-photograph of the transmitter front-end chip and Table 1 summarizes the overall performances.

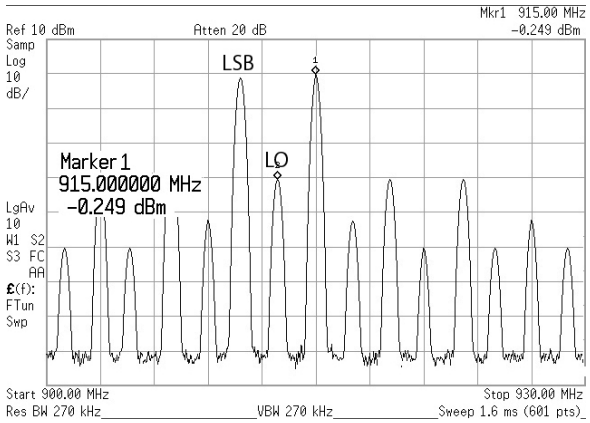

Fig. 5 Measured output spectrum of the transmitter at the -16 dBm input power

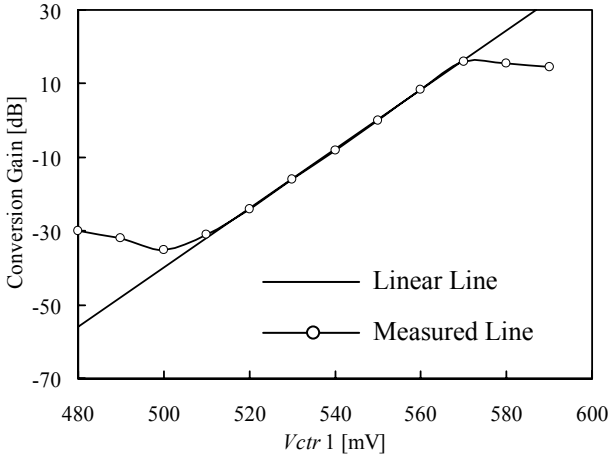

Fig. 6 Measured power conversion gain of transmitter front-end as function of V_{ctr1} of the upmixer

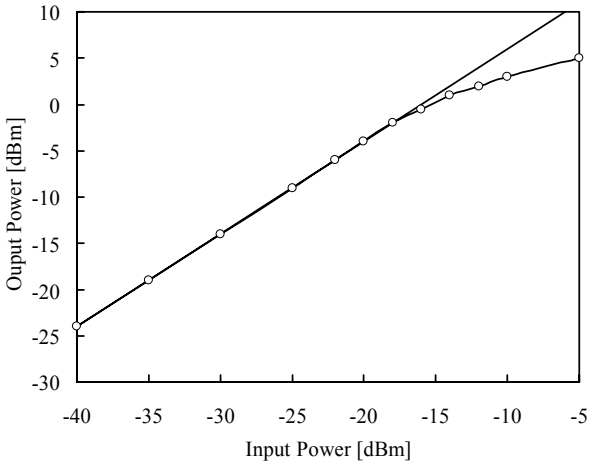

Fig.7 Output P-1dB of the transmitter front-end at the highest gain

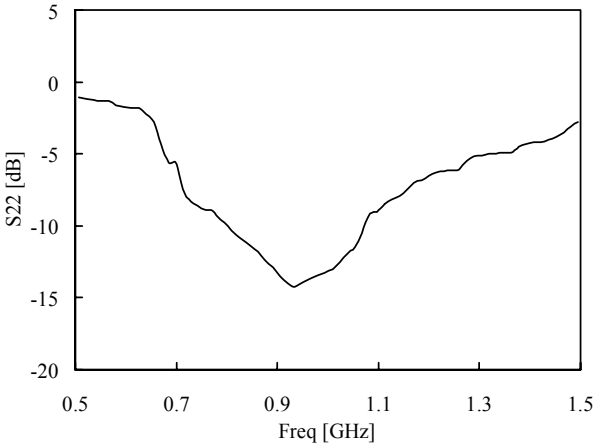

Fig. 8 Measured output return loss of the transmitter front-end

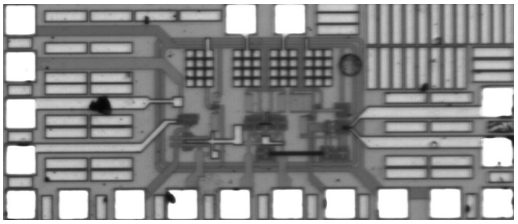

Fig. 9 Microphotograph of the transmitter front-end

Parameters	Value
Operation frequency [MHz]	900
Power conversion gain [dB]	16
Output P-1dB [dBm]	2 (at highest gain)
OIP3 [dBm]	12 (at highest gain)
Gain-range variation [dB]	> 46
LO suppression [dB]	30
Supply voltage [V]	1.25
Power consumption [mW]	3.75
Chip area [mm^2]	0.5
Technology [μm]	0.25 CMOS

TABLE 1 Summary of the measured 900 MHz transmitter front-end performances.

IV. CONCLUSION

This paper presents a low voltage low power variable gain direct conversion transmitter front-end for 900 MHz Zigbee applications. The up-mixer is designed for variable gain by adopting a novel transconductance stage. The operational principle of the proposed gain control circuit is analyzed. With the driver amplifier, high linearity is archived by adopting a folded cascode topology. By addition of an extra capacitor at the gate-source terminal of the input transistor, the driver amplifier achieves high 1-dB compression point while dissipating low power. The proposed transmitter front-end is implemented in a 0.25 μm CMOS technology. Measurements show the total power conversion gain of 16 dB, output P-1dB of 2 dBm, dB-linear gain-range of 46 dB with the linearity less than ± 0.5 dB. The overall transmitter front-end dissipates 3 mA from 1.25 V supply and occupies 0.5 mm^2 of silicon area.

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