P2-21

A Direct Conversion CMOS Front-End for 2.4 GHz Band of IEEE 802.15.4 Standard

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Abstract— **Design description and measurement results of 0.18 µm CMOS direct conversion receiver front-end intended for use in a transceiver for 2.4 GHz band of 802.15.4 standard are presented. Front-end consists of LNA and two current-mode passive mixers. Single-ended RF drive of double-balanced I/Q mixers was used as a means of power dissipation reduction. The measurement showed the following performance: noise figure 7.3 dB, 1/f-noise corner 70 kHz, power gain 10 dB, input IP3 –8 dBm with DC current dissipation of 3.5 mA while operating from voltage supply of 1.8 V.**

I. INTRODUCTION

In the recent years, the concepts of intelligent interactive environment and ubiquitous radio access has asked for the whole complex of new solutions at all levels of organization of wireless communication systems: from the development of new standards to the hardware architectures and circuit solutions. The goal is low-power, small size and low-cost transceivers. Requirements of low cost and close integration with digital circuitry dictate the usage of CMOS IC processes for RF and analog parts of transceiver. At the same time, while pursuing toward low-cost low-power transceiver for low data-rates, direct conversion architecture is the natural selection.

In the area of home and industrial automation, IEEE 802.15.4 standard is expected to become a dominant technology. This article presents design description and measurement results of 0.18 µm CMOS direct conversion receiver front-end intended for use in transceiver for 2.4 GHz band of 802.15.4 standard.

II. DESIGN DESCRIPTION

A. Front-end architecture

Direct down-conversion is implemented by passive I/Q mixers without DC current. Compared to active current-communicating mixers, passive mixer flicker-noise contribution is negligible. Therefore, by this approach, the flicker-noise issue of direct-conversion architecture is eliminated, at least when it comes to RF blocks. As a way to decrease power consumption in a low data rate system, single-ended RF drive of double-balanced mixers is used. This allows single-ended RF gain circuitry and reduction of current consumption compared to differential one. Second terminal of differential RF input of the mixers is AC-grounded through capacitor. The LNA is a cascode with inductive loading. Additional MIM capacitor is connected between source and gate of common-source transistor in order to facilitate input matching.

One may argue that with single-ended RF current drive of the double-balanced switching stage, its operation principle is reduced to that of single-balanced one. Therefore, it might look like if single-ended RF drive is selected, double-balanced mixer should not be used, since its advantages over single-balanced one disappear, while single-balanced mixer can provide better noise performance due to smaller number of switching transistor used. In order to test this guess, simulation with passive version of single-balanced switching core was performed. As a result, single-balanced mixer core showed much higher 1/f corner frequency. One possible explanation of this behavior is as follows. It was appreciated in literature that 1/f noise appears in a passive mixer due to non-zero time varying drain-source voltage induced by local oscillator (LO) through capacitive coupling [1]. In double-balanced switching core, this LO coupling can be cancelled out more efficiently due to higher circuit symmetry compared to single-balanced switching core. While detailed analysis of the 1/f-noise origins in passive mixers is being currently attempted by authors, double-balanced mixer topology was selected based on mentioned considerations and simulation results.

As for the usage of passive mixer in a way most beneficial for linearity, two opposite opinions were published. In [2], authors suggested using high-impedance loading for the passive mixer in order to decrease current flowing through the nonlinear drain-source resistance of the

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switching transistors in on-state, thus decreasing nonlinear distortion and improving linearity. In this mode the mixer operates as a voltage switch. Nevertheless, the authors noticed that as amplitudes of RF and down-converted signal grow, voltage swing at RF and base-band ports starts to modulate the switching instances of the mixer, thus introducing additional distortion.

Authors of another approach, called current-mode of passive mixer operation, suggested eliminating this voltage swing by synthesizing low-impedance at the output of the mixer, in which case the down-converted signal is accepted by the base-band in the form of current [3,4]. Reduction of the voltage swing at RF and base-band ports proved to be effective for linearity improvement. The later approach was selected for this design.

I/Q mixers operate in current domain: both driven from one LNA (which acts as a transconductance stage), while driving the low-impedance loading, which is the input impedance of the trans-impedance amplifier (TIA). Thus, the overall voltage gain of the front-end is composed of transconductance gain of the LNA, 6 dB20 current division between I and Q mixers, mixer's current conversion gain, and trans-impedance gain of the TIA. The architecture of the resulting front-end is shown in Fig.1.

B. Trans-impedance amplifier

Low input impedance and current-to-voltage conversion function of the first base-band stage are implemented by inclosing differential operational amplifier (OP-amp) in shunt-shunt feedback. TIA consists of two stages: gain stage and buffer. Gain stage is a differential inverter composed of large devices in order to minimize flicker-noise, Fig.2. Self-biased inverter also sets the quiescent output voltage of TIA, and therefore biases the input of subsequent base-band stages, which should be used with given front-end. The gain of the TIA is determined by the feedback resistance and is equal to 2 kOhm.

Receiver gain budget and selected supply voltage of 1.8 V imposed a number of issues in TIA design.

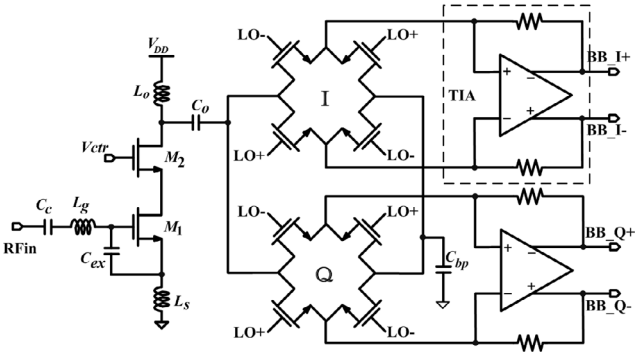

Figure 1. Front-end architecture.

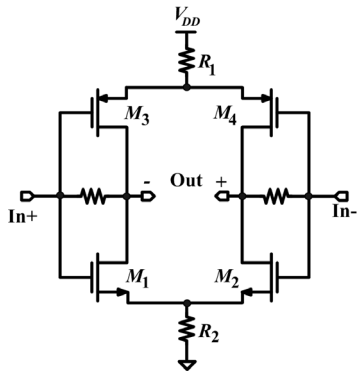

Figure 2. First stage of the OP-amp used for TIA synthesis.

For TIA stability and sufficient loaded gain, two stages architecture was selected: gain stage and buffer. Since the first stage is inverter, buffer has to be non-inverting amplifier. Also, TIA must operate with equal input and output quiescent voltages. They in turn were set to $V_{DD} / 2 = 0.9$ V to maximize the voltage swing that inverter and subsequent base-band circuits can handle.

Under this conditions, and taking into account requirements for the voltage swing, simple source follower cannot be used as the buffer due to V_{GS} level shift associated with it. An OP-amp in unity-gain feedback operates without level shifting and therefore can satisfy all the requirements for the buffer. The architecture of the TIA therefore looks like shown in Fig.3.

For OP-amp in unity-gain feedback, the requirement for output voltage swing automatically translates to the requirement of common-mode voltage swing. Therefore, OP-amps of wide-common-mode-swing topology were used as output buffers to prevent nonlinear distortions at a high input power levels, Fig.4.

Implementing the buffers without voltage level shift allows alleviating voltage headroom constraint and maintaining unified supply voltage of 1.8 V throughout the device, as opposed to similar front-end implementation in [3,4], where trans-impedance amplifiers operate from supply voltage of 2.5 V, which is higher then that of RF blocks.

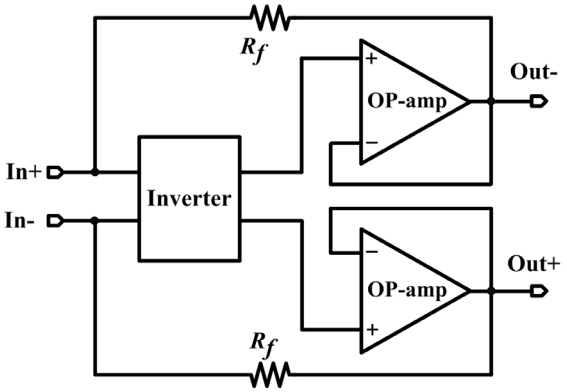

Figure 3. TIA block diagram.

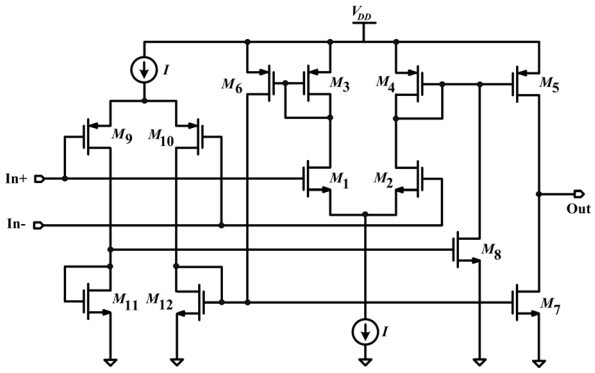

Figure 4. Schematic of the OP-amp used as TIA output buffers.

III. MEASUREMENT RESULTS

Front-end noise figure (NF) at base-band frequencies was measured with the aid of spectrum analyzer following the method described for example in [5].

Measured front-end performance is summarized in Table 1. Note that final stage of signal processing takes place at base-band frequency, therefore, reported value of NF reflects not only RF circuitry noise performance, but also 1/f-noise contribution of the first base-band stage, which becomes dominant while using 1/f-noise-free passive mixers.

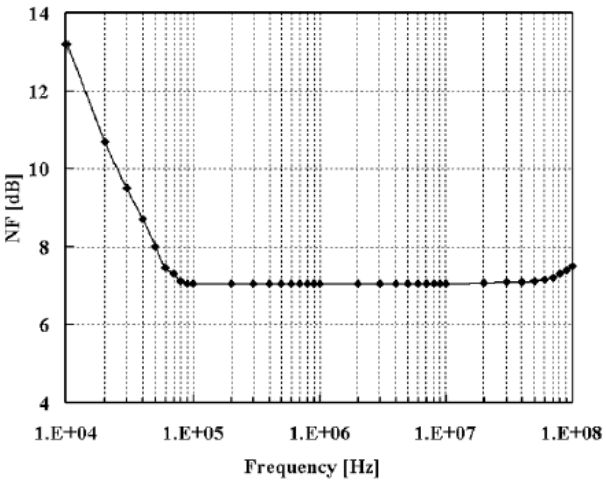

Figure 5. Front-end noise figure versus frequency.

TABLE I. MEASURED FRONT-END PERFORMANCE

Parameter	Value
Double-side-band NF (at frequencies higher then 1/f-noise corner)	7.3 dB
1/f-noise corner frequency	70 kHz
Power gain (with 50 Ohm load)	10 dB
Input-referred IP3	–8 dBm
DC current consumption	3.5 mA
Device area (including bond-pads)	1.66 x 1.25 mm^2

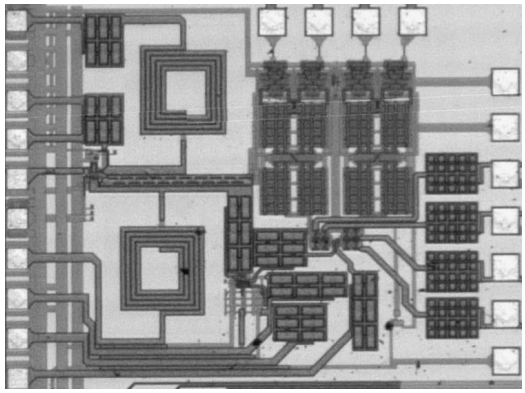

Figure 6. Chip microphotograph.

IV. CONCLUSIONS

An RF front-end intended for applications in 2.4 GHz IEEE 802.15.4 transceiver was designed in 0.18 µm CMOS technology. Single-ended RF drive of double-balanced I/Q mixers was used as a means of power dissipation reduction. Passive mixers resolve the 1/f-noise issue of direct conversion architecture, while current-mode of mixers' operation preserves linearity. This design differs from similar one [4] by the fact that unified supply voltage of 1.8 V is maintained for both RF and base-band circuitry thanks to usage of OP-amp-based buffers without level shifting. This property is vital if integration in a mobile low-power system is required.

ACKNOWLEDGMENT

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