2.5 A CMOS Burst-Mode TIA with Step AGC and Selective Internally Created Reset for 1.25Gb/s EPON

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The burst-mode TIA (BM-TIA) in the burst-mode receiver (BM-RX) requires reset after a strong burst to avoid inter-burst interference, thereby having fast response and high loud/soft ratio, as defined in [4]. Therefore, the BM-TIA for EPON system that does not provide any reset signal needs an internal reset-generation mechanism. Unlike the single-chip BM-RX in [1], the BM-TIA with limited gain cannot generate reset for every burst. Moreover, the BM-TIA has size constraint to enable integration with photodiode (PD) in a TO-can for best sensitivity. To address this issue, a selective internal reset mechanism for BM-TIA, where reset is only generated after strong bursts, is proposed. In conjunction with step AGC method, the BM-TIA achieves high dynamic range, full-swing loud/soft ratio that is equal to the dynamic range, and fast response. Most importantly, the BM-TIA handles burst-mode signal recovery by itself and can be AC-coupled with a normal limiting amplifier to make a BM-RX module. The BM-TIA exceeds 20km EPON specification by only using an inexpensive PIN photodiode.

Figure 2.5.1 shows the block diagram of the BM-TIA. The core TIA block converts input current from the PD to single-ended output voltage which is then converted to differential outputs matched to 50Ω using feedforward topology [1]. Particularly, the bottom-hold (BH) circuit [1] detects and holds the negative peak of the core TIA output. The dummy TIA that has the same circuit as the core TIA generates a reference voltage called the dark level. The dark level is equal to the output voltage of the core TIA when there is no input signal. By a 1:1 resistive divider between the BH and the dark levels, the DC level of the core TIA output is detected and fed to the single-to-differential converter (S2D) which is a differential amplifier, resulting in symmetric differential outputs with small offset. The top-hold circuit in [1] is replaced by the dummy TIA to reduce the chip size.

The feedback network of the core TIA, shown in Fig. 2.5.1, consists of R_1 and R_2 resistors, SW switch, and C_{FB} capacitor. By turning on or off the switch, the feedback resistance is either R_2 or $R_1 + R_2$, setting the core TIA to low- or high-gain modes, respectively. The BH level reflects the input signal level. Before each burst, the AGC signal is LOW and the core TIA is at high gain. At the beginning of a burst, if the detected BH level is lower than V_{ref_AGC}, i.e., high power burst, the AGC comparator in Fig. 2.5.1 turns AGC signal to HIGH, which switches the core TIA to low gain mode and shrinks the core TIA output swing. After the AGC switching, the logic control circuit generates an AGC internal reset pulse for the BH circuit to detect the new BH level of the shrunk output, thereby keeping S2D conversion accurate. The AGC signal waveforms are shown in Fig. 2.5.2.

The EOB reset signal is needed to reset the logic-control and BH circuits to initial states so that the core TIA is at high gain and BH circuit can detect BH level of the coming burst. Without reset, the detected BH level in Fig. 2.5.1 is the negative peak of the core TIA output of the strongest burst in the system, making an offset at S2D inputs of weak bursts. A system with only low-power bursts does not need the reset signal as the offset is small and cannot saturate the S2D while the AC-coupling cancels the offset at the input of the limiting amplfier. Therefore, the EOB reset signal is only required after high-power bursts.

At the beginning of a burst, BH level is detected and compared to V_{ref_ENBL}. In case of a high-power burst, i.e., the BH level is lower than V_{ref_ENBL}, reset-enable comparator output is HIGH to enable the reset generation after that burst. Capacitor C_E and resistor R_E form a low-pass filter producing V_{mid} that tracks the DC level of the core TIA output. With the resistive divider ratio in Fig. 2.5.1, the burst-based reference level, $V_{1/4}$, is lower than dark level by 1/4 of output swing of the core TIA. During burst period, V_{mid} is always lower than $V_{1/4}$. After the burst, V_{mid} rises up toward dark level, passing $V_{1/4}$, and sets the output of the reset comparator to HIGH. This makes the logic-control block generate a short EOB reset pulse. As both V_{mid} and $V_{1/4}$ are relative to burst amplitude, the discharge time required for V_{mid} to pass $V_{1/4}$ is short and independent from the burst power. After EOB reset, BH level is close to dark level because there is no signal at that time, so reset enable is turned to LOW, avoiding any more reset being generated until the next high-power burst comes in. If the burst has low power such that the BH level is not low enough to turn on the reset-enable signal, reset is not generated. Calculations of V_{ref_ENBL} and S2D gain are needed to make sure the weak burst offset does not saturate the S2D. Internal reset generation waveforms are depicted in Fig. 2.5.3. The reset signal for BH (Fig. 2.5.1) also closes switch SW_E that shorts V_{mid} to the core TIA output. This reset removes the effect of AGC and/or previous burst on V_{mid}, allowing for quick and precise detection of V_{mid} . The core TIA output swing after AGC is controlled to guarantee EOB reset generation. The logic-control block uses some timers and latches to maintain smooth AGC and accurate reset generation.

The burst-mode TIA chip is fabricated in a mixed-mode 1P6M 0.18μm CMOS process with all components on-chip, and assembled with a die PIN PD inside a TO- can to make a PIN-TIA module. The PD has 0.5pF intrinsic parasitic capacitance and 0.9A/W responsivity. The PIN-TIA module is AC-coupled to a commercial limiting amplifier to make a BM-RX module. The Agilent ParBERT 81250 parallel BER tester is used to evaluate burst-mode performance of the receiver module at 1.25Gb/s with BER<10^{-12} and 2^5 - 1 PRBS pattern which is suitable for EPON with 8B/10B line code. The worst case with alternative sequence of strong and long bursts from one optical network unit (ONU) and weak and short bursts from the other ONU is used in all the BER tests [4]. The extinction ratios of the ONUs are >8dB.

The measured waveform at the BM-RX module output showing quick recovery of signals in the worst case is depicted in Fig. 2.5.4. Guard time and preamble time are both 100ns. The BM-TIA shows -31dBm sensitivity, -4dBm overload, and an advantageous full-swing loud/soft ratio of 27dB. The chip performance along with comparisons with other EPON receivers are shown in Fig. 2.5.5.

The chip micrograph and typical eye diagrams at BM-RX module output are shown in Fig. 2.5.6. The chip size is 1.1×0.9mm^2 with full-chip ESD protection.

References:

[1] Q. Le, S. G. Lee, Y. H. Oh, et al., "A Burst-Mode Receiver for 1.25Gb/s Ethernet PON with AGC and Internally Created Reset Signal," *IEEE J. Solid-States Circuits,* vol. 39, no. 12, pp. 2379-2388, Dec., 2004.
[2] K. Nishimura, H. Kimura, M. Wantanabe, et al., "A 1.25Gb/s CMOS Burst-Mode Optical Transceiver for Ethernet PON System," *IEEE J. Solid-States Circuits*, vol. 40, no. 4, pp. 1027-1034, Apr., 2005.
[3] M. Nakamura, Y. Imai, Y. Umeda, et al., "1.25Gb/s Burst-Mode Receiver ICs with Quick Response for PON Systems," *IEEE J. Solid-States Circuits*, vol. 40, no 12, pp. 2680-2688, Dec., 2005.
[4] J. M. Baek, J. W. Kwon, J. W. Park, et al., "Low-Cost and High-Performance APD Burst-Mode Receiver Employing Commercial TIA for 1.25Gb/s EPON," *IEEE Photonics Technology Letters*, vol. 17, no. 10, pp. 2170-2172, Oct., 2005.

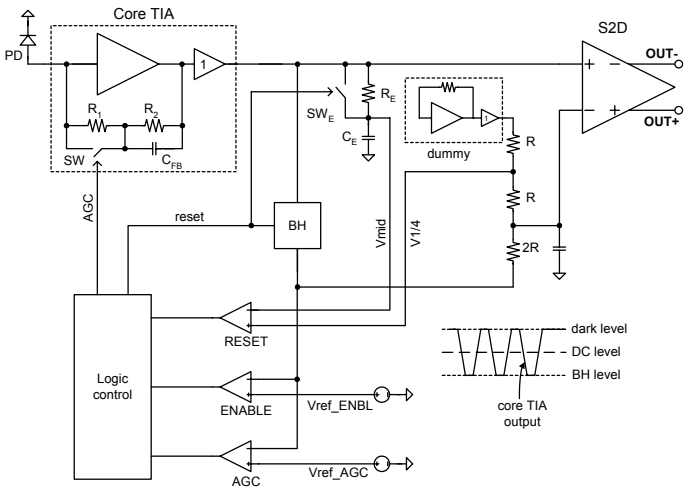

Figure 2.5.1: BM-TIA block diagram.

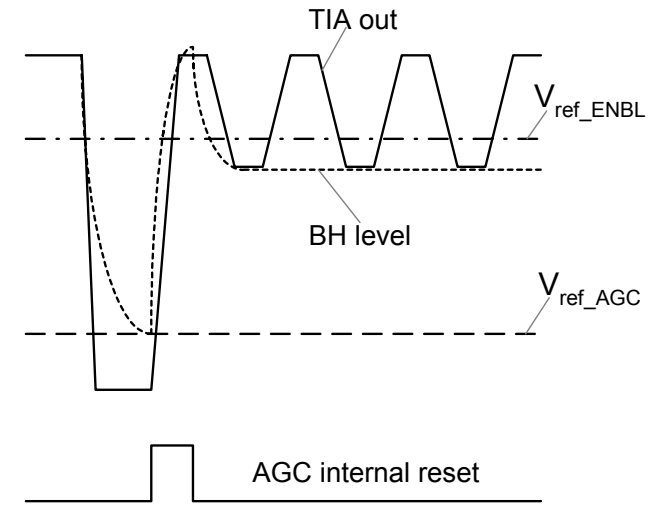

Figure 2.5.2: AGC operation waveform.

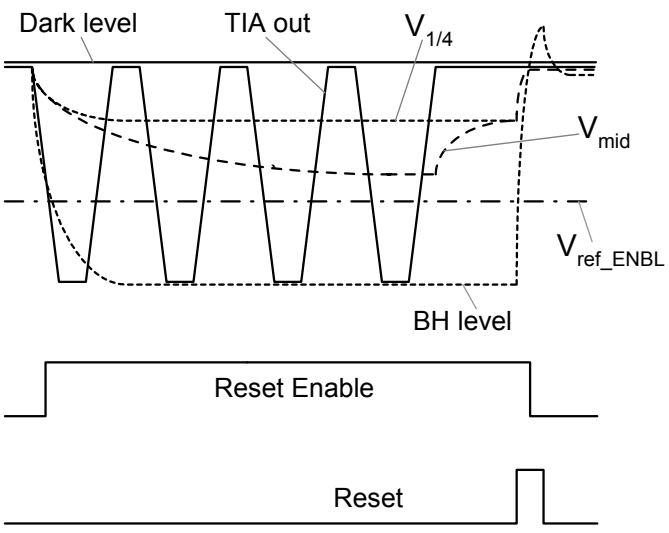

Figure 2.5.3: Internal reset generation waveform.

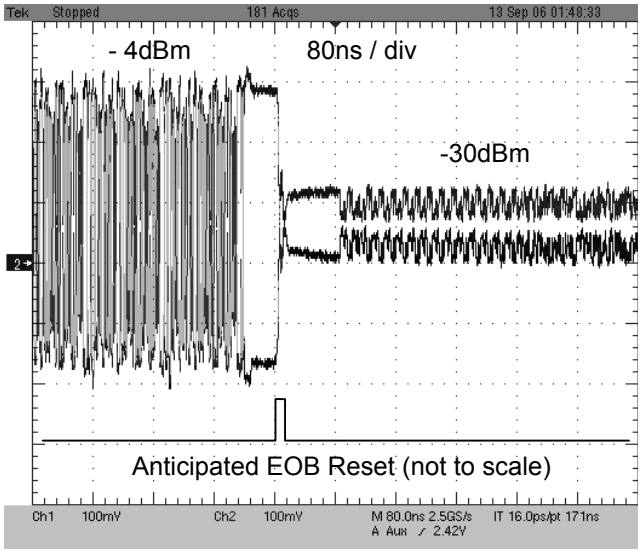

Figure 2.5.4: Measured waveform of BM-TIA outputs with 26dB loud/soft ratio.

	Standard EPON	[1] EPON	[2] GPON	[3] GPON	**This work EPON**
Sensitivity (dBm)	-27	-26.5	-29	-30	**-31**
Overload (dBm)	-6	-5.5	-2.2	-4	**-4**
Loud/soft ratio (dB)		21	26.8	26	**27**
Guard time	400ns	250ns	25,6ns	25.6ns	**100ns**
Preamble time	512ns	120ns		16ns	**100ns**
Reset		**Internal**	External	External	**Internal**
Module		One-chip	BM-TIA & BM-LA	BM-TIA & BM-LA	**BM-TIA & CW-LA**
Process		CMOS 0.18μm	CMOS 0.25μm	SiGe 0.25μm	**CMOS 0.18μm**

Figure 2.5.5: Performance comparison.

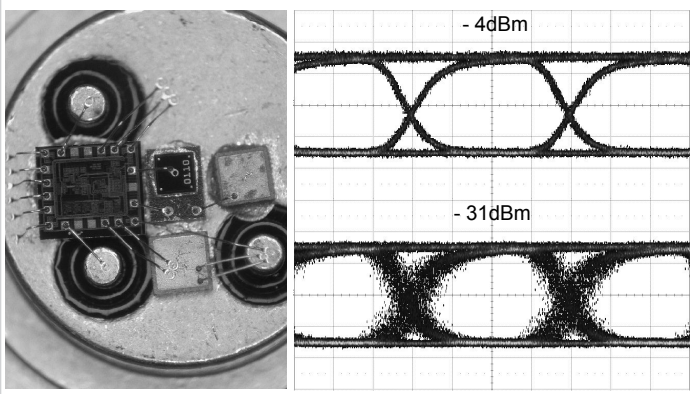

Figure 2.5.6: PIN-TIA assembly and typical BM-RX module eye diagrams.