Highly Linear CMOS Low Noise Amplifier with IIP3 Boosting Technique

Abdul Mujeeb, Sigit Yuwono, Jeong Seon Lee and Sang-Gug Lee
μ-Radio Lab, Information and Communications University
Daejeon, South Korea
mujeeb@icu.ac.kr

Abstract— **A High Linear technique for the (CMOS) low noise amplifier (LNA) is presented, the proposed method uses an additional PMOS transistor for IIP3 boosting the third order intermodulation distortion (IMD3) current generated by the CS and CG stages ;However, reducing the gain and increasing noise figure, this technique is applied to achieve the linearity of CMOS LNA using 0.18 μm technology .The LNA achieved +14 dBm IIP3, 12 dB gain, and 1.2 dB NF at 2.4 GHz, consuming 8.2 mA from 1.8 V supply .**

Keywords- CMOS, LNA, PMOS IIP3 boosting technique.

I. INTRODUCTION

LNAs are widely used in wireless communications. They can be found in almost all RF and microwave receivers in commercial applications such as cordless telephones, cellular phones, wireless local area networks, and satellite uplinks and downlinks. Low noise amplifiers (LNAs) are usually placed at the front-end of a receiver system, immediately following the antenna. The purpose of a LNA is to boost the desired signal power while adding as little noise and distortion as possible.

LNAs can be fabricated using many techniques, such as, Bipolar, CMOS, BiCMOS, etc. Although CMOS is the technology of choice in term of digital integration, it is seldom preferred for high performance LNAs due to its limited ability to handle interferences. The CMOS technology enables the successful design of a high gain and low noise CMOS LNA with low power consumption.

A CMOS LNA design using CMOS technology presents considerable challenge due to its simultaneous requirement for high gain, low noise figure, good input, and output matching, and unconditional stability at the lowest possible current draw from the amplifier; however, the linearity has not benefited by the evolution of the device technology, which has motivated several linearization techniques [1]. Until now, the most efficient linearization method for a CMOS LNA has been the derivative superposition (DS) technique [2]. This method nulls the negative third-order derivative of the main field-effect transistor's(FET's) dc transfer characteristic(g_3) by paralleling the auxiliary FET biased near the weak inversion region with multiple gated transistor (MGTR)method [1] to the modified DS method. Despite the outstanding improvements in the quality factor (Q) of input matching network which plays a main role for Low noise optimization [4]. This paper presents a low-power, low-noise, high Linearity, high gain LNA designs for 2.4 GHz WLAN application. In this design a conventional cascade LNA structure is used with an IP3 boosting technique to increase linearity. In the following simple explanation and analysis are given to explain how the folded cascade PMOS acts. At the end, simulation results using 0.18 μm CMOS technology will be presented.

II. THEORY OF PMOS IIP3 BOOSTING METHOD

In order to overcome the challenges of LNAs design, high linearity, high gain, low noise, and low power etc. many state of the art techniques and topologies for LNA have been researched and applied. Some of those are really good at high performance with low power dissipation requirement, and an IP3 boosting technique to increase linearity. Thus it is possible to achieve low noise, low distortion, and low Power consumption simultaneously. In the traditional cascode LNA design, no matching has been considered between the common-source stage and the common-gate stage. This is not desirable for the maximum power transfer loss of the power directly affects the noise performance of the LNA, since both the input impedance of the common-gate stage. In the cascode amplifier the drain current of the CS FET can be expressed in terms of gate–source voltage v_{gs} using the power-series expansion [2].

$$i_d = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + ..., \quad (1)$$

Where g_i is the ith-order derivative of the dc transfer characteristic the third-order nonlinearity of the CS FET is a major source of IMD3, Since the CG FET in the cascode amplifier operates as a current buffer, and the nonlinear current generated in the CS FET is fully transferred to the CG FET. If the source node of the CG FET has an additional current path which selectively absorbs the IMD3 current component, only the fundamental current component can be delivered to the output. The concept of IMD sinking is simple but the practical implementation is not easy due to the difficulty of separating the fundamental, and the IMD3 current [1]. Here, we show that an additional cascode PMOS FET can nearly work as IIP3 booster. Fig. 1(a) shows the proposed circuit. The resulting output current I_{sA} in Fig. 1(a) can be expressed as the sum of I_{sB} and I_{sC}. When the nonlinearity is approximated to the third-order, I_{sB} and I_{sC} can be expressed

$$i_{sA} = g_{1A} v_{gs} + g_{2A} v_{gs}^2 + g_{2A} v_{gs}^3 \quad (2)$$

$$i_{sC} = g_{1C} v_{gsB} + g_{2C} v_{gsB}^2 + g_{2C} v_{gsB}^3 \quad (3)$$

Into the power-series with v_{gsA} and v_{gsB} as

$$v_{gsA} = C_1 v_{gsB} + C_2 v_{gsB}^2 + g_3 v_{gsB}^3 \quad (4)$$

From KCL we can write

$$Y = i_d - i_{sB} - i_{sC} = 0 \longrightarrow i_d = i_{sB} + i_{sC} \quad (5)$$

This work was supported by the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korea government (MEST) through NRL (No. R0A-2007-000-10050-0).

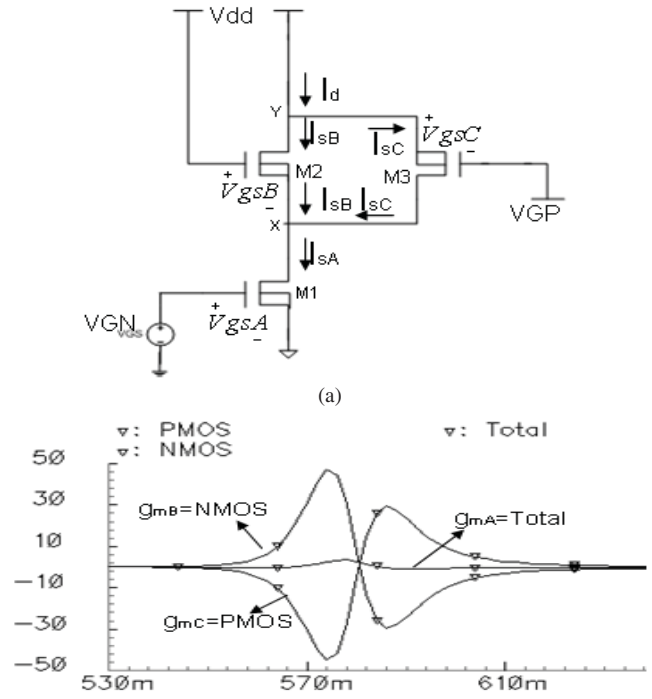


Figure 1: (a) Cascode amplifier with the folded cascode PMOS IIP3 booster. (b) Third-order power series coefficients of i_{sA} at dc.

$$X = -i_{sA} + i_{sB} + i_{sC} = 0 \longrightarrow i_{sA} = i_{sB} + i_{sC} \tag{6}$$

Then we can write $i_d = i_{sA}$

$$i_{sA} \approx (g_{1A} + C_1 g_{1C}) v_{gsA} + (g_{2A} + C_1^2 g_{2C}) v_{gsA}^2 + (g_{3A} + C_1^3 g_{3C}) v_{gsA}^3 \tag{7}$$

In (7), it is clear that c_1 has a negative value from the basic circuit theory. Therefore, the coefficient of the third term in (7) can be made zero by adjusting the gate bias and size of M_C. The above analysis can be confirmed by the simulation results in Fig. 1(b), where g_m's are composite third-order power-series coefficients.

$$g_{mB} = \partial^3 i_B / 6 \partial v_{gsA}^3, \; g_{mC} = \partial^3 i_C / 6 \partial v_{gsA}^3, \; g_{mC} = \partial^3 i_s A / 6 \partial v_{gsA}^3 \tag{8}$$

The g_{mA} of the CS FET M1 has fixed Current (i_{sA}) due to constant V_{gs}, and g_{mB} CG FET M2 are compensated by g_{mB} of the PMOS (M3) $V_{gp}(V_{gs})$. This means that the IMD3 generated by the third order nonlinearity in M1 especially M2 can be fully absorbed by M3. As shown in Fig. 2(a), M2 has fixed V_{gs} but at M3, V_{gs} (V_{gp}) need optimization. Because its value does not only effect on i_{sC}, it also effects on i_{sB}. And both current of i_{sC} and i_{sB} have important rule in fundamental current which boost IIP3. Unfortunately, as can be seen in (7), g_{1A} is also partially reduced by g_{1C} of the IIP3 booster. It causes the lowering of gain. The noise figure is also degraded due to the additional channel noise of the folded PMOS FET. However, degradation in gain and noise is not severe because the bias current and transconductance of the PMOS FET are much smaller than those of the CG NMOS FET due to its low mobility.

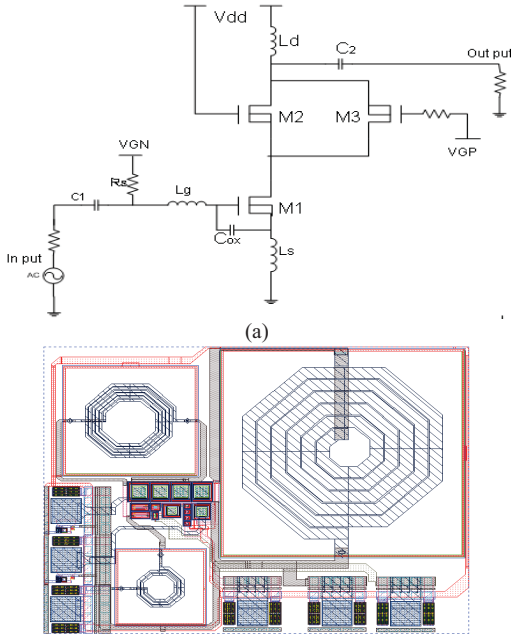


Figure 2. (a) Circuit diagram and (b) layout of the purposed LNA.

This will be confirmed in the simulation results. It has been reported that the cancellation of the third-order nonlinearity cannot guarantee a low IMD3; because, of contribution the second order nonlinearity and feedback by the source degeneration inductance [2]. Referring to the notation in [2], the IMD3 of the source current of CG FET in Fig. 2(a) is proportional to

$$\varepsilon = g_3 - \frac{\frac{2g_2^2}{3}}{g_1 + \frac{1}{j2\omega_0 L_s} + j2\omega_0 C_t + Z_s(2\omega_0)\frac{C_t}{L_s}} \tag{9}$$

From Fig. 2(a), we can write

$$Z_s(2\omega_0) = R_s + j2\omega_0 L_g \tag{10}$$

$$C_t = C_{dd} + C_{gs} \tag{11}$$

Where C_{gs} is an intrinsic gate source capacitance of M1 and C_{dd} is an on-chip capacitor for noise optimization [5]. In [6], the first term comes from the third-order nonlinearity and the second term from the combination of the second-order nonlinearity and feed-back. However, even with a presence of the second term in [6] a noticeable improvement in IIP3 can be obtained. The values of L_s and L_g in Fig. 2(a) are determined for input matching by the following relations:

$$L_s = \frac{C_t}{g_1} R_s, L_g = \frac{1}{C_{gs}\omega_o^2} - L_s \tag{12}$$

Then ε can be written as follows.

$$\varepsilon = g_3 - \frac{\frac{2g_2^2}{3}}{3(1 + j1.5Q_s)} \tag{13}$$

Where

$$Q_s = \frac{1}{(2\omega_o C_t R_s)} \tag{14}$$

Therefore, a high Q-matching network mitigates the contribution of IMD3 caused by the second-order nonlinearity.

If the IMD IIP3 booster simply absorbs the in-phase current with g_3, the improvement factor(IF) using the expression for IIP3 in [2] will be [1].

$$IF = \frac{[\varepsilon]}{|\mathrm{Im}(\varepsilon)|[dB]} - GR[dB] \quad (15)$$

Where GR is gain reduction factor due to the IMD IIP3 booster. With g_1=1.3 A/V, g_2=2.23 A/V^2, $g_3 = 0.61$ A/V^3, the CS FET shown in Fig. 1 at 2.4GHz with L_s=1.34nH yields $IF = 11.21 - GR$ $[dB]$. It is noticeable that the improvements can be obtained under the input matching condition.

III. LNA Design and Simulation Results

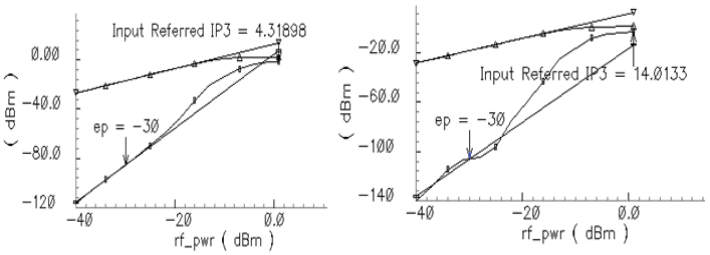
In the LNA design processes PCSNIM (Power-Constrained Simultaneous Noise and Input Matching) technique is used.

- Choose V_{GS} from F_{min} vs. V_{GS} curve for an arbitrary transistor size (choose optimum F_{min})
- Choose C_{gs}(or W) to satisfy P_D (Power dissipation)
- Choose C_{ex} to satisfy Re[Z_s] = Re[Z_{opt}]
- Choose L_S to satisfy Re[Z_s] = Re[Z_{in}]
- Given L_s satisfies Im[Z_{in}*] ≈ Im[Z_{opt}]automatically
- $Z_{opt} = Z_{in}$* at any given P_D
- Insert matching circuit to make $Z_s' \Rightarrow Z_s$
  Noise/input matched simultaneously at any given P_D

The designed LNA in Fig. 2 will be manufactured in a 0.18-μm RF CMOS process and all pads were electrostatic discharge (ESD) protected. Table 1 is the LNA simulation result summary. The IIP3 improved by 9.7 dBm, Noise figure and gain were degraded by 0.2 dB, and 1.2 dB. Fig. 3 shows comparison of the IIP3 of the cases of with and without IIP3 boosting technique. Fig. 4 shows the NF with and without IIP3 boosting technique cases. Fig. 5(a) shows the gain of proposed LNA and (b) shows the input and output matching.

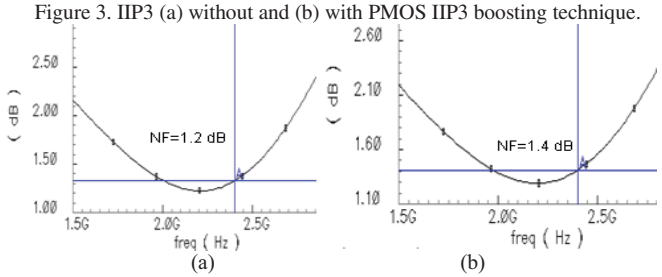
Table 1: THE LNA'S RESULT SUMMARY

	LNA with IIP3 bossting technique	LNA with out IIP3 bossting technique.
Process (um)	0.18	0.18
Supply voltage (v)	1.8	1.8
IIP3 (dBm)	14	4.3
NF (dB)	1.4	1.2
Gain (dB)	12	13.2
Power dissipation(mW)	14.7	14.4



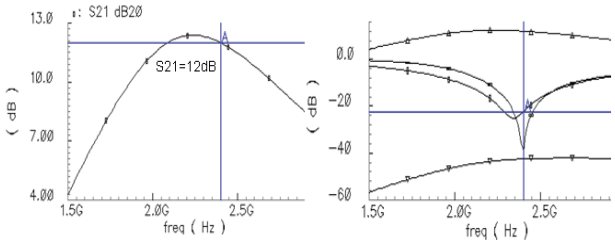
(a) (b)

Figure 3. IIP3 (a) without and (b) with PMOS IIP3 boosting technique.



(a) (b)

Figure 4. NF (a) without and (b) with PMOS IIP3 boosting technique.



(a) (b)

Figure 5. (a) Gain and (b) S11, S22 of the designed LNA.

IV. Conclusions

The paper represents a new technique adopting PMOS transistor source node connected with source of CG FET and drain node connected with CS FET drain. Normally the circuit looks like transmission gate switch; however, due to devices saturation region it dose not work as switch. The proposed technique enables the optimum low noise design at the Common Gate and Common Source stages, which is confirmed by the noise performance at 2.4GHz.

References

[1] Tae-Sung Kim; Byung-Sung Kim, "Post-linearization of cascade CMOS low noise amplifier using folded PMOS IMD sinker", Microwave and Wireless Components Letters, IEEE Volume 16, Issue 4, April 2006.

[2] V. Aparin and L. E. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifiers," IEEE Trans. Microw. Theory Tech., vol. 53, no. 2, pp. 571–581, Feb. 2005

[3] Rajashekharaiah, M.; Upadhyaya, P.; Deukhyoun Heo, "Enhanced gm3 cancellation for linearity improvement in CMOS LNAs", Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on21-24 May 2006.

[4] D. K. Shaeffer and T. H. Lee, the Design and Implementation of Low-Power CMOS Radio Receivers. Norwell, MA: Kluwer, 1999.

[5] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," IEEE Trans. Circuits Syst., vol. 48, no. 9, pp. 835–841, Sep. 2001.