A FULLY INTEGRTED RSSI WITH WIDE DYNAMIC RANGE, LOW POWER CONSUMPTION IN DVB-H.

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INTRODUCTION

RSSI (Received Signal Strength Indicator) is an important block in wireless receiver to detect the received signal strength. Especially in digital TV (DTV) application, such as DVB-T/H (Digital Video Broadcasting-Terrestrial/Handheld) which has a wide input dynamic range, the performance is largely influenced by power control scheduling in receiver, therefore wide range received power detection is an essential task in DTV tuner design. In addition, as an important factor of handheld device, the power consumption of receiver should be minimized to extend battery life. Thus, the RSSI for DVB-H tuner should be designed with low power consumption. It is noticeable that as input power range increases, the power consumption of RSSI increases, proportionally. In this paper, a low power, wide dynamic range RSSI circuit which adopts output to output feedback for dc offset cancellation is presented.

CIRCUIT DESIGN

Figure 1 presents the block diagram of the proposed RSSI which composes of seven gain cells, eight FWRs (Full Wave Rectifier), and one 2^{nd} order LPF. The input to the RSSI is amplified and rectified through each gain cell/FWR, summed up and filtered to a dc voltage output. DCOC (dc offset cancellation) is added at each gain stage, separately, since dc offset from the outputs of the each amplifier can severely deteriorate the performance of rectifiers. Due to utilizing pseudo differential amplifier for low voltage design, common mode feedback (CMFB) circuit is necessary to stabilize the DC operating point and bias the circuit.

Power consumption, gain, and bandwidth have a tradeoff relationship in the cascaded amplifier design for the RSSI [1]. Considering DVB-H application [2], the gain of cascaded stages is set about 77dB. The optimized number of seven stage cascaded amplifiers in RSSI is decided in order to minimize the power consumption [3], as shown in Figure 2.

Figure 3 (a) and (b) show the schematic of the proposed gain cell with feedback-type (output to output) DCOC and the conventional gain cell with feedforward-type (input to output) DCOC [4], respectively. The proposed gain cell uses feedback-type DCOC which constitutes with M1′, M2′, M3′, M4′, M5′, and LPF composed of R_i and C_i. The DCOC of the proposed gain cell detects output dc level of AMP and subtract it from the output again, performing negative feedback operation. Different from that, the DCOC of the structure in Figure 3 (b) detects dc level at the input of gain cell and substrates it from the output. This DCOC requires same amount currents flowing to transistors M1′ and M2′ as input transistors M1, M2, to remove dc offset effectively, wasting additional current. However, the proposed feedback-type DCOC consumes much less current comparing with input transistors M1, M2. Therefore, the proposed gain cell dissipates lower power in whole gain stage.

Figure 4 shows the schematic of the rectifier which transforms the input ac signal from the amplifier (AMP) in Figure 1 to the quantity of the output current (I_0). The rectifier gives its

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output current to LPF and the dc output of LPF represents the received signal strength, following ac input power of RSSI. In this design, 2nd order LPF is used for on-chip integration. The component values in the Figure 1, of R_L, C_L, R_{out}, and C_{out} are 2.5KΩ, 10pF, 300KΩ, and 10pF, respectively.

SIMULATION RESULTS

The proposed RSSI circuit is simulated with the model of CMOS 0.13um technology. The simulated frequency response of the whole gain stages are shown in Figure 5. Simulation results show 77dB cascaded gain and 7MHz 3dB-bandwidth in the whole gain stages. The simulated RSSI output voltage with input signal power is shown in Figure 6, the RSSI linear range is approximately 70dB with ± 1 dB error. In Table.1, the performance of the proposed RSSI is compared to the previously reported RSSI. The proposed RSSI shows lower power dissipation than others under similar performance level of dynamic range.

Table.1 Summarized performances of RSSI

	[3]	[4]	This Work
Technology	0.6 um CMOS	0.18 um CMOS	0.13 um CMOS
Supply voltage	2 V	1.2 V	1.2 V
Current consumption	3.1 mA	1.9 mA	1.2 mA
Total gain	84 dB	54 dB	77 dB
BW	10 MHz	3 MHz	7 MHz
RSSI DR	75 dB	50 dB	70 dB
RSSI error	± 1 dB	± 1.5 dB	± 1 dB

CONCLUSIONS

This paper presents a low power, wide dynamic input range RSSI for DVB-H application. By using negative feedback-type DCOC circuit and 2nd-order LPF, the low power and more integrated RSSI design can be achieved. Simulation results show 77dB voltage gain, 7MHz 3dB-bandwidth, and 70dB linear range with ± 1dB error in the RSSI output, while consuming 1.2mA from a 1.2V supply.

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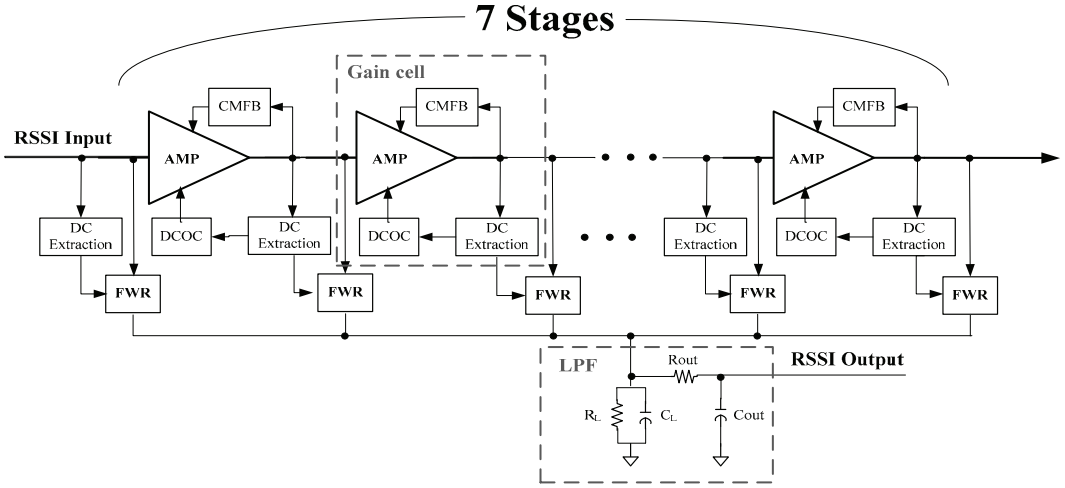

Figure 1. Block diagram of designed RSSI.

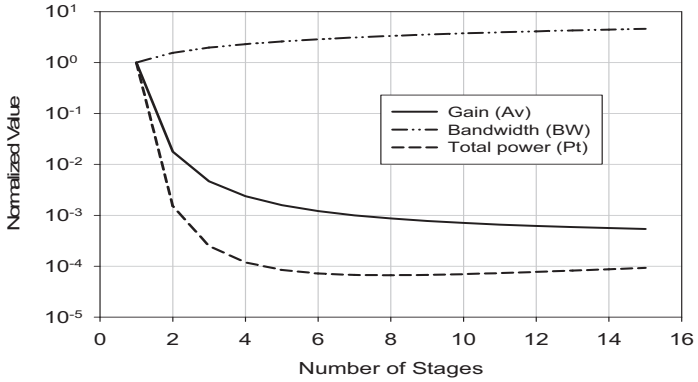

Figure 2. Normalized gain(Av), bandwidth(BW), and total power consumption (Pt) as a function of the number of stages where total gain is 77dB.

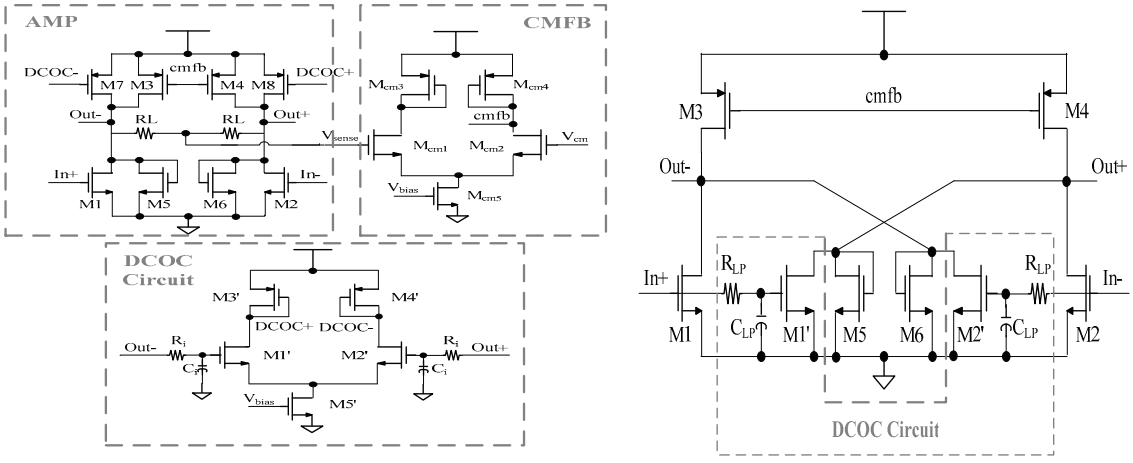

Figure 3. Schematic of gain cells. (a) Proposed gain cell. (b) Conventional gain cell.

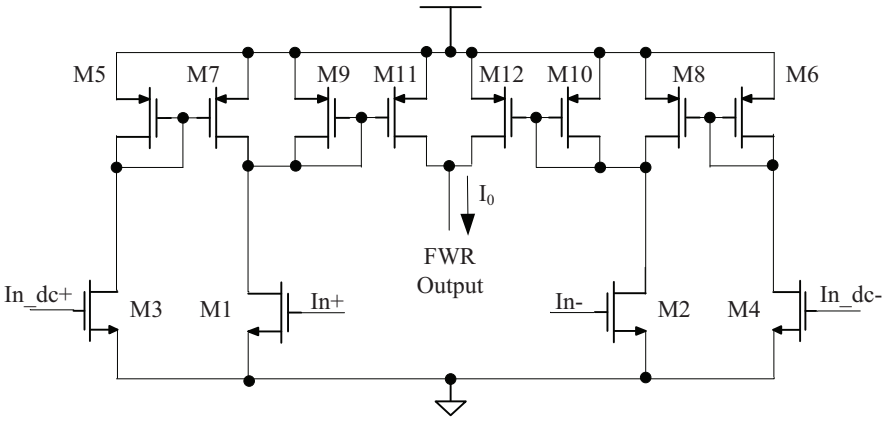

Figure 4. Schematic of full wave current rectifier.

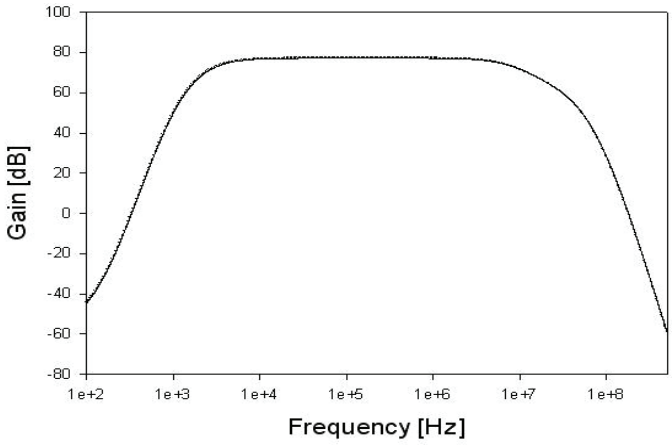

Figure 5. Simulated ac response.

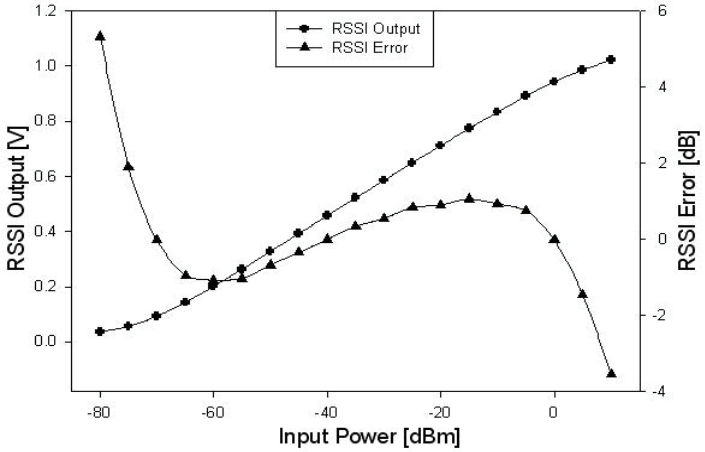

Figure 6. Simulated RSSI output and error.