A Current-Reused Low-Power Four-Quadrant Multiplier with Single-Ended Current Output

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***Abstract*—This paper presents an alternative topology for realizing a four-quadrant amplifier with single-ended output. In the proposed multiplier, constituting differential circuits are vertically arranged resulting in single-ended current output with output DC voltage equal to a half of supply voltage. Since the circuit operates in a current-reused mode, the power consumption is systematically reduced by a factor of 50% compared to the original topology. The proposed multiplier is designed based on a 0.18 μm CMOS process and can operates under a 1.2 V supply.**

I. INTRODUCTION

An analog multiplier is widely used for modulation-demodulation, rectification, multiplication, frequency translation, etc. Multipliers give linear products of two continuous signals x and y, yielding an output $z = Kxy$, where K is a multiplication constant with suitable dimension. A four-quadrant multiplier is a multiplier where both x and y can be bipolar, and therefore it has four input combinations, i.e. ($+x$, $+y$), ($+x$, $-y$), ($-x$, $+y$) and ($-x$,$-y$).

Multipliers utilizing the non-linearity of MOSFET have been frequently reported. Best performing four-quadrant MOSFET multipliers are almost always based on a fully differential circuit that both inputs x and y are fully differential. Very often a fully differential multiplier also implies that it has differential outputs [1]-[6].

However, some circuits require only one output from a multiplier, e.g. up-conversion mixer [7] or when simplicity is demanded. For this requirement, additional circuits are needed to convert differential output of the multiplier into single-ended output.

In this paper an alternative four-quadrant multiplier topology is introduced. The topology provides single-ended current output while keeping fully-differential multiplication.

II. DERIVATION OF THE PROPOSED MULTIPLIER

A. Reference Multiplier Topology and Operation

The original four-quadrant fully differential multiplier structure is shown in Fig. 1(a) [1]. The circuit utilizes the transistors M_1~M_4 in linear region. It has two pairs of differential voltage inputs, ($+x$, $-x$) and ($+y$, $-y$), and a pair of differential output (I_{o1}, I_{o2}). The transistors M_5~M_8 operate in saturation region to function as voltage followers. The currents in the branches are expressed as

$$I_1 = K\left(X + x - V_T - \frac{V_{sy+}}{2} \right) V_{sy+}, \tag{1}$$

$$I_2 = K\left(X - x - V_T - \frac{V_{sy+}}{2} \right) V_{sy+}, \tag{2}$$

$$I_3 = K\left(X - x - V_T - \frac{V_{sy-}}{2} \right) V_{sy-}, \tag{3}$$

$$I_4 = K\left(X + x - V_T - \frac{V_{sy-}}{2} \right) V_{sy-}, \tag{4}$$

where $V_{sy+} = Y + y - V_T$ and $V_{sy-} = Y - y - V_T$. $K = \mu_0 C_{ox} \frac{W}{L}$ and V_T are the notation for MOSFET (M_1~M_4 in this case) transconductance parameter and the threshold voltage, respectively. In order to obtain the multiplication result, the output currents are subtracted from each other.

$$\begin{aligned} I_o &= I_{o1} - I_{o2} \\ &= (I_1 + I_3) - (I_2 + I_4) \\ &= 4Kxy. \end{aligned} \tag{5}$$

B. Proposed Multiplier

The circuits producing currents I_{o1} and I_{o2} in Fig. 1(a) are re-drawn in Fig. 1(b) into two separate subcircuits. The two subcircuits of the multiplier are identical. The only difference is the way input signals are assigned to perform a fully differential multiplication. Further, we can find four identical

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linear and saturated mode transistor pairs in the circuit, i.e.: M_1-M_5, M_2-M_6, M_3-M_7 and M_4-M_8.

By following Kirchhoff's current law (KCL), the currents come out from the lower ends of both subcircuits shown in Fig. 1(b) are equal to the currents enter into the upper ends. Therefore, if we stack one subcircuit onto the other subcircuit and later tap the current from the connection node, then this current will be, again by following KCL, equal to the result of subtraction in (5), which is linearly proportional to the result of multiplication of x and y. This proposed multiplier structure is shown in Fig. 2. In this figure Z is the connection node, from which the final output current is tapped.

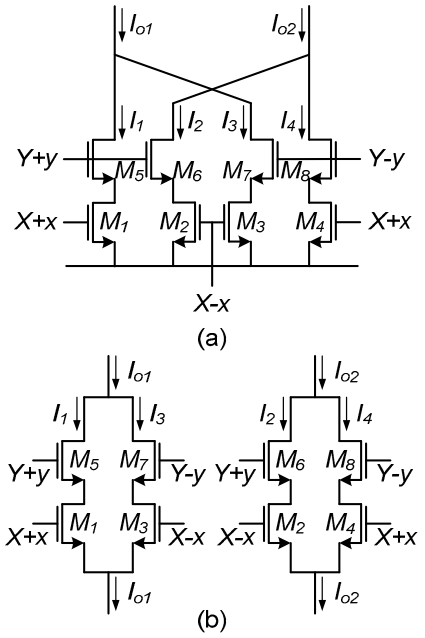


Figure 1. (a) Fully-differential four-quadrant MOS multiplier[1], (b) the constituting subcircuits.

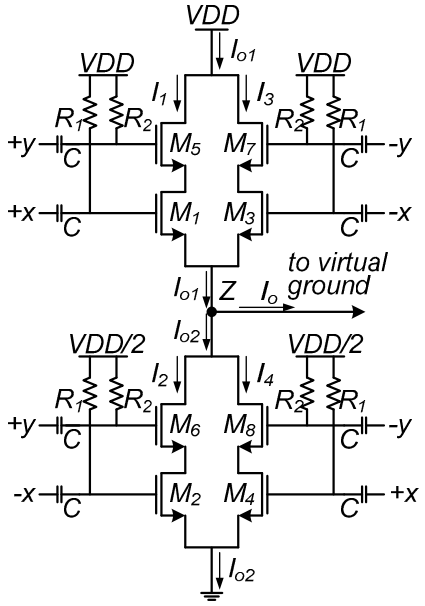


Figure 2. Proposed single-ended current output four-quadrant MOS multiplier.

In order to ensure that the multiplication is performed properly by the proposed multiplier, the subcircuits have to be kept balanced, which means that transistors M_1~M_8 in the topology shown in Fig. 2 have to have the same bias conditions as transistors M_1~M_8 in the original topology shown in Fig. 1(a) or, in other words, the bias of all linear and saturated mode transistor pairs have to be the same, including the threshold voltages V_T. The latter is possible by connecting the body to the source of the respective transistors. Therefore, to implement the circuit, a CMOS technology that has a triple-well feature is required.

When above conditions are fulfilled, the current tapped from node Z then will give the same multiplication result. Moreover, since two symmetrical subcircuits are connected in series between the supply voltage, *VDD*, and the ground, automatically node *Z* is locked to a voltage level of *VDD/2*.

In Fig. 2 four transistors are stacked from *VDD* to ground. Contrary to common sense, they do not require large *VDD* because transistors M_1~M_4 are in linear region. Drain-source voltages V_{ds} of these MOSFETs can be set very low. Therefore, the required *VDD* could be as low as

$$VDD \cong 2\left(V_{ds-lin} + V_T + y\right), \tag{6}$$

where $V_{ds\text{-}lin}$ is V_{ds} of transistors M_1~M_4. For 0.18 μm CMOS technology in which the circuit is simulated $V_T \approx$ 450 mV, so the multiplier still can operate with *VDD* of 1.2V, which is a voltage level that can be easily provided with ordinary dry-cell batteries.

Since there are two identical balanced subcircuits stacked between *VDD* and ground, maximum gate-source voltage V_{gs} is only *VDD*/2. By biasing all gate terminals with voltages of *VDD*/2 through resistors, transistors M_5~M_8 are self biased, thus ensured to be in the saturation region. On the other hand, since the threshold voltages of transistors in linear and saturation regions are almost the same, and the threshold voltage for gate-source and gate-drain connections are also the same, consequently transistors M_1~M_4 are in the linear region as expected.

In Fig. 2 the reference floor of upper-side subcircuit (above node *Z*) has a voltage of *VDD/2*, therefore gate terminals of transistor M_1, M_3, M_5 and M_7 are hooked to *VDD* instead of *VDD*/2. However, although the DC voltage level of node *Z* is equal to *VDD*/2, it is decided not to hook the gate terminals of transistors M_2, M_4, M_6, and M_8 to this node because the output impedance could be comparable to resistors R_1 or R_2 in series with MOSFET input impedances, which can create feedbacks and vary the DC bias. These transistors are then biased from separate *VDD*/2 source, which is simply a voltage divider supplied with *VDD*.

In Fig. 1(a) due to its parallel arrangement, each two gate terminals with the same input signal (either +x, -x, +y or –y) can be directly coupled to each other because they have the same biasing DC voltage. In the proposed circuit, gate terminals with the same input signal cannot be coupled directly because they have different biasing voltages. Therefore, DC-blocking capacitors *C* are needed.

C. Advantages of the Proposed Multiplier

Two advantages have been described earlier. First, the multiplier can provide single-ended output without additional circuits. Actually the proposed topology is still able to provide a differential output, when it is necessary, with the cost of chip area. The structure in Fig. 2 is formed by stacking the left-sided subcircuit in Fig. 1(b) onto the right-sided one. If the stacking is performed in the reverse order, the output current also will be reverse. Simultaneous implementation of both structures will create a four-quadrant multiplier with fully differential outputs.

The second advantage that has been mentioned is the DC voltage level of the output is locked to *VDD*/2 due to the symmetry of the upper- and lower-side subcircuits. This well defined DC voltage can allow direct DC coupling with subsequent block.

Another significant advantage is the reduction of power consumption. In multipliers based on the topology of Fig. 1(a) [1, 2, 3] or Gilbert-cell [6], *VDD* supplies currents I_{o1} ($=I_1 + I_3$) and I_{o2} ($=I_2 + I_4$) through resistive loads. In the proposed multiplier, due to the current-reused biasing technique, a comparably equal *VDD* supplies either only I_{o1} ($=I_1 + I_3$) or only I_{o2} ($=I_2 + I_4$), which means the power consumption is reduced by a factor of 50%.

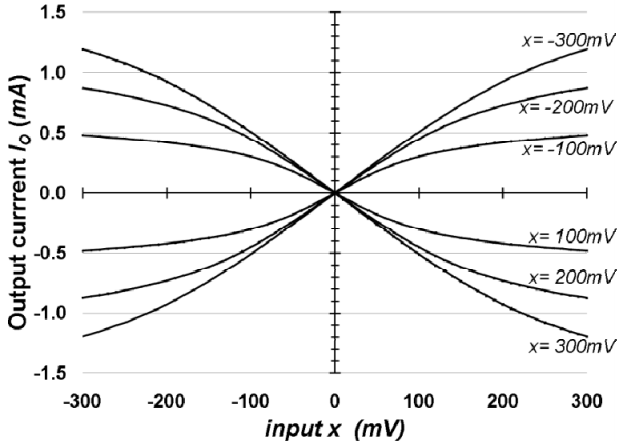
Furthermore, multipliers applying resistive loads have a difficulty to increase their gains by increasing *W/L* ratio of the transistors; as *W/L* ratio is increased, the output DC voltage drops and the multipliers can be turned off or the dynamic range of their output voltage is reduced. In the proposed multiplier, increasing gain by increasing *W/L* ratio of all transistors does not change the bias voltages due to its symmetrical structure. This feature can be very important when the multiplier is fed with an output of an amplifier preceding it, because it means that the minimum required gain of the amplifier can be shared to the multiplier so that the amplifier gain can be more relaxed.

III. Simulation Results

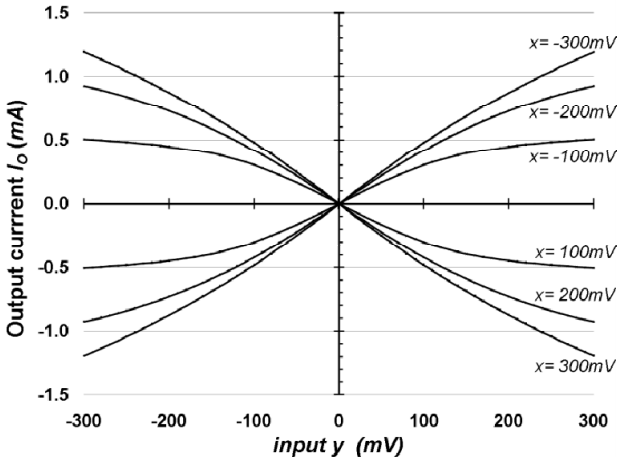
Simulations have been performed to verify that the proposed circuit can function properly as a multiplier. The proposed multiplier have been designed and simulated based on 0.18 μm CMOS technology. In the simulations all transistors are basically self-biased as shown in Fig. (2). The multiplier is simulated with 1.2V supply (*VDD*), linear MOSFETs (M_1~M_4) with *W/L*= 1.5 μm/180 nm, and saturated MOSFETs (M_5~M_8) with *W/L*= 2 μm/200 nm. Besides that, *Number of Fingers* (NOF) parameters, which also represent the effective *W/L* ratio, of all MOSFETs are set to 10.

Figs. 3(a) and (b) show the simulated DC transfer characteristics of the multiplier for input signal *x* and *y*. It shows that the circuit can have a good linearity for signal with amplitude up to 300 mVpp.

Fig. 4 shows another simulation result to test the linearity of the circuit. Setting both input amplitudes to 200 mVpp at frequency 6.95 GHz for *x* and 7 GHz for *y*, the output amplitude of the constituting frequencies at the lower band of the spectrum (i.e. frequencies less than 7 GHz) is much lower than the amplitude of the target frequency; i.e. 50 MHz. For the same input setting the total harmonic distortion can be as low as 1.1% by attaching a simple single-pole low pass filter with 200 MHz cut-off frequency to the output of the multiplier to filter out upper-band spectrum.



(a)



(b)

Figure 3. Multiplier DC transfer characteristics for (a) input *x* of the linear transistors, (b) input *y* of the saturated transisotrs.

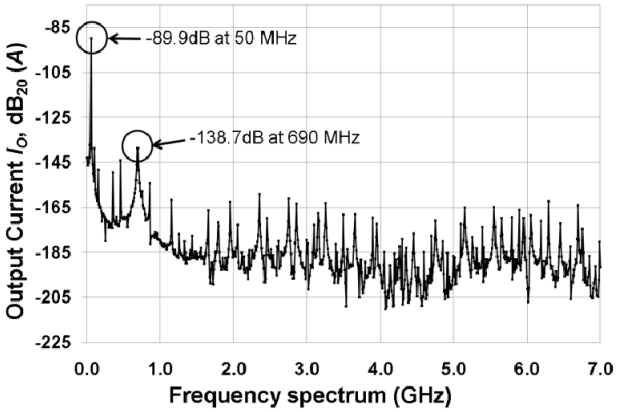


Figure 4. Lower-band frequency spectrum of a multiplication result between 6.95 GHz and 7 GHz sinewaves with 200 mVpp amplitudes.

To test the bandwidth of the multiplier, both input signals with 200 mVpp amplitude are constantly set to two frequencies spaced with 50 MHz. The frequency of the signal *y* is the highest; while the frequency of the signal *x* is the lowest. After that, the frequency of the signal *y* is swept from 500 MHz to 50 GHz. For each combination frequency of signal *y* and *x*, the output current amplitude at 50 MHz is recorded. The result is shown in Fig. 5. For this method, the bandwidth is defined as the frequency where the amplitude is dropped as high as 6 dB for the reason that a multiplier is a two-input system, and if both inputs are at the edge of their 3dB-bandwidth frequencies then the output of the multiplier will experience a 6dB-gain drop. From this simulation, the bandwidth of the multiplier is surprisingly around 14GHz which is more than enough for an impulse radio UWB application.

Results of other simulations to verify the capability of the proposed circuit in multiplying two ac signals at its inputs are shown in Fig. 6 and 7. Fig. 6 shows the multiplication of input signal *x* (drawn on the first row) and input signal *y* (drawn on the second row). The result is shown on the third row. In this mode the multiplier functions as a modulator; input *x* is the modulating signal and input *y* is the modulated signal. In Fig. 7, two input signals with the same frequencies, represented with two sequences of pulses shown on the first and second rows, are multiplied. The sequence of unipolar pulses shown on the third row as its result confirms that the circuit is able to multiply its inputs.

IV. CONCLUSIONS

A single-ended current output four-quadrant MOSFET multiplier has been described and the proposed circuit can perform the multiplication function. The multiplier operates in the current-reused mode that reduces the power consumption. Due to its vertically symmetrical structure, the output DC voltage is fixed to a value of *VDD/2*. The gain of the multiplier can be easily increased by increasing *W/L* ratio of all transistors simultaneously with the same multiplication factor.

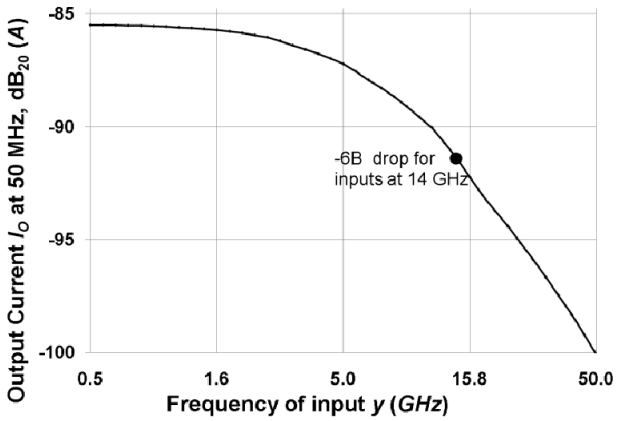


Figure 5. Bandwidth of the multiplier with inputs injected simultaneously; frequency of *x* is 50 MHz lower than frequency of *y*.

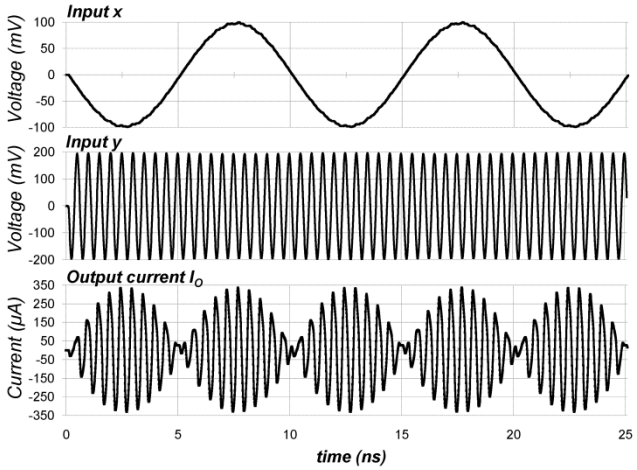


Figure 6. The multiplier working as a modulator.

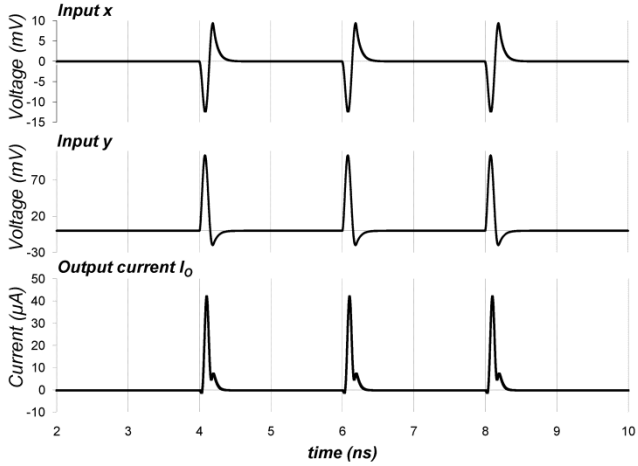


Figure 7. The multiplication of signals with the same frequency.

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