IEEE Asian Solid-State Circuits Conference
November 16-18, 2009 / Taipei, Taiwan

A new low-distortion transconductor applied in a flat band-pass filter

Ha Le-Thai, Huy-Hieu Nguyen, Hoai-Nam Nguyen, Hong-So Cho, Jeong-Seon Lee, Sang-Gug Lee
Korea Advanced Institute of Science and Technology
F 514, Research Wing, 305 - 714, u-radio Lab, 119, Mujiro, Yuseong-gu, Dae-jeon, Republic of Korea
Email: {sglee, hale}@icu.ac.kr

Abstract- **A new linearity improvement technique is proposed to implement a low-distortion Gm-C band-pass filter working in high IF ranges. The purpose of the linearization technique is to eliminate G_m'' value of the transconductor by employing a superposition method that combines two opposite non-linear behaviors of the two parallel wings designed inside the transconductor. Instead of conventional biquad structure, a resonant-coupling structure is adopted for the band-pass filter working at center frequency of 80MHz to make the frequency response flat and stable and to allow a stable frequency tuning as well as a flexible bandwidth tuning. Fabricated in 65nm CMOS process, the implemented IF band-pass filter provides a flat band-pass whose ripple is smaller than 0.1dB, a third-order rejection of 27dB, an IIP3 of -2dBm, and a NF of 21.5dB, while consuming 11mA from 1.2-V supply. The filter occupies a chip size of 0.5 mm × 0.5 mm.**

I. INTRODUCTION

In some wireless transceivers, the usages of off-chip IF filters show disadvantages such as size and additional power consumption due to the buffers to drive off-chip components. Therefore, there comes a need for on-chip IF filters.

G_m-C filters are popular due to their advantages of high frequency performance and low power consumption, but have linearity problems. To overcome the disadvantage of linearity of G_m-C filters, many linearization techniques for transconductors have been reported. Source degeneration technique [1] may be the simplest and most well-known one. Cross-coupling technique [2] and its modifications are also reported to achieve high linearity at the cost of poor bandwidth. Linearity is also improved with the bias feedback technique [3], but the obligated usage of a current tail in this method limits its performance at low supply voltage. In this paper, a new linearization technique is proposed to implement a low-distortion transcondutor by realizing a superposition method to diminish nonlinear components. The proposed transconductor is implemented with pseudo differential structure which is suitable for low voltage applications.

The important requirements for band-pass filter design are high unwanted signal rejection ratio and flat pass-band characteristics. For high rejection ratio, there seems no simpler method than the adoption of negative resistance. And for flat pass-band requirement, C-coupling method [4] and magnetic coupling method [5] have been reported. However, each of them has its own disadvantages. With C-coupling technique, it is hard to achieve small bandwidth in high frequency ranges because of the correlation between the center frequency and the Q factor of the filter. Although magnetic coupling technique has been usually used as a Q-enhancement method in GHz-range applications, adopting this method for hundred-MHz IF frequency ranges is not simple because of the usage of transformer at frequencies lower than 1GHz. In this paper, resonant-coupled filter band-pass architecture is employed, which adopts the proposed linear transconductor.

The proposed linearity technique for the transconductors is described in Section II. Section III presents the filter architecture. The implementation result is presented in Section IV. Finally, Section V concludes the paper.

II. TRANSCONDUCTOR DESCRIPTION

Fig. 1 shows the new linearity improvement technique for the transcondutor of the G_m-C filter designs. The proposed linearization method is based on the superposition of two parallel wings of opposite behaviors inside the transconductor. The two opposite responses of the two parallel wings in Fig. 1 compensate each other to diminish non-linear elements. As a result, the G_m'' value of the overall transconductor is kept nearly zero over a large range of input signal amplitude.

The structure of both the two parallel parts is pseudo differential structure which is more suitable for low voltage design than fully differential structure whose current tail consumes a certain amount of headroom.

The self-cascode structure shown in Fig. 2 (a) is the core of this linearity improvement technique. In the self-cascode structure, M_1 is in triode region while M_2 is in saturation region. Based on the characteristics of self-cascode circuit, transconductor shown in Fig. 1 is analyzed as follows.

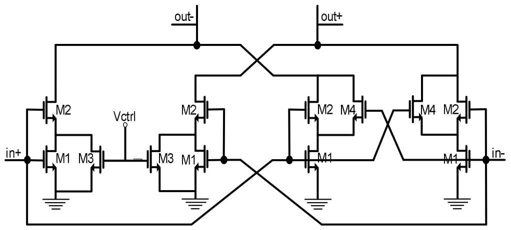


Figure 1. The structure of the proposed CMOS transconductor

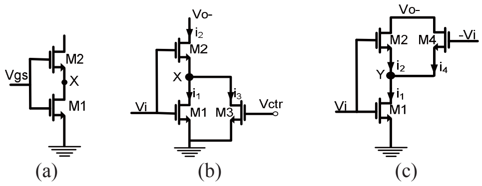


Figure 2. The core circuit and the half circuits of the two wings of Fig. 1, (a) self-cascode structure, (b) the half of the left wing in Fig. 1, (c) the half of the right wing in Fig. 1

The circuits shown in Fig. 2 (b) and Fig. 2 (c) are the halves of circuits in the left and right wings of the circuit shown in Fig. 1, respectively.

For Fig. 2 (b), M_1 and M_3 work in triode region, while M_2 is in saturation region. For Fig. 2 (c), M_2 and M_4 work in saturated region, while M_1 is linear.

We call that V_{CM} and v are the common mode and small ac voltages of the input node, respectively; V_t is the threshold voltage of NMOS transistors; $k_i = 0.5(W/L)_i C_{OX}$; $k_{ij} = k_i + k_j (i \neq j)$; $k_{ijl} = k_i + k_j + k_l (i \neq j \neq l)$.

After some steps of calculations, the total drain current of the combination of Fig. 2 (b) and Fig. 2 (c) is expressed by

$$i_\Sigma = i_{2(b)} + i_{2(c)} = \frac{k_2}{k_{123}^2}\Delta'_X + \frac{k_{24}}{k_{124}^2}\Delta'_Y + [\frac{k_2k_3^2}{k_{123}^2} + 4\frac{(k_2k_4^2 + k_4k_{12}^2)}{k_{124}^2}]v^2 + [\frac{2k_2k_3}{k_{123}^2}\sqrt{\Delta'_X} - \frac{4k_4k_1}{k_{124}^2}\sqrt{\Delta'_Y}]v \quad (1)$$

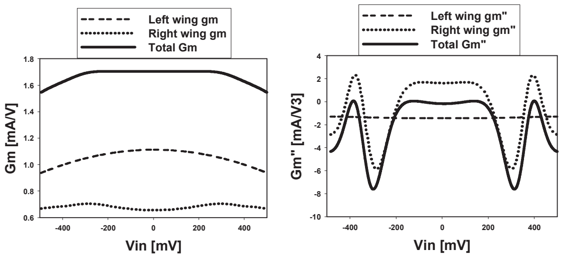
where

$$\Delta'_X = (k_{12}^2 - k_{123}k_2)v^2 + 2k_{123}k_1(V_{CM} - V_t)v + k_{123}k_{13}(V_{CM} - V_t)^2 \quad (2)$$

$$\Delta'_Y = [(k_{12} - k_4)^2 - k_{124}k_{24}]v^2 + 2k_{124}k_1(V_{CM} - V_t)v + k_{124}k_1(V_{CM} - V_t)^2 \quad (3)$$

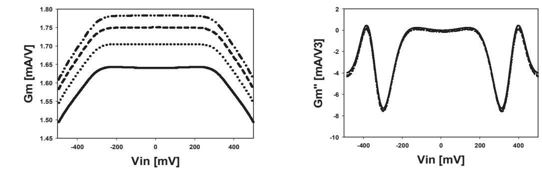
The output current of the differential transconductor is $i_{out} = i_\Sigma^+ - i_\Sigma^-$, which removes all v^2 elements in (1). It means that there is only $[\frac{2k_2k_3}{k_{123}^2}\sqrt{\Delta'_X} - \frac{4k_4k_1}{k_{124}^2}\sqrt{\Delta'_Y}]$ containing distortion components in i_{out}.

In Equation (1), the component $(2k_2k_3/k_{123}^2)\sqrt{\Delta'_X}$ is the nonlinear contributor of the left wing in Fig. 2 (b), while $-(4k_4k_1/k_{124}^2)\sqrt{\Delta'_Y}$ is the nonlinear contributor of the right wing in Fig. 2 (c).



(a) (b)

Figure 3. Characteristics of transconductances (g_m) and their derivatives (g_m''), (a) g_m values of the left and right wings and the combined G_m value, (b) g_m'' values of the left and right wings and the combined G_m'' value.



(a) (b)

Figure 4. The variation of G_m'' value versus G_m tuning, (a) G_m tuning with control voltage from 600 to 900mV, (b) the change of G_m'' versus G_m tuning

The combination of these two wings diminishes as the two nonlinearities of opposite behaviors are added increasing the linearity at the output. Because of the fact that tuning the values of $(2k_2k_3/k_{123}^2)\sqrt{\Delta'_X}$ and $-(4k_4k_1/k_{124}^2)\sqrt{\Delta'_Y}$ is just a matter of transistor size tuning, the optimum condition for linearity can be easily achieved by changing the size of transistors in the G_m cell.

In order to make the idea more intuitive and easier to understand, Fig. 3 gives us the simulation results of transconductance values and their second derivatives. As shown in Fig. 3 (a) and Fig. 3 (b), the g_m and g_m'' values of the left and right wings of the transconductor have opposite responses to each other in a large range of input signal amplitude. Therefore, we can achieve the overall G_m'' value to be near zero as depicted in Fig. 3 (b) by the superposition of g_m'' values of both the left and right wings of the parallel structure in Fig. 1. The overall G_m value shown in Fig. 3 (a) of the proposed transconductor is constant in a large range of input signal amplitude.

Fig. 4 shows another advantage of the proposed linearization technique. When the overall transconductance value - G_m is tuned by the control voltage, the value of G_m'' changes little, which makes the transconductor keeps itself linear over the tuning range of G_m. The reason for this advantage is simply that the control voltage is at the gates of transistors M_3, which work in triode region. Thus, the linear amount of current contributed by M_3 does not have much effect on the linearity of the transconductor. Or continuous-time tuning of the filter does not raise linearity problems due to the changed bias.

III. FILTER ARCHITECHTURE

To achieve a flat pass-band, a resonant-coupling filter is employed by adopting the proposed linear transconductor shown in Fig. 1. Fig. 5 shows the principle theory to make the pass-band flat by making two poles at two different frequencies, which relates to multi-resonator filters [6].

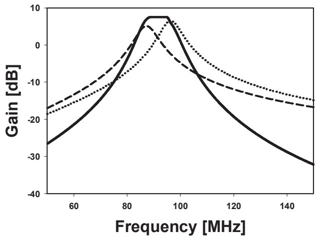


Figure 5. Making the pass-band flat by combining two resonant frequencies

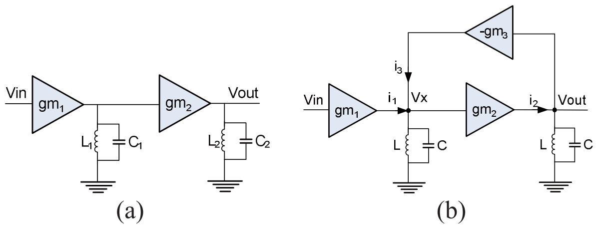


Figure 6. Two investigated structures: (a) cascaded resonators, (b) resonant coupling

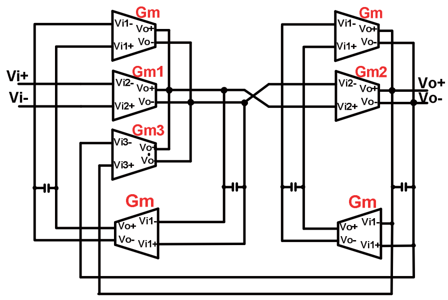


Figure 7. Complete structure of the filter

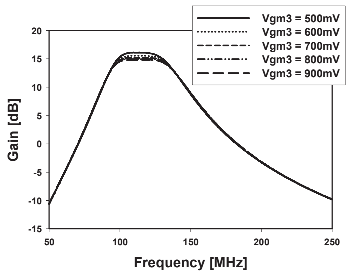


Figure 8. Q-factor of the filter versus gm_3 tuning

In stead of using two resonators at two frequencies, in this filter design, two resonators at the same frequency with a negative feedback path taking part as a coupling component is employed. That feedback path is a transconductor whose g_m value determines the bandwidth of the overall filter.

Two investigated filter structures to make the band-pass flat are shown in Fig. 6. Fig. 6 (a) describes a filter composed of two cascaded resonators which operate at different frequencies. The ac response of this filter can be easily derived as

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}s^2}{(s^2+\omega_1^2)(s^2+\omega_2^2)} \qquad (4)$$

where $\omega_1^2 = 1/(L_1C_1)$ and $\omega_2^2 = 1/(L_2C_2)$

Since the two center frequencies in (4) are determined by two separated L-C resonators, the pass-band and the center frequency are sensitive to process and temperature variations, and component mismatch.

Fig. 6 (b) shows a filter with two identical resonators coupled by a negative feedback path ($-g_{m3}''$). The frequency transfer function of the filter can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_{m1}g_{m2}}{C^2}s^2}{s^4+2s^2(\omega_0^2+\omega_\Delta^2)+\omega_0^4} = \frac{\frac{g_{m1}g_{m2}}{C^2}s^2}{(s^2+\omega_1^2)(s^2+\omega_2^2)} \qquad (5)$$

where $\omega_0^2 = 1/(LC)$, and $\omega_\Delta^2 = g_{m2}g_{m3}/C^2$.

The bandwidth of the filter is derived as

$$BW = \omega_2 - \omega_1 = \sqrt{2}\omega_\Delta = \sqrt{g_{m2}g_{m3}/C^2} \qquad (6).$$

Equation (5) says that the center frequency is $\omega_0 = 1/\sqrt{LC}$ and equation (6) says that the bandwidth of the filter response depends on the feedback G_m cell ($-g_{m3}$).

The L-C resonators are easily implemented with G_m-C integrators, which is very well-known. Fig. 7 shows the complete filter design based on the resonant-coupling structure in Fig. 6 (b).

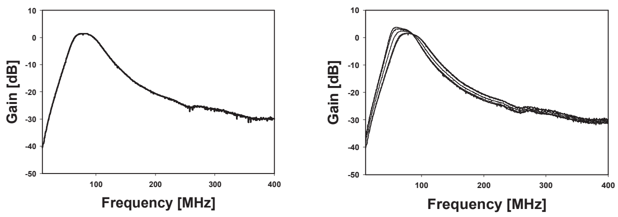
Usually, the bandwidth of the pass-band is changed by controlling the value of g_{m3} while g_{m1} and g_{m2} are kept constant. Fig. 8 shows the variation of bandwidth versus g_{m3} tuning. The flatness of the pass-band characteristic is well controlled over the tuning. The bandwidth of the filter increases when the g_{m3} value increases and vice-versa.

IV. EXPERIMENTAL RESULTS

The forth-order Gm-C filter shown in Fig. 7 is designed in a 65nm CMOS process. The designed filter excluding the output buffer draws 11mA from 1.2-V supply. The buffer at the output is included for matching with the 50 Ohm measurement equipment. Fig. 9 shows the measured frequency response of the implemented filter. Because of the resonant-coupling structure, the achieved band-pass ripple in Fig. 9 (a) is smaller than 0.1dB in whole bandwidth of 10MHz at 80MHz center frequency. Fig. 9 (b) describes frequency responses over continuous-frequency tuning. The gain variation over frequency tuning is caused by the asymmetrical layout causing variations on bias conditions. The filter attenuates the signals at the frequencies of $0.5f_0$ and $3f_0$ of the center frequency f_0 by 17dB and 27dB, respectively.

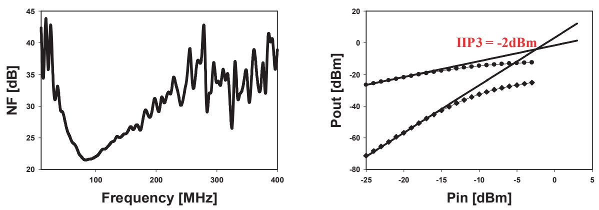
Fig. 10 (a) shows the measured noise figure of the whole filter including the output buffer, where the NF is 21.5dB at center frequency of 80MHz. The IIP3 of -2dBm is shown in Fig. 10 (b) for two input tones of 79 and 81MHz. The measured IIP3 is 2dB lower than the simulation result, which appears to be caused by the output buffer.

Table I compares the performance of the implemented filter with those of other reported filters working under similar conditions.



(a) (b)

Figure 9. Frequency response of the implemented filter, (a) frequency response with 80MHz center frequency, (b) frequency response in continuous-time tuning



(a) (b)

Figure 10. (a) Noise Figure of the filter including output buffer, (b) IIP3 of the filter with two tones of 79MHz and 81MHz at the input

TABLE I FILTER PERFORMANCE PARAMETERS

	[7]	[8]	[9]	[10]	This work
Order	6	2	-	6	4
f_0 (MHz)	70	85	80	100	80
BW (MHz)	0.2	0.6	1.8-5	10	10
Pass-band gain (dB)	30	2-12	19.55	0	2
In-band ripple (dB)	-	-	-	4	0.1
IIP3 (dBm)	-10	-1	-2.8	-	-2
NF (dB)	46	-	-	-	21.5
Current (mA)	36	7.5	20	10	11
Technology	$0.5\mu m$ HP	HF3 CMOS	$0.25\mu m$ BiCMOS	$0.6\mu m$ CMOS	65nm CMOS
Supply Voltage (V)	2.5	± 2.5	3.3	2.95	1.2

V. CONCLUSION

This paper reported a new linearization technique for transconductors used in a resonant-coupling Gm-C filter. The proposed transconductor is suitable for high-frequency applications which require a low voltage supply and a large input range. The achieved results show the advantages of flat band-pass and stable ac shape of the resonant-coupling structure. With good performance at 80MHz, this work also promises new applications on higher frequencies with tuning systems.

VI. ACKNOWLEDGMENT

This work was sponsored by ETRI SoC Industry Promotion Center, Human Resource Development Project for IT SoC Architect. The CAD tools have been supported by IDEC of KAIST

VII. REFERENCES

[1] Krummenacher, F.; Joehl, N., "A 4-MHz CMOS continuous-time filter with on-chip automatic tuning" *Solid-State Circuits*, IEEE Journal of Volume 22, Issue 3, Jun 1987 Page(s):335 - 342.

[2] Silva-Martinez, J.; Steyaert, M.S.J.; Sansen, W.M.C., "A large-signal very low-distortion transconductor for high-frequency continuous-time filters" *Solid-State Circuits*, IEEE Journal of Volume 26, Issue 7, July 1991 Page(s):946 - 955.

[3] Kim, C.S.; Kim, Y.H.; Park, S.B., "New CMOS linear transconductor" *Electronics Letters*, Volume 28, Issue 21, 8 Oct. 1992 Page(s):1962 – 1964.

[4] Lerstaveesin, S.; Gupta, M.; Kang, D.; Bang-Sup Song, "A 48–860 MHz CMOS Low-IF Direct-Conversion DTV Tuner" *Solid-State Circuits*, IEEE Journal of Volume 43, Issue 9, Sept. 2008 Page(s):2013 - 2024.

[5] Kuhn, W.B.; Yanduru, N.K.; Wyszynski, A.S., "Q-enhanced LC bandpass filters for integrated wireless applications" *Microwave Theory and Techniques*, IEEE Transactions on Volume 46, Issue 12, Part 2, Dec. 1998 Page(s):2577 - 2586.

[6] A.I. Zverev, "Handbook of Filter Synthesis" *John Wiley and Sons*, New York, 1967, pp. 300 – 310.

[7] Choi, Y.W.; Luong, H.C., "A high-Q and wide-dynamic-range 70 MHz CMOS bandpass filter for wireless receivers" *Circuits and Systems II: Analog and Digital Signal Processing*, IEEE Transactions on Volume 48, Issue 5, May 2001 Page(s):433 - 440.

[8] Fabre, A.; Saaid, O.; Wiest, F.; Boucheron, C., "Low power current-mode second-order bandpass IF filter" *Circuits and Systems II: Analog and Digital Signal Processing*, IEEE Transactions on Volume 44, Issue 6, June 1997 Page(s):436 - 446.

[9] Kumar, A.; Allen, P.E., "An 80MHz Noise Optimized Continuous-Time Bandpass Filter in 0.25¿m BiCMOS" *Custom Integrated Circuits Conference, 2007. CICC '07*, .IEEE 16-19 Sept. 2007 Page(s):679 - 682.

[10] Andreani, P.; Mattisson, S., "A 100MHz CMOS gm–C bandpass filter" *Solid-State Circuits Conference, 1999. ESSCIRC '99. Proceedings of the 25th European,* 21-23 Sept. 1999 Page(s):374 - 377.