A High-Linearity Low-Noise Reconfiguration-Based Programmable Gain Amplifier

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***Abstract*—This paper presents a high-linearity low-noise small-size programmable gain amplifier (PGA) based on a new low-noise low-distortion transconductor and a proposed reconfiguration technique. The proposed transconductor combines an inverter-based differential pair with an adaptive biasing circuit to reduce noise and distortion. The reconfiguration technique saves the chip size by half and improves the bandwidth of the amplifier by utilizing the same differential pair for the input transconductance and load-stage, interchangeably. Fabricated in 0.18-µm CMOS, the proposed PGA shows a dB-linear control range of 21dB in 16 steps from -11dB to 10dB with a gain error of less than ±0.33dB, an IIP3 of 7.4÷14.5dBm, a P1dB of -7÷1.2dBm, a noise figure of 13dB, and a 3-dB bandwidth of 270MHz at the maximum gain, respectively. The PGA occupies a chip area of 0.04 mm2 and consumes only 1.3mA from the 1.8V supply.**

I. INTRODUCTION

Variable gain amplifiers (VGAs) are key building blocks in many applications to accommodate a large dynamic range of signals, for example, in various wireless communication systems [1-2]. VGAs are usually implemented in a cascade of many gain stages to satisfy the large dB-linear gain range requirement [1-2]. Nguyen [2] proposed a VGA architecture that can provide an 84dB dB-linear gain range, while consuming the smaller power and chip area, compared to those of conventional topology by combining one variable and three fixed gain amplifier stages. The variable gain stage proposed in [2] consists of a differential pair with diode-connected active loads. By simultaneously varying the size and bias current of the input and load transistors by the same ratio, the gain is controlled to follow the pseudo-exponential approximation function, $e^{2x} \approx (1+x)/(1-x)$. The simultaneous variation of the size and bias current keeps the current density of the transistors at the same value at all gain levels, leading to better linearity at a low gain compared to the case of the current density controlled VGA reported in [1]. However, the linearity of the VGA is still limited by the inherent nonlinearity of the input and load transistors. The variable gain stage shown reported in [2] can be considered a cascade of V-I (G_m-stage) and I-V (diode-connected active loads) converters. The distortion caused by the V-I converter (pre-distortion) can be eliminated by the inversion I-V conversion (distortion). Therefore, for unity gain condition, the nonlinearity generated by the G_m-stage is cancelled by the load-stages, leading to a very good linearity. However, for the voltage gain that is greater (or smaller) than one, the transistor size and the bias current of the G_m-stage becomes larger (or smaller) than that of the load. Therefore, the signal swing at the input of the load-stage becomes larger (or smaller) than that of the G_m-stage. Thus the distortion is not fully compensated, leading to linearity degradation. In summary, the variable gain stage reported in [2] shows the best linearity at unity gain, and at other gains, the linearity is determined by the combination of the V-I/I-V distortion compensation and the linearity of the G_m-/load-stage. Therefore, transconductance linearization techniques are required to further improve the linearity of VGAs.

This paper proposes a new low-noise low-distortion transconductor that combines an inverter-based differential pair with an adaptive biasing circuit. The advantage of the proposed transconductor will be discussed in Section II. A new reconfiguration technique that utilizes the same differential pair for the G_m-stage and load-stage interchangeably is also presented to save the PGA chip size by half and improve the 3dB-bandwidth of the PGA. The new reconfiguration technique and the implementation details of the proposed 4-bit PGA are described in Section III. The experimental results are presented and discussed in Section IV. Finally, the conclusions are given in Section VI.

II. INVERTER-BASED DIFFERENTIAL PAIR WITH ADAPTIVE BIASING

In the conventional differential pair, the common-source node does not stay constant, but fluctuates with respect to the input signal amplitude. This fluctuation of the common-source node voltage is the reason for the distortion. [3,4] introduced an adaptive biasing circuit that can be used to keep the common-source node as a perfect virtual ground by varying the bias current of the differential pair with respect to the amplitude variation of the input signal. However, the small-signal transconductance of the differential pair with adaptive biasing is smaller than that of the conventional differential

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pair. The reason is because a part of total bias current is injected into the adaptive biasing circuit that senses the input voltage but does not generate any output current. The larger the injected current is the lower small-signal transconductance is provided by the differential pair with adaptive biasing, leading to higher input referred noise. Thus the differential pair with adaptive biasing introduced in [3,4] trades small-signal transconductance and noise performance for low distortion performance.

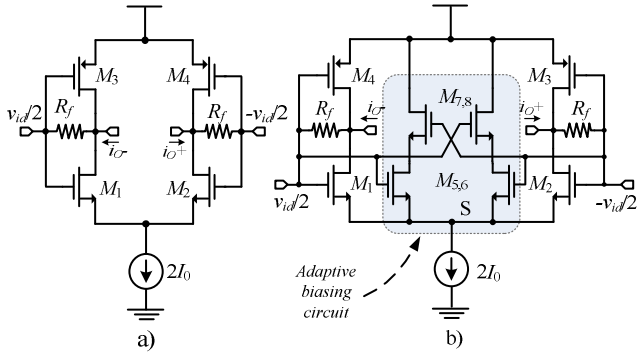

Fig. 1. (a) Inverter-based differential pair and (b) Inverter-based differential pair with adaptive biasing

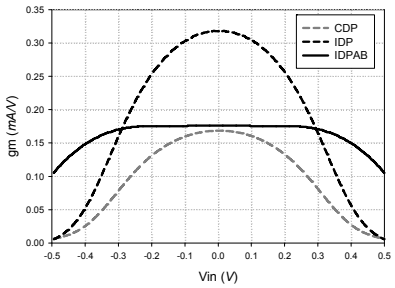

Fig. 2. Simulated g_m vs. input signal amplitude of the CDP, IDP and IDPAB

Fig. 1(a) shows a differential amplifier based on a shunt-feedback inverter. The transconductance of the inverter-based differential pair (IDP) shown in Fig. 1(a) can be twice that of the conventional differential pair (CDP), by properly sizing the PMOS transistor and for large enough of feedback resistor, R_f. Due to higher transconductance, the IDP offers much smaller input referred noise compared to the CDP. Moreover, by adopting shunt-feedback resistors, the output common mode voltage is defined without any additional circuit for biasing and common-mode feedback. By applying adaptive biasing circuit introduced in [3, 4] to the inverter-based differential pair, the disadvantages of adaptive biasing technique on transconductance and noise are compensated while low distortion performance is still archived.

The new highly linear transconductance stage that combines the inverter-based differential pair and adaptive biasing technique is shown in Fig. 1(b). In Fig. 1(b), the adaptive biasing block varies the bias current of the inverter by sensing the input signal amplitude. When the input signal, v_{id}, is small, the cross-coupled transistor pairs M_7 and M_8 operate in saturation mode while M_5, M_6 are in linear mode. When the input signal, v_{id}, is large enough, one of the transistor pairs M_5 and M_6 enters into the cutoff mode, while the other fall into saturation mode, reducing the total current through the adaptive biasing circuit [3]. For the given tail current of $2I_0$, the current reduction in the adaptive biasing circuit leads to a bias current increase in the inverter-based differential pair. This increase in bias current compensates the transconductance reduction of the differential pair at a large v_{id}. By properly choosing sizes of transistors M_1-M_8 (the quantitative derivation is given in [3]), the transconductance of the inverter-based differential pair with adaptive biasing (IDPAB) in Fig. 1(b) stays constant over a wide range of input signal amplitude, thereby providing better linearity [3].

Fig. 2 shows the transconductance characteristics versus the input signal amplitude of differential pairs: CDP, IDP, and IDPAB that consume the same amount of bias current. As can be seen in Fig. 2, the transconductance of IDP is higher than that of CDP due to the additional transconductance provided by the PMOS transistor pair. By adopting adaptive biasing technique, the small-signal transconductance of IDPAB is smaller than that of IDP but slightly larger than that of CDP. The transconductance of CDP and IDP decrease with an increase in the input signal amplitude while IDPAB shows nearly constant transconductance over a wide input range.

III. Proposed PGA with a New Reconfiguration Technique

Fig. 3(a) shows the circuit details of the PGA where the gain control scheme introduced in [2] is applied but the CDP is replaced with the IDPAB for both the G_m- and load-stages. In Fig. 3(a), both arrays of G_m- and load-cells contain IDPAB cells with weighted size factors of a geometric sequence, 2^0, 2^1, $2^3 \ldots 2^{n-1}$, respectively. It means that the transistor sizes of IDPAB in the two arrays are varied in a binary weighted sequence while the current density is kept constant. By properly combining control bits, the input transconductance and the load impedance can be varied in binary sequences.

Similar to the gain control scheme reported in [2], the gain of the PGA shown in Fig. 3(a) can be varied by switching the G_m- and load-cells of the corresponding arrays ON or OFF. For example, when the control word $a_{n-1} \ldots a_2 a_1 a_0$ is set to 0… 000, all of the G_m-cells in the G_m-stage array turn OFF, except for the "G_m-cell null", while all of the load-cells in the diode-connected load array turn ON, including the "load-cell null", leading to the smallest value of input transconductance and load resistance. Thus the lowest level of voltage gain is achieved. When the control word $a_{n-1} \ldots a_2 a_1 a_0$ is changed to 0…001, the "G_m-cell 0" and "G_m-cell null" turn ON, while the "load-cell 0" turns OFF. Thus the input transconductance and the load resistance increase slightly, leading to one step increase in voltage gain. Note that in each gain step, when the i-th G_m-cell is ON, the i-th load-cell is OFF and vice versa. Therefore, each i-th G_m- and the corresponding load-cell can be combined into one reconfigurable G_m-/load-cell, as shown in Fig. 3(b), where the cell can be configured as G_m-cell (a_i = 1) or load-cell (a_i = 0) depending on the states of a_i. Fig. 3(c) shows the final circuit schematic of the proposed PGA based on the reconfigurable IDPAB-based G_m-/load-cell, which occupies approximately half the amount of chip area compared to the original PGA shown in Fig. 3(a).

The 3-dB bandwidth of PGA shown in Fig. 3 depends on parasitic capacitance at the output nodes and load resistance. In the PGA shown in Fig. 3(a), at high gain mode, some load-

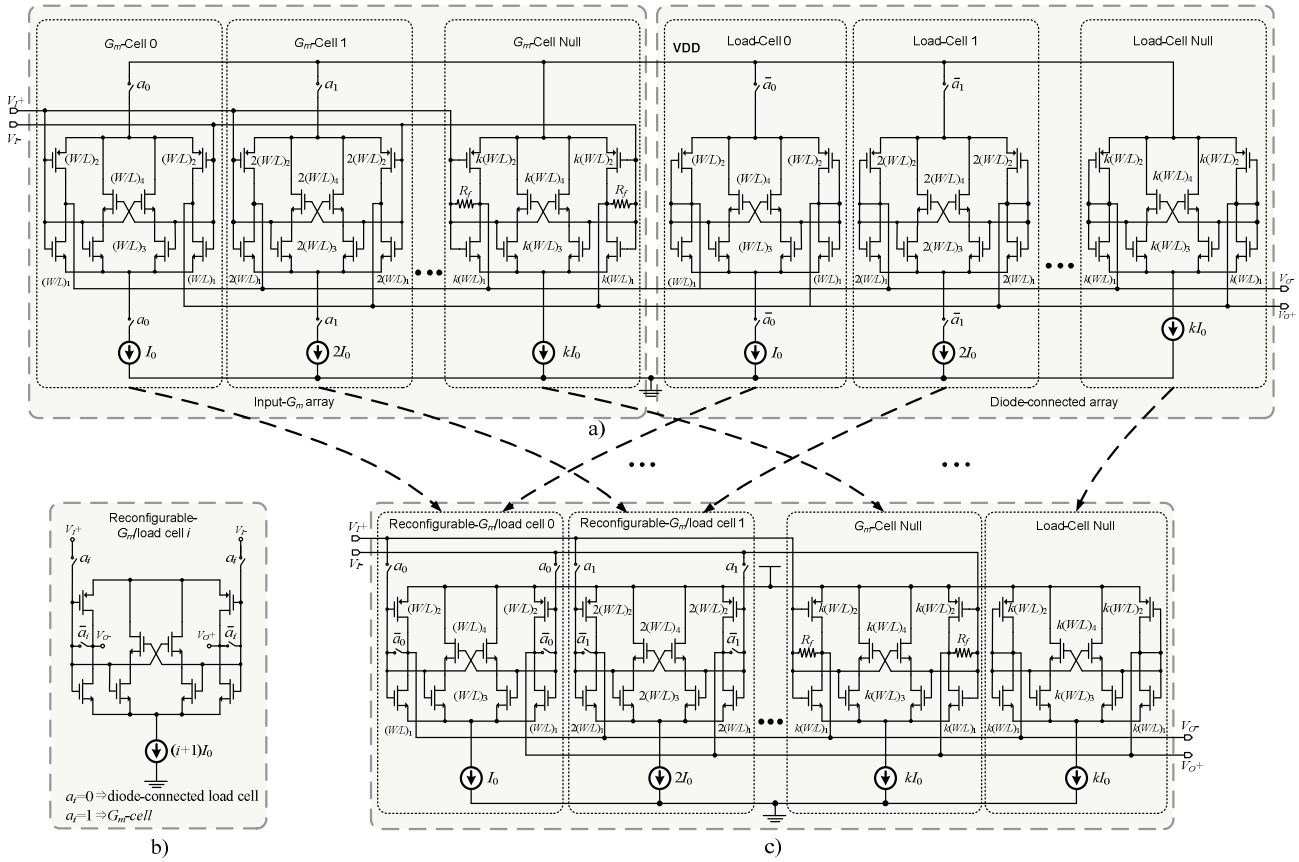

Fig. 3. (a) The proposed PGA with separate G_m- and load-cells (b) Schematic of reconfigurable G_m-/load-cell (c) The final PGA schematic based on the reconfigurable G_m-/load-cell

cells in the load array are turned OFF. The additional parasitic capacitance of each deactivated load-cells degrades the 3-dB bandwidth of the PGA. Whereas, in the PGA shown in Fig. 3(c), the reconfigurable-G_m/load cells always turn ON. Thus there is no additional parasitic capacitance from deactivated cells. Moreover, the sizes of switches $\bar{a}_i$ can be chosen so that their parasitic capacitance is smaller than additional parasitic capacitance contributed from deactivated load-cells. Therefore, the PGA shown in Fig. 3(c) provides wider 3-dB bandwidth compared to the PGA shown in Fig. 3(a).

From Fig. 3(c), since the transconductances of the G_m-/load-cells in the arrays are geometrically binary weighted, the transconductances of the G_m- and load-stages can be given by

$$G_{m\text{-}input} = g_{m0}(2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3 + ... + 2^{n-1} a_{n-1} + k) \quad (1)$$

$$G_{m\text{-}load} = g_{m0}(2^0 \bar{a}_0 + 2^1 \bar{a}_1 + 2^2 \bar{a}_2 + 2^3 \bar{a}_3 + ... + 2^{n-1} \bar{a}_{n-1} + k) \quad (2)$$

where a_i is the digital control bit, n the number of control bit, g_{m0} the transconductance of G_m-/load-cell 0, and k the size factor of "G_m-cell null". From (1) and (2), the voltage gains of the PGA shown in Fig. 3(c) can be given by

$$A_V = \frac{G_{m\text{-}input}}{G_{m\text{-}load}} = \frac{x+k}{k+2^n-1-x} \quad (3)$$

where $x = 2^0 a_0 + 2^1 a_1 + 2^2 a_2 + ... + 2^{n-1} a_{n-1}$. By defining $t=(x-2^{n-1}+0.5)/(k+2^{n-1}-0.5)$, (3) can be expressed as $A_v=(1+t)/(1-t) \approx e^{2t}$, which is a pseudo-exponential function that can provide the dB-linear range of 20dB with a gain error of less than ±0.25dB. The constant k in (3) can be adjusted to control the gain range of the PGA while trading off the gain error values. Equation (3) shows that the voltage gain of the proposed PGA does not depend on any component parameters but the ratios of the transconductance of reconfigurable G_m-/load-cells. Thus the proposed PGA is very insensitive to temperature and process variations.

IV. Measurement Results

In this work, the PGA shown in Fig. 3(c) is designed for 4 control bits to obtain the step size of around 1.4dB while the constant k is set to 6 in order to achieve the dB-linear range of 21dB. The proposed PGA is implemented in 0.18μm CMOS technology with a 1.8V supply. For comparison, a 4-bit PGA based on the CDP reported in [2] and a 4-bit PGA based on IDP are also implemented. The IDP- and IDPAB-based PGAs are designed to dissipate the same amount of current (1.3mA) while the CDP-based PGA is designed to consume 0.1mA more for bias and common mode feedback circuits. Fig. 4 shows the measured voltage gain and gain error versus the control word of the CDP-, IDP-, and IDPAB-based PGAs at a frequency of 100MHz. The three PGAs show almost the same dB-linear gain range of 21dB from -11 to 10dB with a gain error of less than ±0.33dB.

Measurements show the 3-dB bandwidth as being 270MHz, 290MHz and 470MHz at the maximum gain for the IDPAB-, CDP- and IDP-based PGAs, respectively. As can be seen in Fig. 2, IDP provides the higher small-signal

transconductance, leading to lower impedance at the output node of IDP-based PGA compared to that of CDP- and IDPAB-based PGA. Additionally, the new reconfiguration technique is adopted for IDP- and IDPAB-based PGA only. Thus the IDP-based PGA shows a lager 3-dB bandwidth compared to that of CDP-based PGA. From Fig. 2, IDPAB provides slightly higher transconductance compared to CDP. However, due to the additional parasitic capacitance from the adaptive biasing circuits in load-stage, 3-dB bandwidth of IDPAB-based PGA is still smaller than that of CDP-based PGA even thought the new reconfiguration technique is adopted. The noise figures of the CDP-, IDP-, and IDPAB-based PGA at the maximum gain of 10dB are measured at 11, 13, and 15.5dB, respectively. Fig. 5 shows the measured spectrum of three PGA outputs when 99MHz and 101MHz tones (-18dBm each) are applied, while the voltage gain of three PGAs is set at maximum of 10dB. The IDPAB-based PGA shows the value of the third inter-modulation product smaller by 12.6dB and 17.4dB compared to that of the IDP- and CDP-based PGAs, respectively. The measured input IP3 and input P1dB of the all three PGAs are summarized in Table 1. As shown in Fig. 6, the CDP-, IDP- and IDPAB- based PGAs occupy 0.05, 0.036 and 0.04 mm^2, respectively, including output buffers. Note that the chip areas of the IDP- and IDPAB-based PGAs are smaller than that of the CDP-based PGA since the reconfiguration technique is only adopted for IDP- and IDPAB-based PGAs. The slight increase in the chip area of IDPAB-based PGA compared to that of IDP-based PGA is due to the adaptive biasing circuit in the G_m- and load-stage.

Table I shows the performance summary of the three PGAs. As can be seen in Table I, by adopting adaptive biasing technique, the IDPAB-based PGA trades noise figure and bandwidth performances for linearity performance. To compare the amplifiers in term of linearity, gain, bandwidth, noise, and power consumption, a figure of merit (*FoM*) that is defined as in (4) is calculated:

$$FoM = \frac{IIP3[mW] \times Av \times BW[MHz]}{P_{dc}[mW] \times (F-1) \times 1[MHz]} \quad (4)$$

where BW is the bandwidth, F the noise factor, and P_{dc} the power consumption of the amplifiers. The figure of merits in Table I is calculated at highest gain. Due to much higher IIP3 at highest gain, IDPAB-based PGA still archives much better *FoM* even with smaller bandwidth and higher noise figure compared to that of IDP-base PGA.

TABLE I. PERFORMANCE COMPARISONS

	CDP-based PGA	**IDP- based PGA**	**IDPAB-based PGA**	Units
Technology	0.18µm CMOS	**0.18µm CMOS**	**0.18µm CMOS**	-
Power/ Supply	2.52 /1.8	**2.34 /1.8**	**2.34 /1.8**	mW /V
Gain range/ gain step	(-11.2÷10.6) /1.45	**(-11÷10.5) /1.43**	**(-11÷10.2) /1.41**	dB /dB
Gain error	< ±0.27	**< ±0.33**	**< ±0.33**	dB
Bandwidth	290	**470**	**270**	MHz
IIP3	-3÷6.3	**-1.5÷12.3**	**7.4÷14.5**	dBm
P1dB	-10.5÷-5.2	**-7.5÷-0.7**	**-7÷1.2**	dBm
NF	15.5	**11**	**13**	dB
Die area	0.05	**0.036**	**0.04**	mm^2
FoM	5.7	**41.1**	**108.3**	

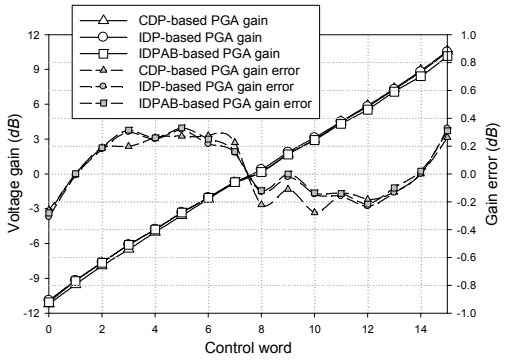

Fig. 4. Measured gain and gain error versus control word of CDP-, IDP-, and IDPAB-based PGA

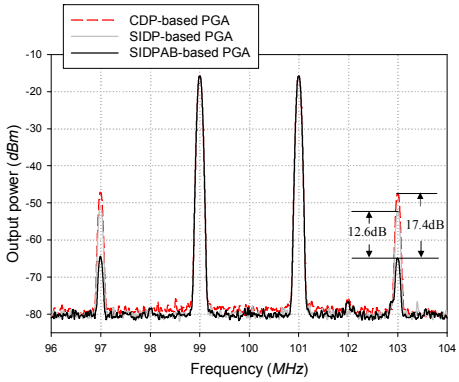

Fig. 5. Two tone test results of CDP-, IDP- and IDPAB-based PGAs at highest gain for -18dBm input power

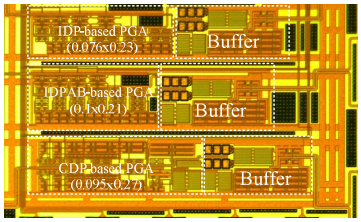

Fig. 6. Chip microphotograph of CDP-, IDP- and IDPAB-based PGAs

V. CONCLUSIONS

An all-CMOS programmable gain amplifier that is based on a proposed inverter-based differential pair with adaptive biasing and a new reconfiguration technique is introduced. By adopting the proposed schemes, the proposed PGA shows about 10dB higher IIP3, 2.5dB lower noise figure and smaller chip size, compared to the conventional PGA while consuming about the same amount of current.

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